



SLP7N65S / SLF7N65S

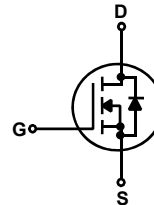
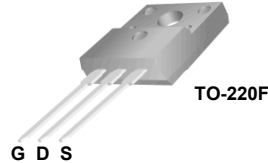
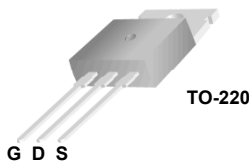
# SLP7N65S / SLF7N65S 650V N-Channel MOSFET

## General Description

This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

## Features

- 7.5A, 650V,  $R_{DS(on)} = 1.4\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 48nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	SLP7N65S	SLF7N65S	Units
V <sub>DSS</sub>	Drain-Source Voltage	650		V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	7.5	A
		- Continuous (T <sub>C</sub> = 100°C)	4.6	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	21		A
V <sub>GSS</sub>	Gate-Source Voltage	±30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	128		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	7.5		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	12.6		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	3.3		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	78	35	W
		0.62	0.28	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

## Thermal Characteristics

Symbol	Parameter	Max		Units
		SLP7N65S	SLF7N65S	
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.6	3.57	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.64	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 3.75\text{ A}$	--	1.2	1.4	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 3.75\text{ A}$ (Note 4)	--	7.5	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1100	--	pF
$C_{oss}$	Output Capacitance		--	251	--	pF
$C_{riss}$	Reverse Transfer Capacitance		--	14	--	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 7.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	15.2	--	ns
$t_r$	Turn-On Rise Time		--	20	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	46	--	ns
$t_f$	Turn-Off Fall Time		--	22	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = 520\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	48	--	nC
$Q_{gs}$	Gate-Source Charge		--	7	--	nC
$Q_{gd}$	Gate-Drain Charge		--	7.4	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.5	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	21	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 7.5\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 7.5\text{ A},$	--	320	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	3.7	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L=1\text{mH}, I_{AS} = 16\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 7.5\text{A}, di/dt \leq 300\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

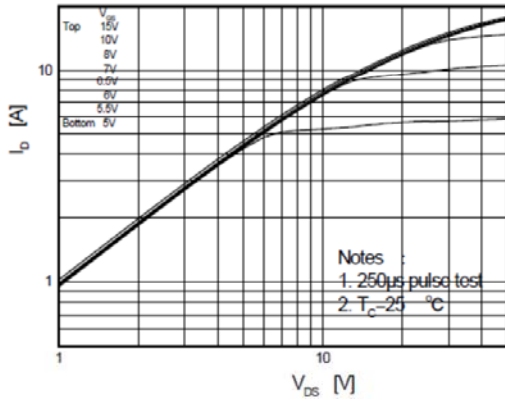


Figure 1. On-Region Characteristics

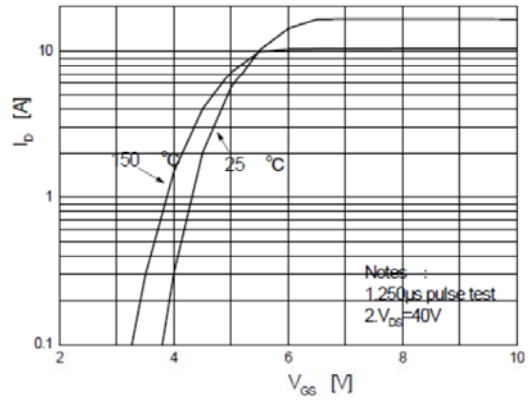


Figure 2. Transfer Characteristics

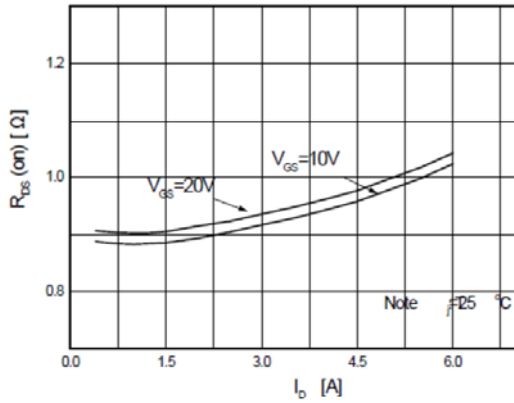


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

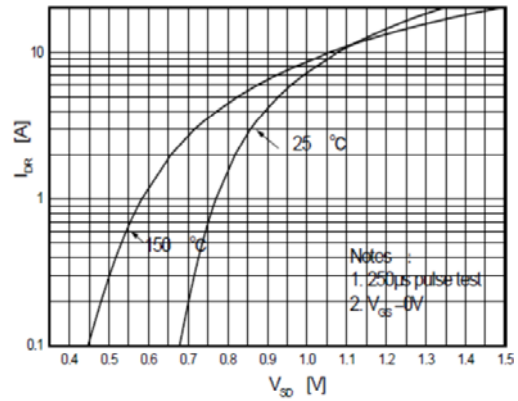


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

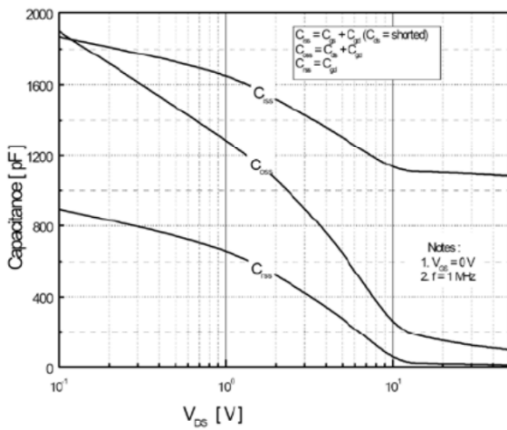


Figure 5. Capacitance Characteristics

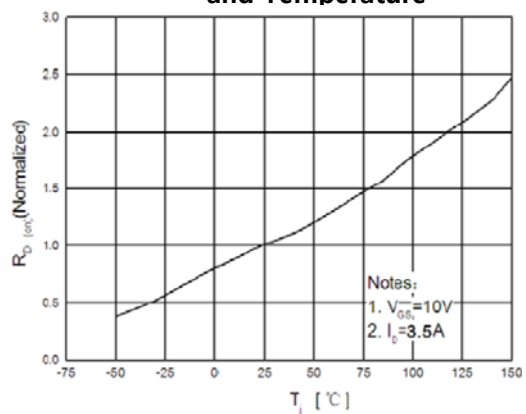


Figure 6. On-Resistance Variation vs Temperature

Typical Characteristics (Continued)

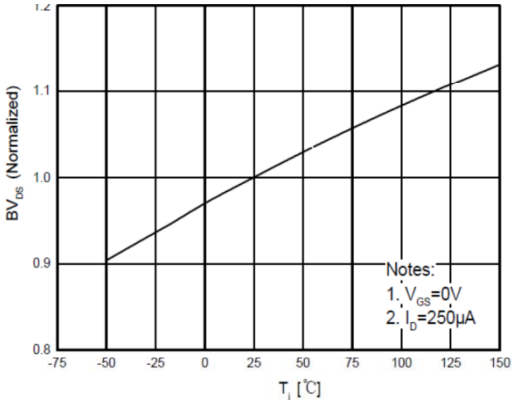
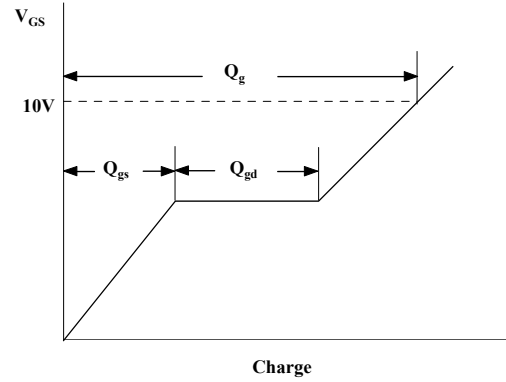
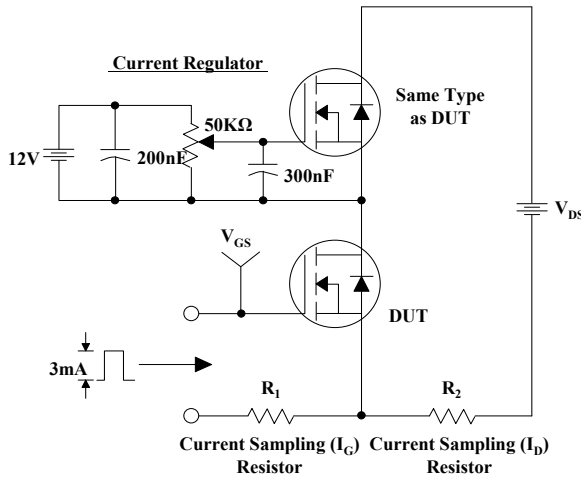
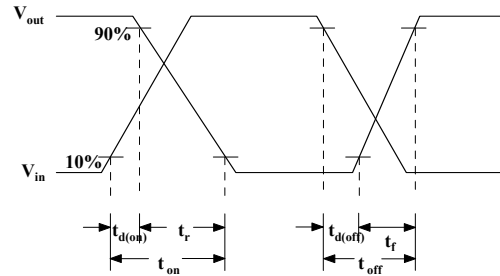
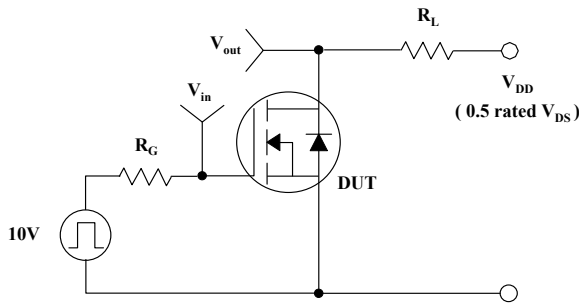


Figure 7. Breakdown Voltage Variation vs Temperature

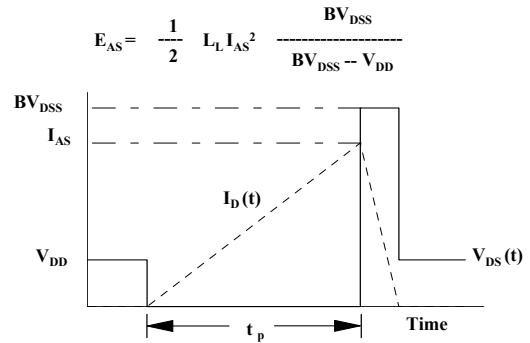
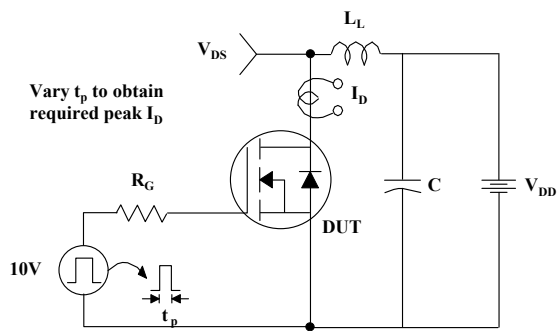
### Gate Charge Test Circuit & Waveform



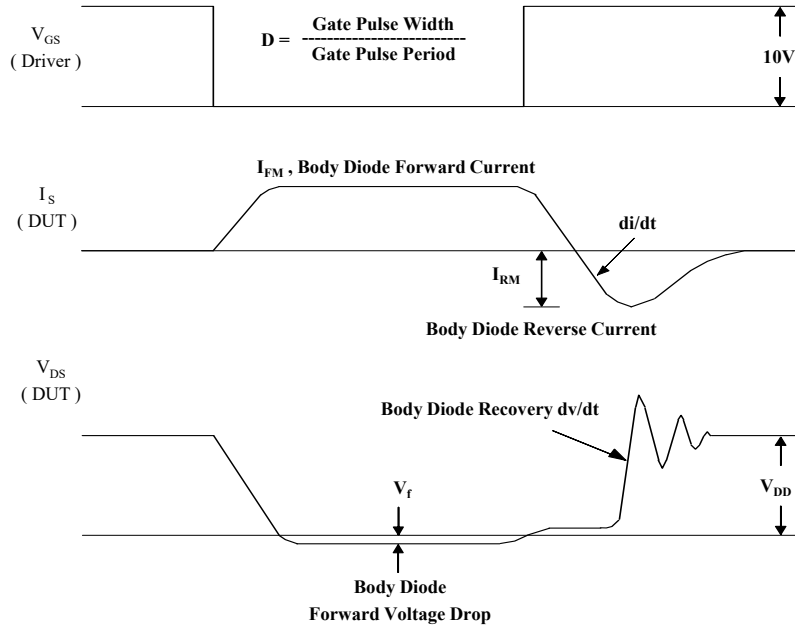
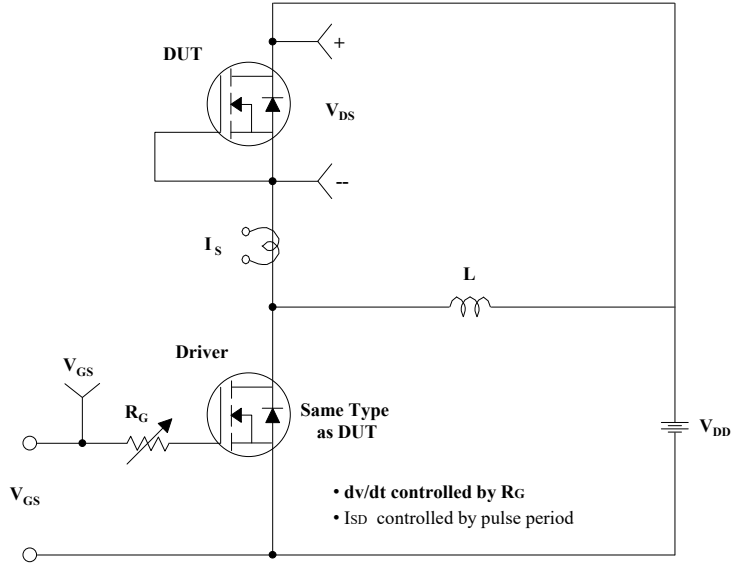
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



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