Maplesemi

LEAD FREE
Pb
RoHS

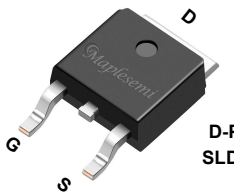
SLD750U / SLF750U
430V N-Channel MOSFET

General Description

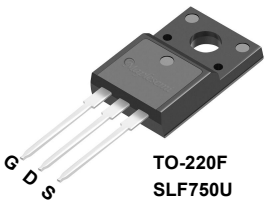
This Power MOSFET is produced using Maple semi's advanced planar stripe DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

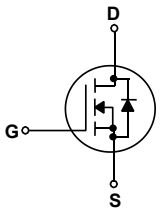
- N-Channel:430V 11A
  $R_{DS(on)Typ}$=0.54Ω@V_{GS} = 10 V
- Very Low On-resistance RDS(ON)
- LowCrss
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



D-PAK
SLD750U



TO-220F
SLF750U



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	SLD750U / SLF750U		Units
V_{DSS}	Drain-Source Voltage	430		V
I_D	Drain Current - Continuous (T_C = 25℃)	11		A
	- Continuous (T_C = 100℃)	6.7		A
I_{DM}	Drain Current - Pulsed (Note 1)	33		A
V_{GSS}	Gate-Source Voltage	±30		V
E_{AS}	Single Pulsed Avalanche Energy	437		mJ
P_D	Power Dissipation (T_C = 25℃)	-	35	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	-	3.57	W/℃
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		℃
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		℃

* Drain current limited by maximum junction temperature.

Package Marking

Part Number	Top Marking	Package	Packing Method	MOQ	QTY
SLD750U	SLP750U	TO-252	Tape	2500	25000
SLF750U	SLF750U	TO-220F	Tube	1000	5000

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	430	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =400 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 340V, T_C = 125℃	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} =30V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D =5.5 A	--	0.54	0.62	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} =25 V, V_{GS} = 0 V, f = 1.0 MHz	--	835	-	pF
C_{oss}	Output Capacitance		--	98	-	pF
C_{rss}	Reverse Transfer Capacitance		--	3.85	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS}= 210V, R_G = 25Ω ,I_D=5.5A	--	19	--	ns
t_r	Turn-On Rise Time		--	70	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	--	ns
t_f	Turn-Off Fall Time		--	27	--	ns
Q_g	Total Gate Charge	V_{DS} = 210V, I_D =5.5A, V_{GS} = 10V	--	23	--	nC
Q_{gs}	Gate-Source Charge		--	5.4	--	nC
Q_{gd}	Gate-Drain Charge		--	5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	11	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	33	A
V_{SD}	Drain to Source Diode Forward Voltage,V_{GS} = 0V, I_{SD} =11A,T J = 25℃		--	--	1.4	V
t_{rr}	Reverse Recovery Time &T_J = 25°C, IF = 5.5A di/dt = 100A/μs		--	410	-	nS
Q_{rr}	Reverse Recovery Charge & T_J = 25°C, IF =5.5A di/dt = 100A/μs		--	7	-	nC

Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J =25℃, V_{DD} =50V, V_G =10V, R_G =25Ω,
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

N- Channel Typical Characteristics

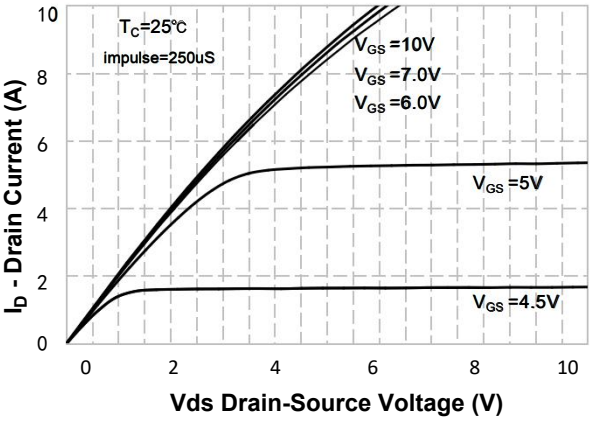


Figure 1. On-Region Characteristics

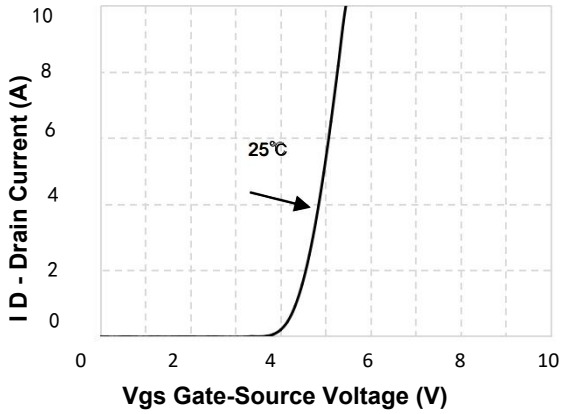


Figure 2. Transfer Characteristics

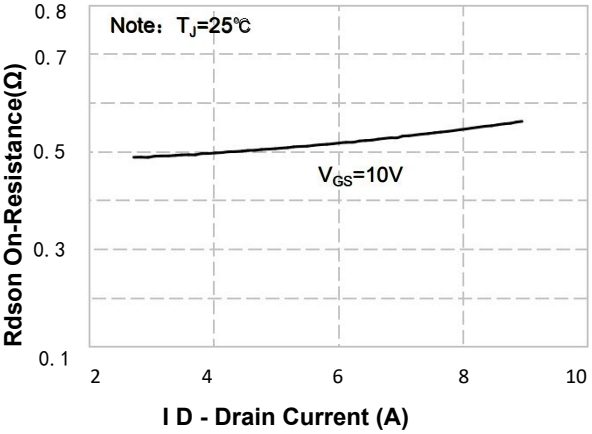


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

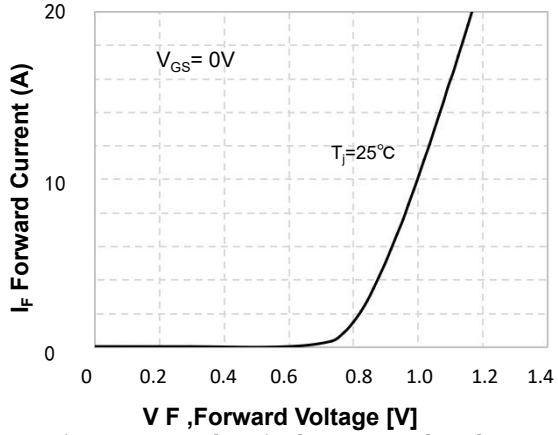


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

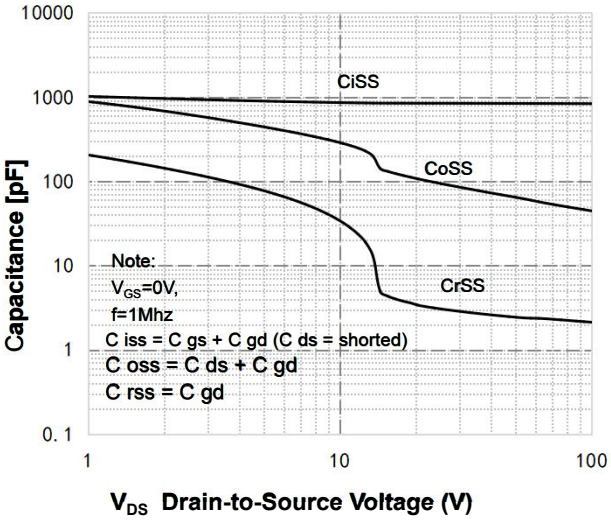


Figure 5. Capacitance Characteristics

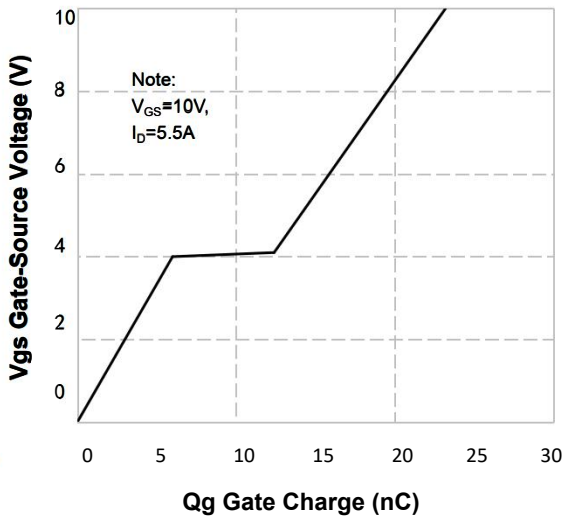


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

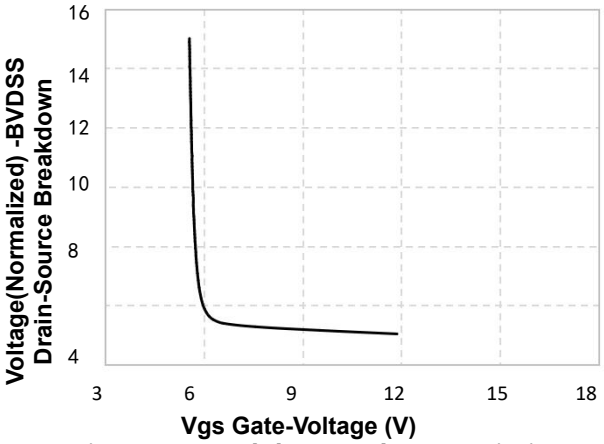


Figure 7. Breakdown Voltage Variation vs Gate-Voltage

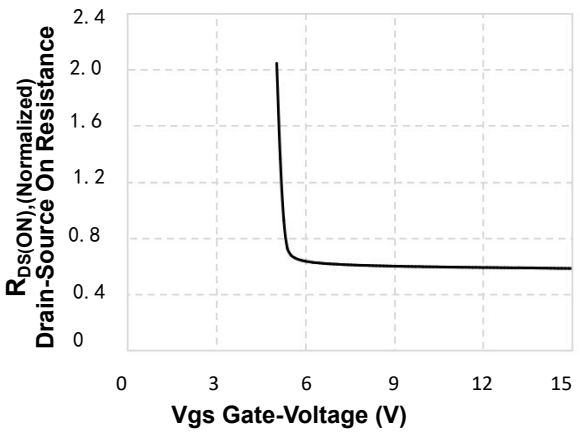


Figure 8. On-Resistance Variation vs Gate-Voltage

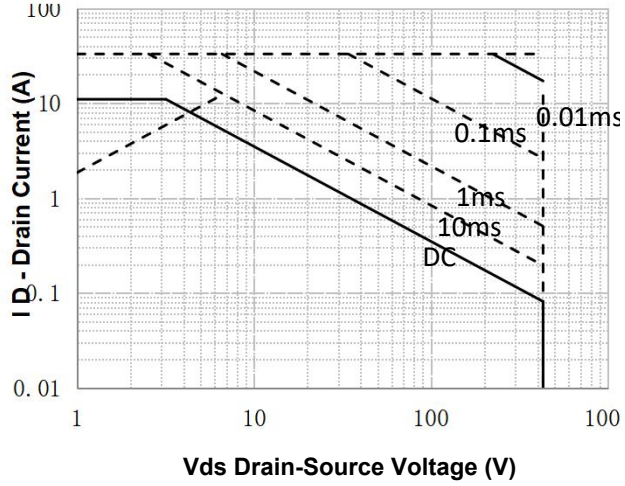


Figure 9. Maximum Safe Operating Area

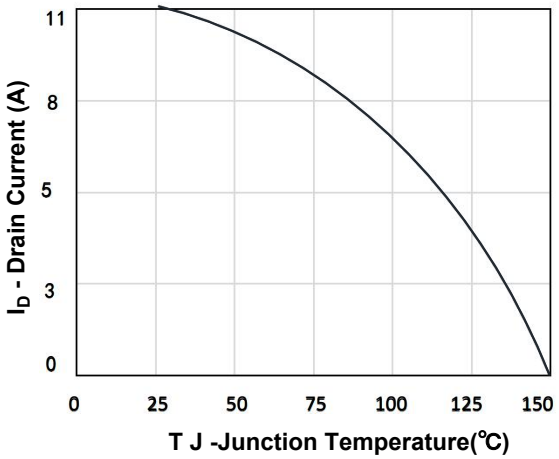


Figure 10. Maximum Drain Current vs Case Temperature

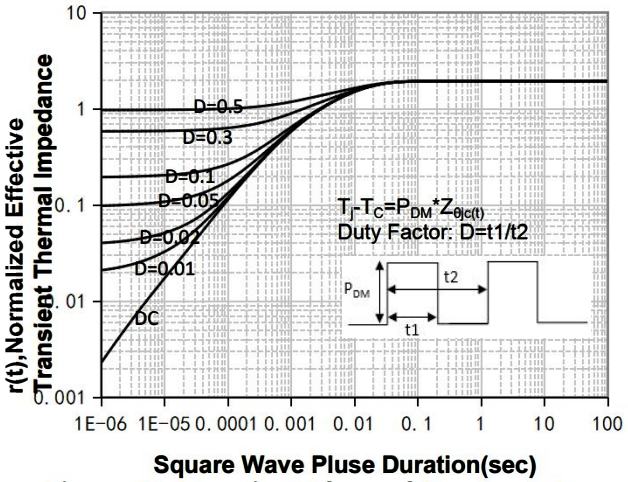
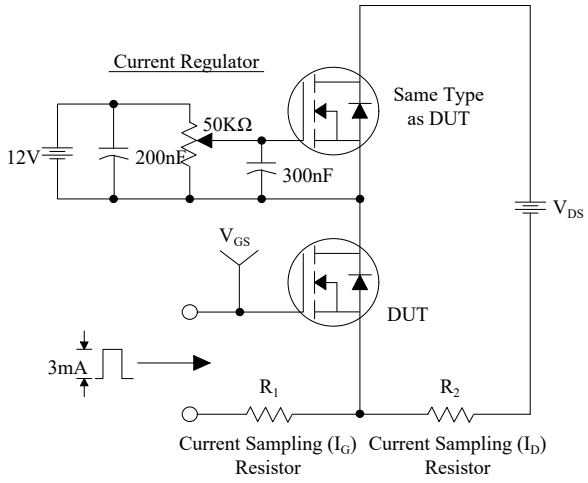
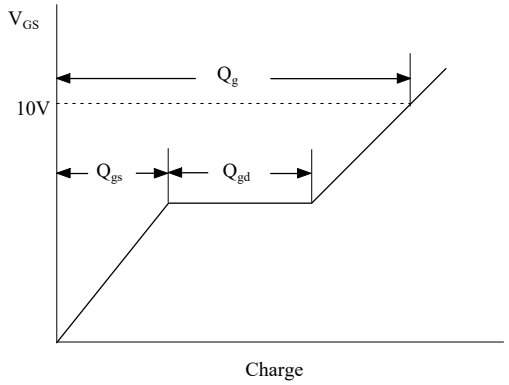


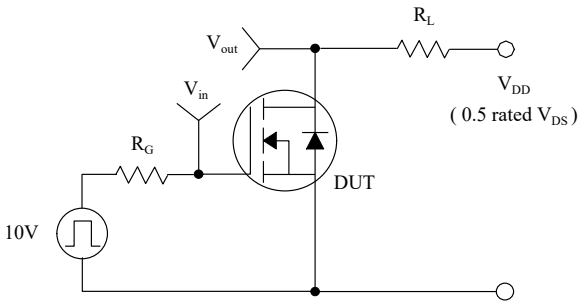
Figure 11. Transient Thermal Response Curve

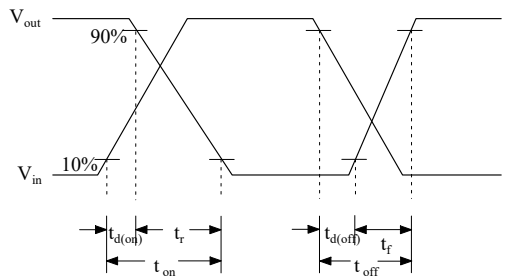
Gate Charge Test Circuit & Waveform



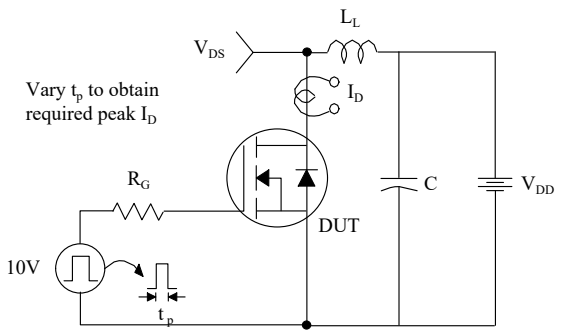


Resistive Switching Test Circuit & Waveforms

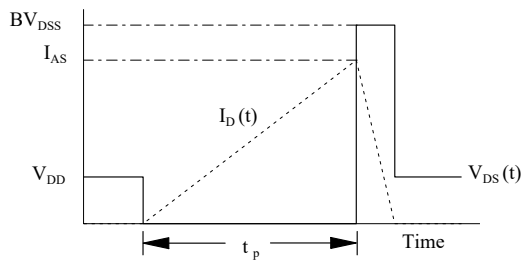




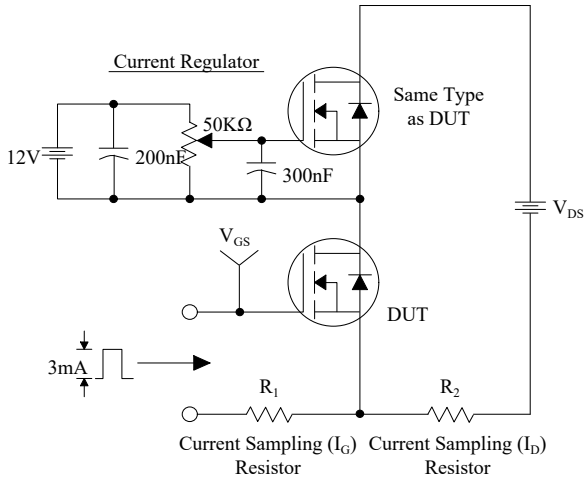
Unclamped Inductive Switching Test Circuit & Waveforms

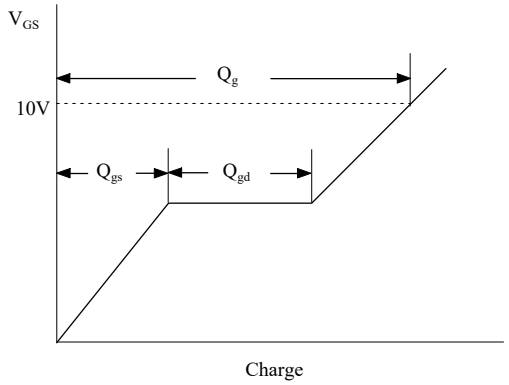


$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

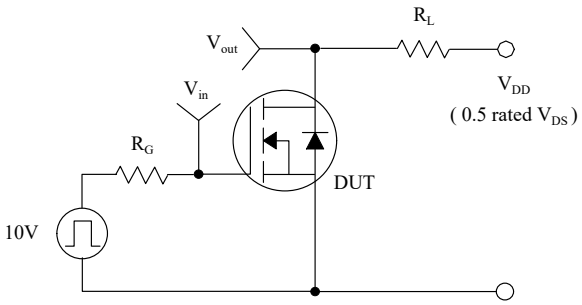


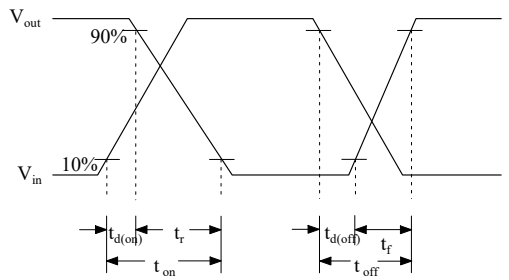
Gate Charge Test Circuit & Waveform



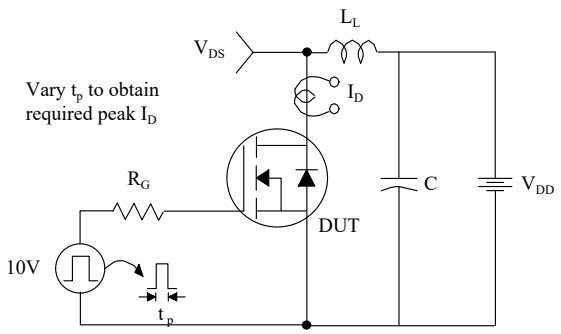


Resistive Switching Test Circuit & Waveforms

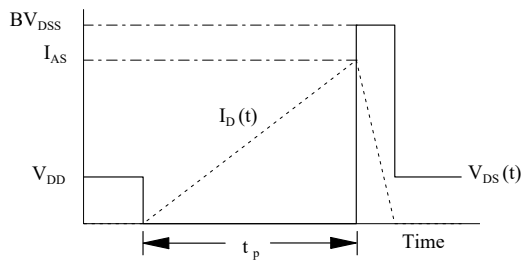




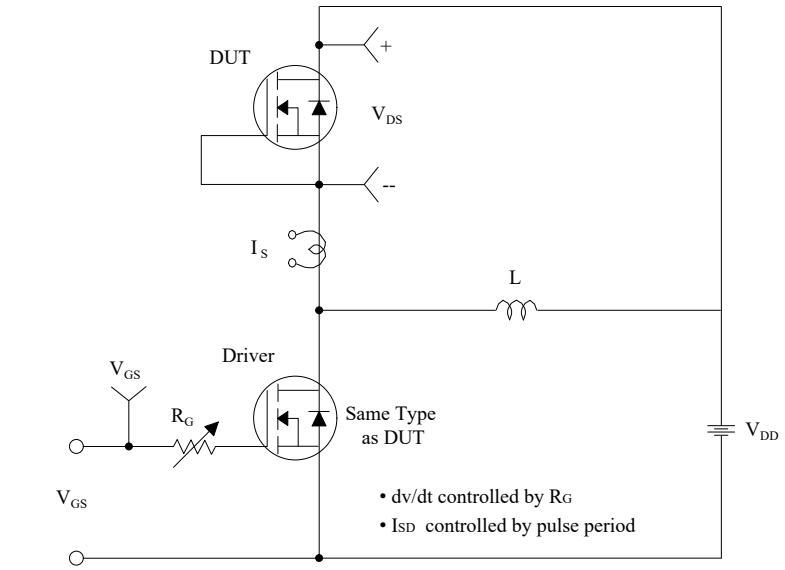
Unclamped Inductive Switching Test Circuit & Waveforms

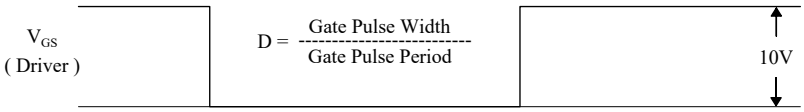


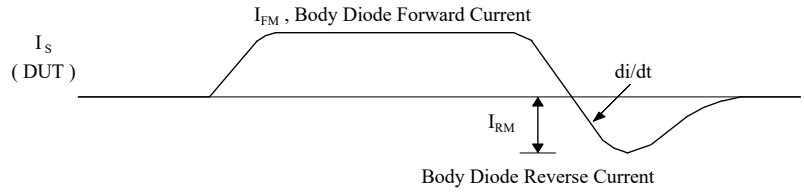
$$E_{AS} = \frac{1}{2} L_L I_{AS}^2$$

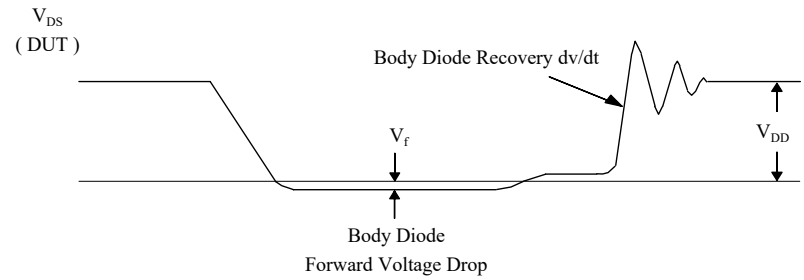


Peak Diode Recovery dv/dt Test Circuit & Waveforms

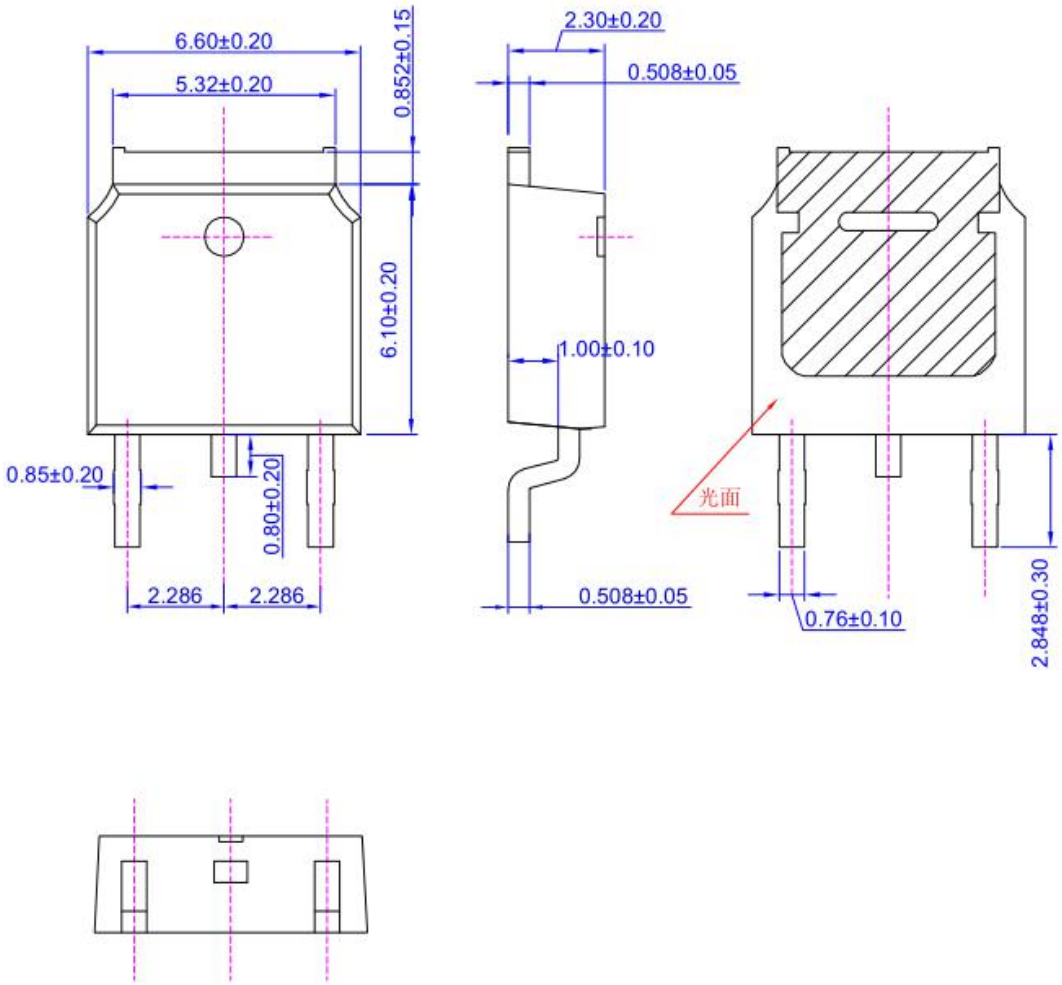






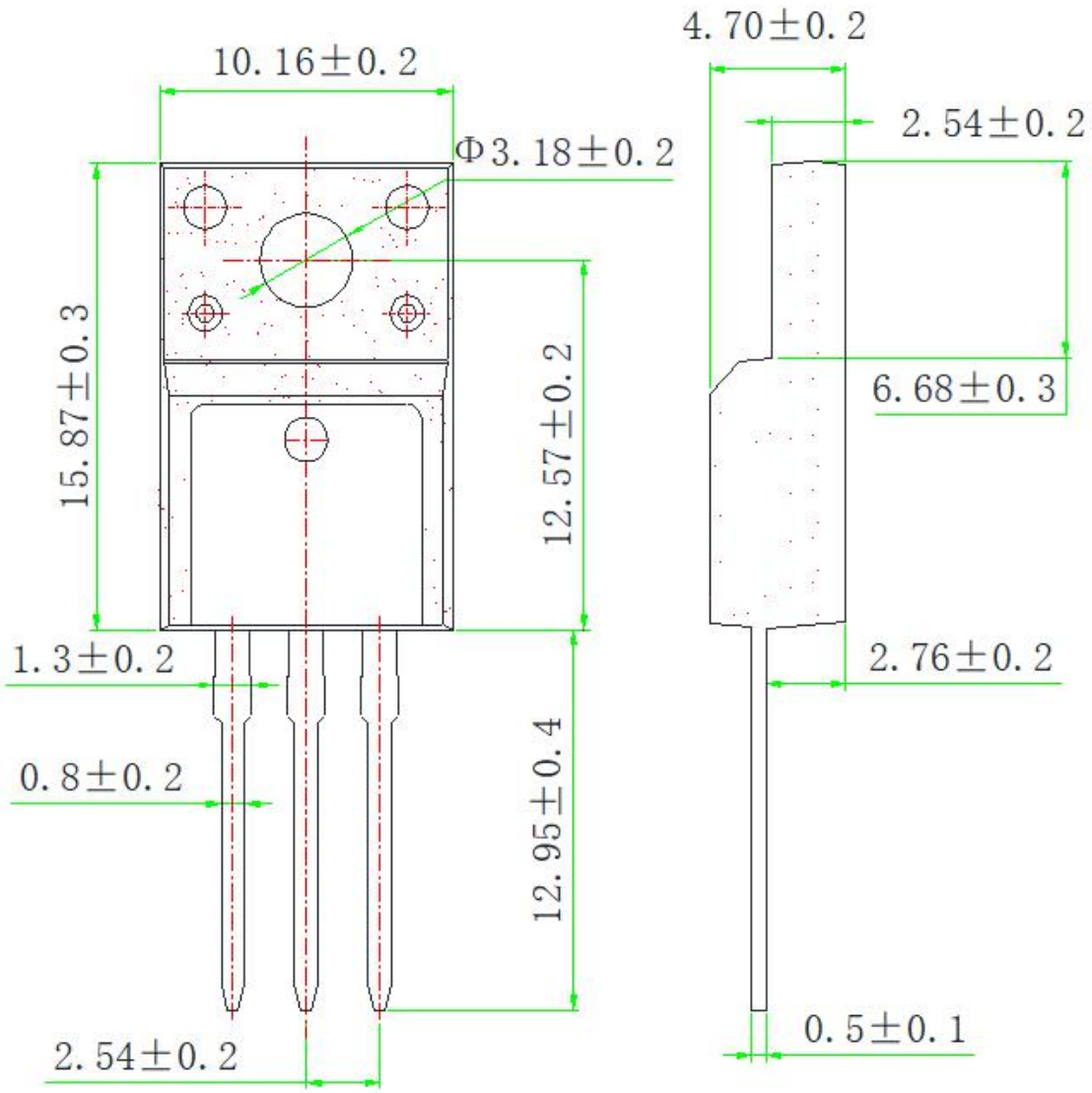


TO-252 OUTLINE



NOTE：
1The plastic package is not marked as smooth surfaceRa=0.1;Subgloss y surfaceRa=0.8
2.Undeclared tolerance±0.25,Unmarked filletRmax=0.25

TO-220F OUTLINE



Note：Distance from top pinhole to colloid surface 0.8±0.15mm

NAME	TO-220F OUTLINE	UNIT	mm	DESIGNED	Shawn Chen	THIRD ANGLE SYSTEM
DWGNO		PAGE	1 OF 1	CHECKED		
VERSION	Ver1.0	ISSUE DATE		APPROVED		

单击下面可查看定价，库存，交付和生命周期等信息

>>Maplesemi(美浦森半导体)