

# SLF12N65C/SLP12N65C

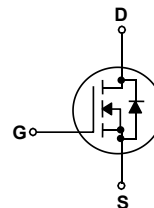
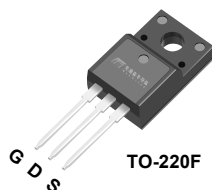
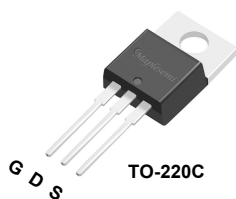
## 650V N-Channel MOSFET

### General Description

This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

### Features

- 12A, 650V,  $R_{DS(on)} = 0.75\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 52 nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	SLP12N65C	SLF12N65C	Units
V <sub>DSS</sub>	Drain-Source Voltage	650		V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	12	12 *	A
		7.4	7.4 *	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	48	48 *	A
V <sub>GSS</sub>	Gate-Source Voltage	±30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	865		mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	12		A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	23		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	230	54	W
		1.85	0.43	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150		°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

\* Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	SLP12N65C	SLF12N65C	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	0.54	2.33	°C/W
R <sub>θJS</sub>	Thermal Resistance, Case-to-Sink Typ.	0.5	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.65	--	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6\text{ A}$	--	0.63	0.75	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 6\text{ A}$ (Note 4)	--	13	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	1850	--	pF
$C_{oss}$	Output Capacitance		--	180	--	pF
$C_{rSS}$	Reverse Transfer Capacitance		--	20	--	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 325\text{ V}, I_D = 12\text{ A}, R_G = 25\text{ }\Omega$ (Note 4, 5)	--	30	--	ns
$t_r$	Turn-On Rise Time		--	90	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	140	--	ns
$t_f$	Turn-Off Fall Time		--	90	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = 520\text{ V}, I_D = 12\text{ A}, V_{GS} = 10\text{ V}$ (Note 4, 5)	--	52	--	nC
$Q_{gs}$	Gate-Source Charge		--	8.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	20	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	12	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	48	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ ,	--	430	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	5.0	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 11\text{ mH}, I_{AS} = 12\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 12\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\text{ }\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

# Typical Characteristics

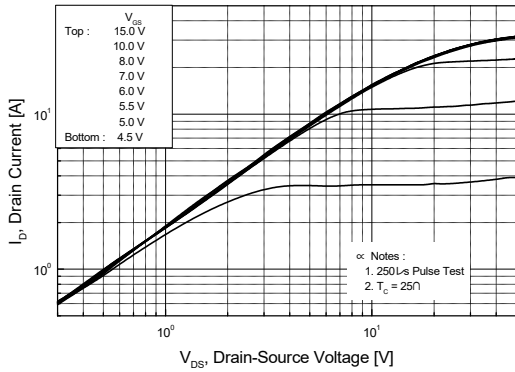


Figure 1. On-Region Characteristics

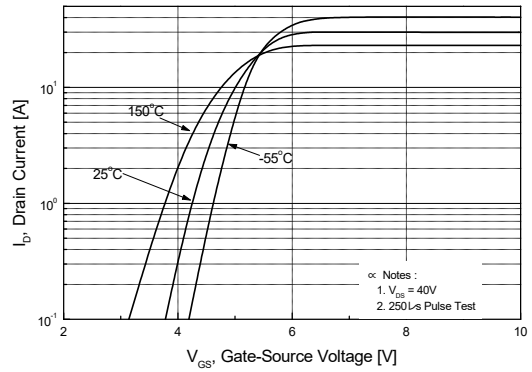


Figure 2. Transfer Characteristics

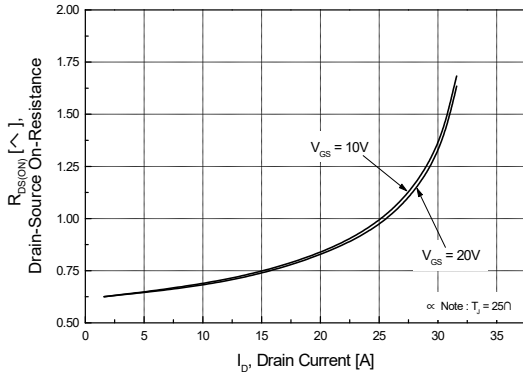


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

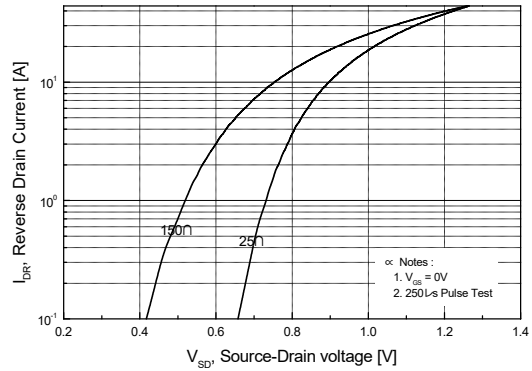


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

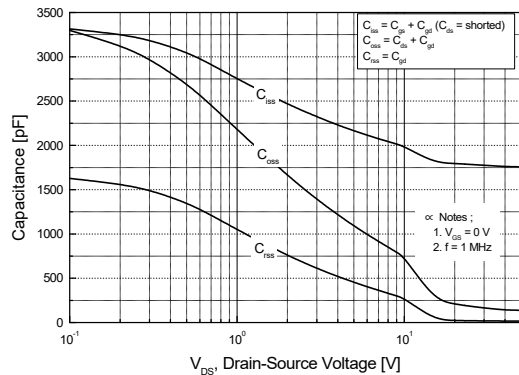


Figure 5. Capacitance Characteristics

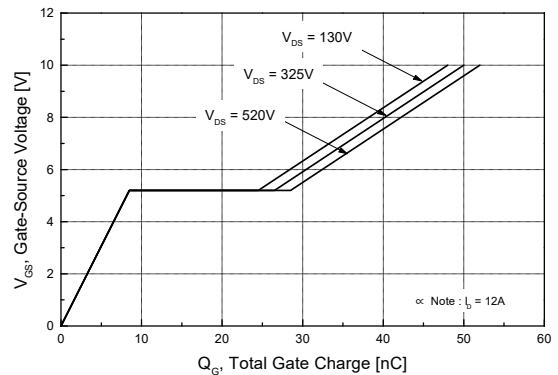


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

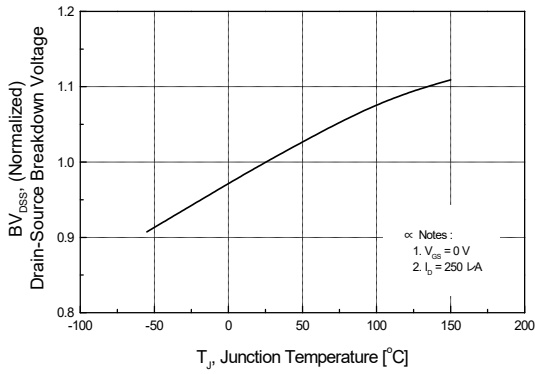


Figure 7. Breakdown Voltage Variation vs Temperature

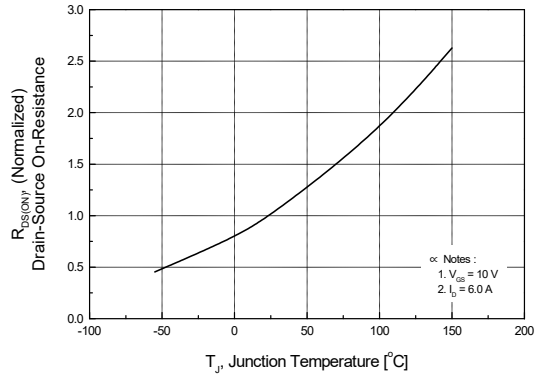


Figure 8. On-Resistance Variation vs Temperature

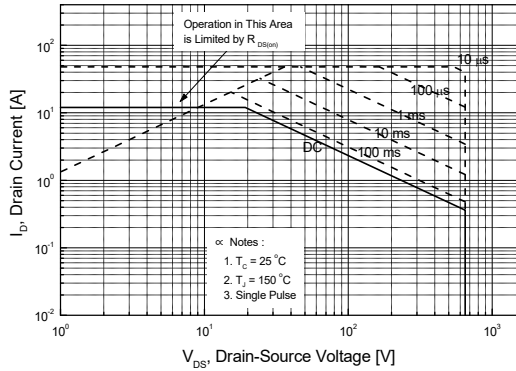


Figure 9-1. Maximum Safe Operating Area for SLP12N65C

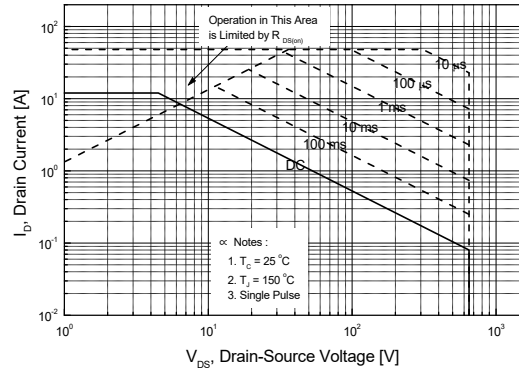


Figure 9-2. Maximum Safe Operating Area for SLF12N65C

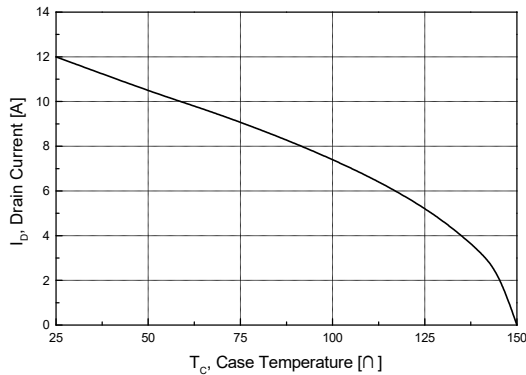


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

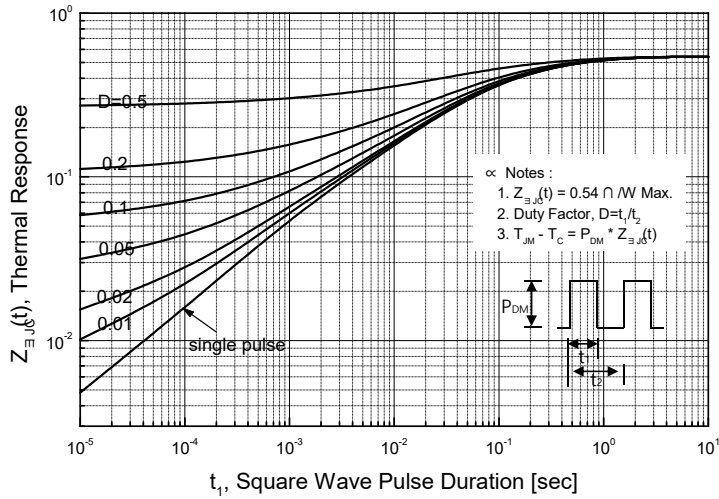


Figure 11-1. Transient Thermal Response Curve for P12N65

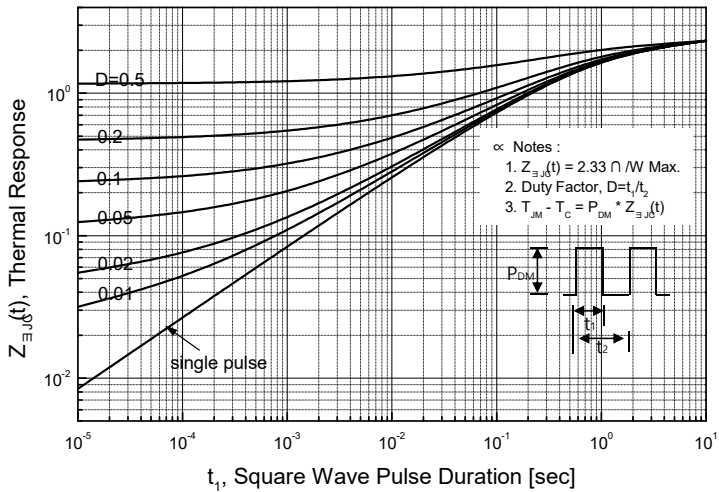
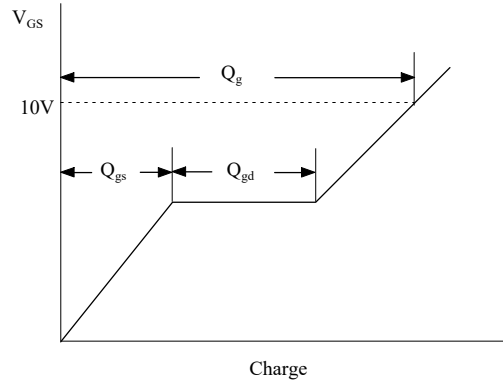
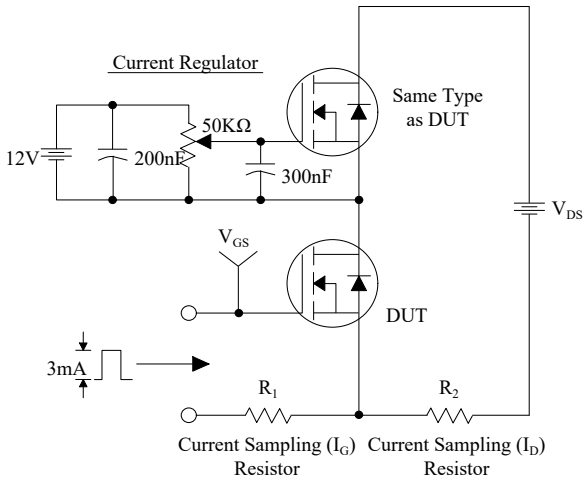
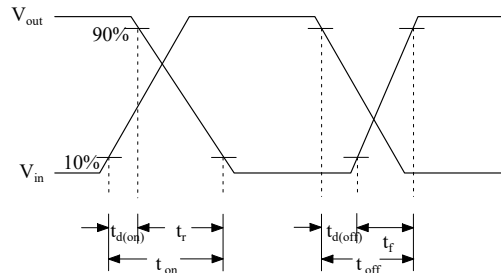
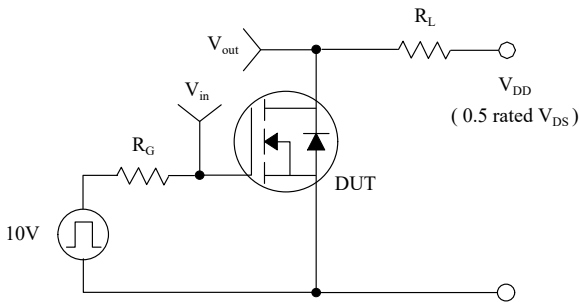


Figure 11-2. Transient Thermal Response Curve for F12N65

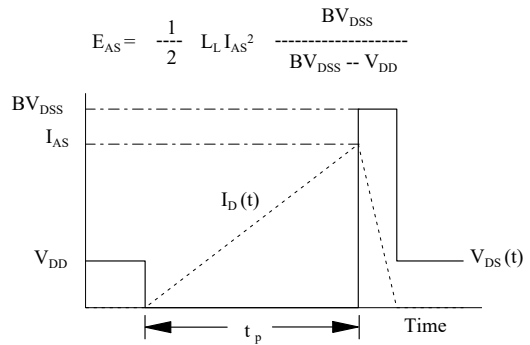
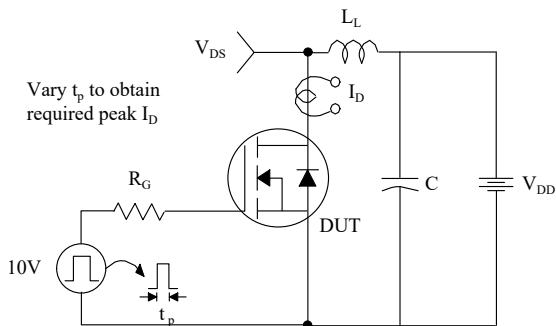
### Gate Charge Test Circuit & Waveform



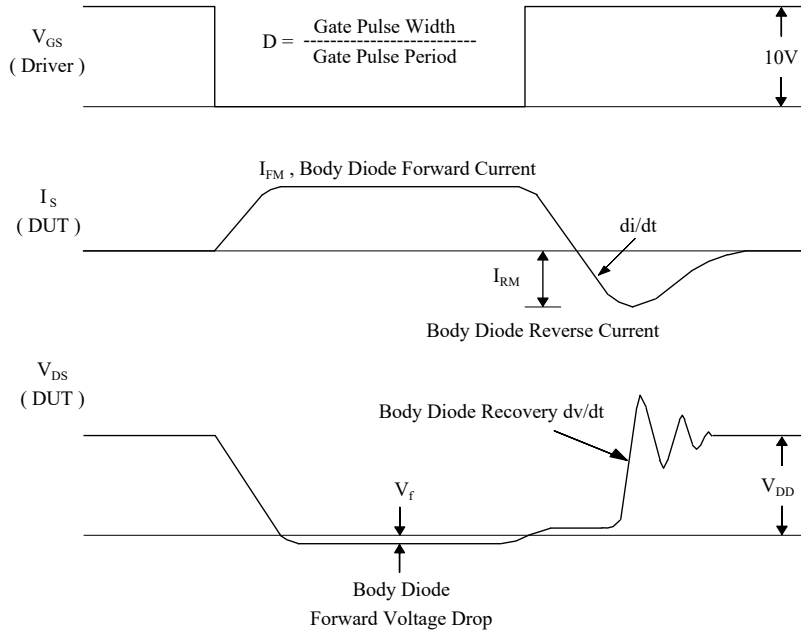
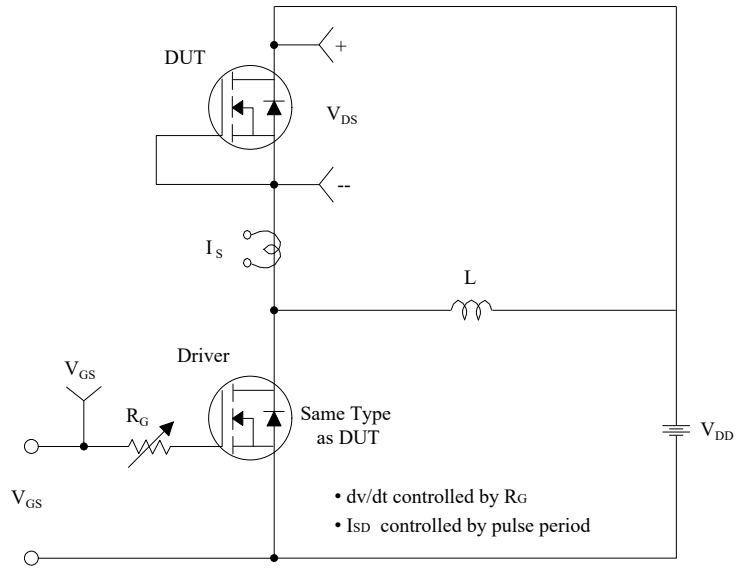
### Resistive Switching Test Circuit & Waveforms



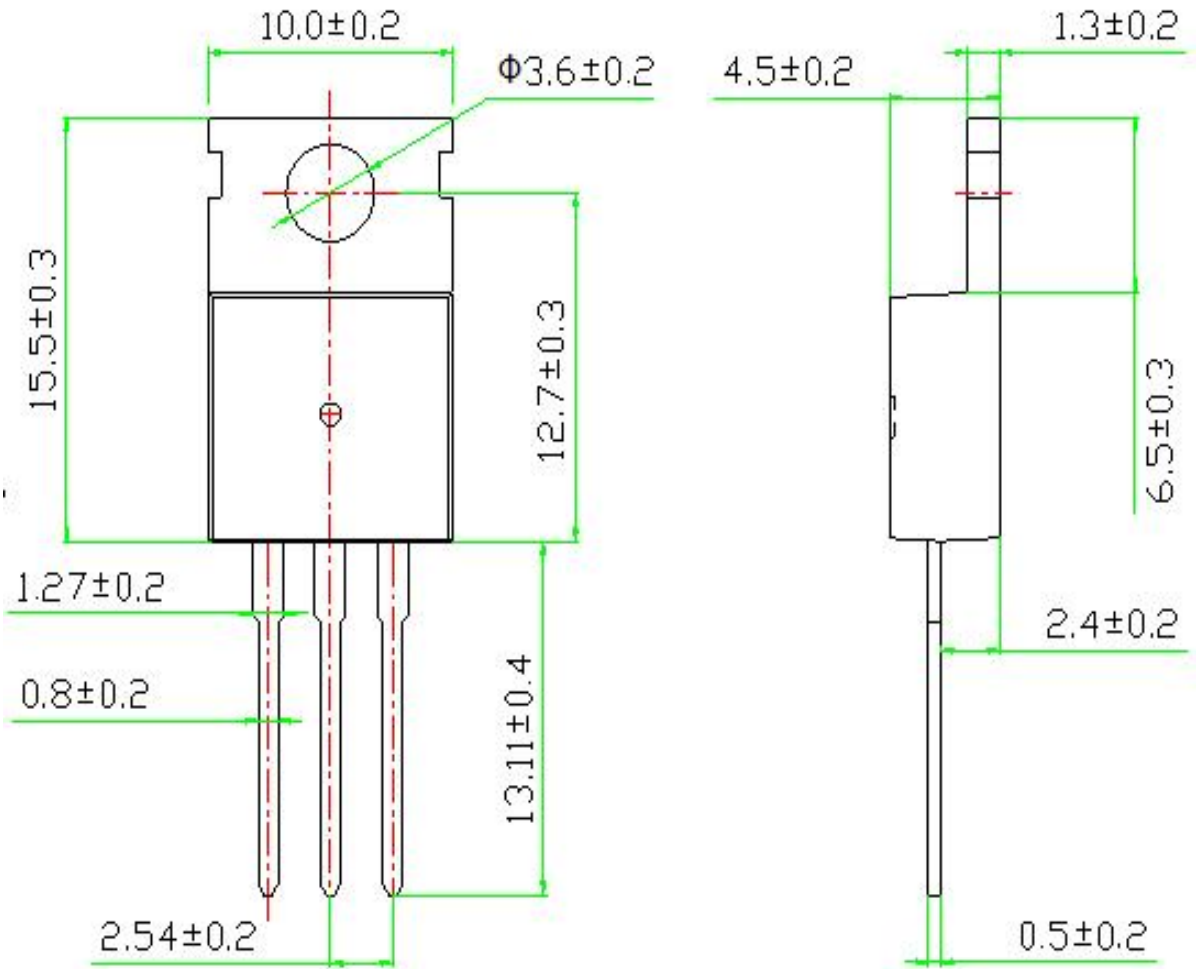
### Unclamped Inductive Switching Test Circuit & Waveforms



### Peak Diode Recovery dv/dt Test Circuit & Waveforms

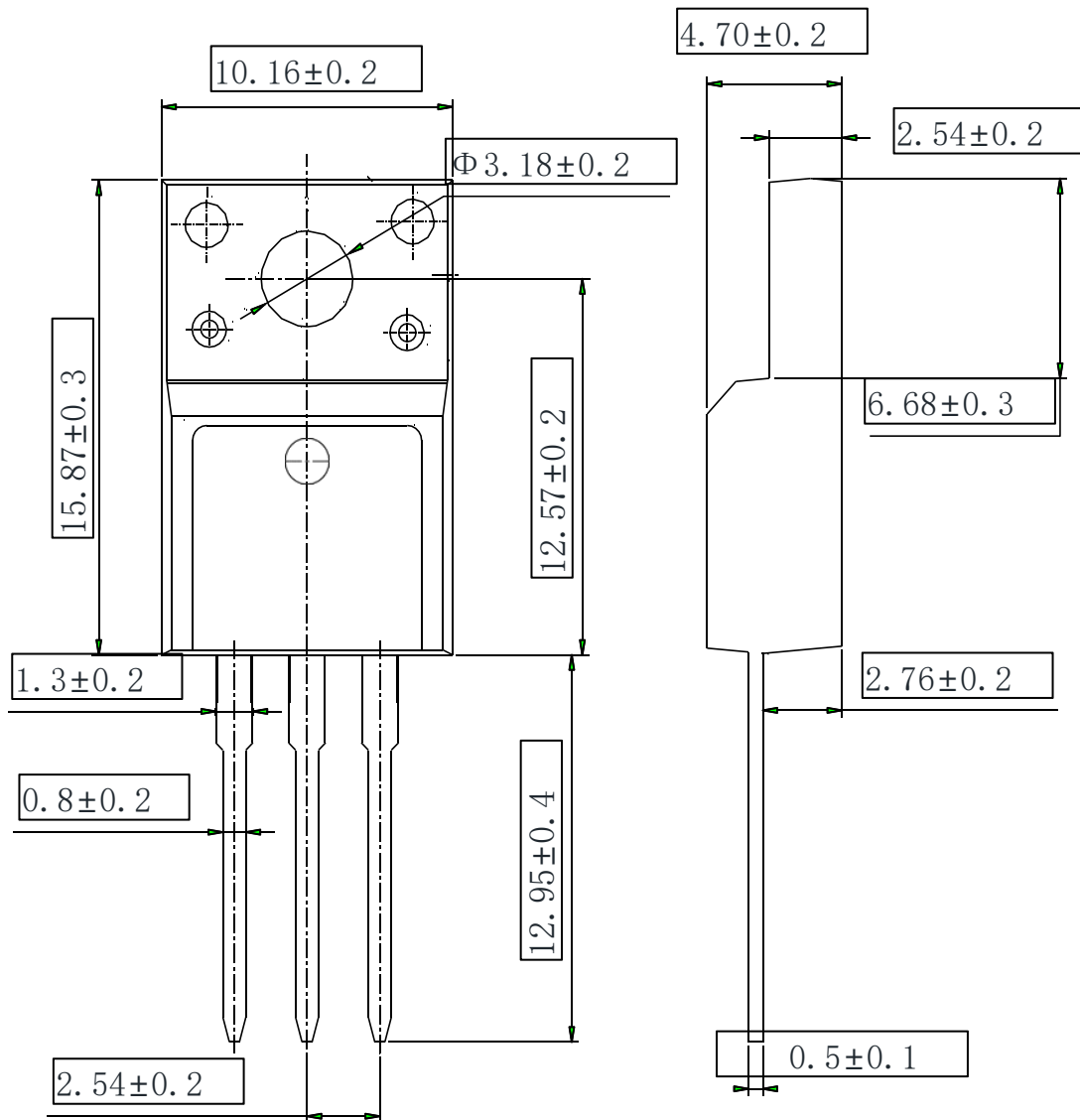


# TO-220C OUTLINE





## TO-220F OUTLINE



## NOTE:

- 1The plastic package is not marked as smooth surface  $Ra=0.1$ ; Subglossy surface  $Ra=0.8$
- 2.Undeclared tolerance  $\pm 0.15$ , Unmarked fillet  $R_{max}=0.25$

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