

## General Description

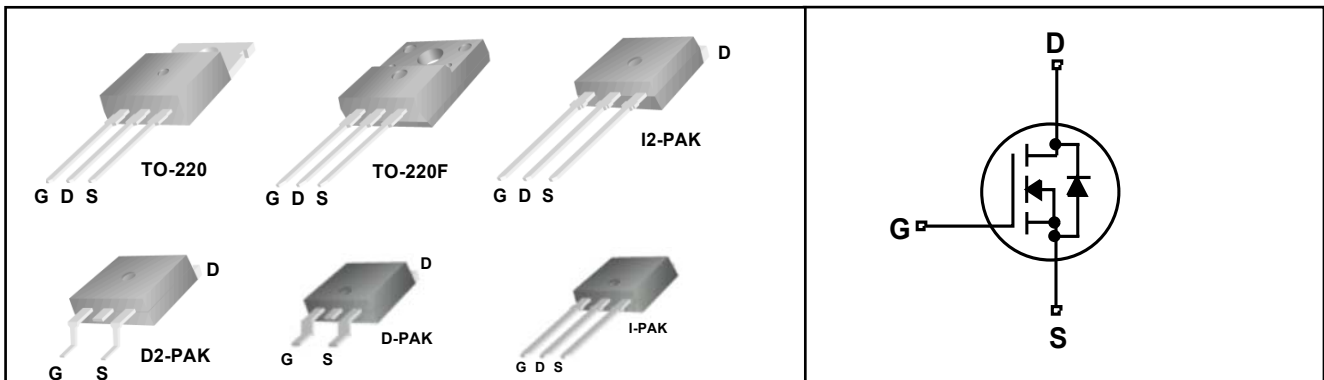
This Power MOSFET is produced using Maple semi's Advanced Super-Junction technology.

This advanced technology has been especially tailored to minimize conduction loss, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for AC/DC power conversion

## Features

- 7A, 800V, RDS(on) typ.= 0.8Ω@VGS = 10 V
- Low gate charge ( typical 25nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



## Absolute Maximum Ratings

TC = 25°C unless otherwise noted

Symbol	Parameter	D2-PAK/D-PAK I2-PAK / I-PAK/ TO-220	TO-220F	Units
VDSS	Drain-Source Voltage	800		V
ID	Drain Current	- Continuous (TC = 25°C)	7.0	7.0*
		- Continuous (TC = 100°C)	4.2	4.2*
IDM	Drain Current - Pulsed (Note 1)	13	13*	A
VGSS	Gate-Source Voltage	±30		V
EAS	Single Pulsed Avalanche Energy (Note 2)	86		mJ
IAR	Avalanche Current (Note 1)	1.7		A
EAR	Repetitive Avalanche Energy (Note 1)	0.2		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	15		V/ns
PD	Power Dissipation (TC = 25°C)	63	30	W
		- Derate above 25°C	0.5	0.24
TJ, TSTG	Operating and Storage Temperature Range	-55 to +150		°C
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		°C

\*Drain current limited by maximum junction temperature.

## Thermal Characteristics

Symbol	Parameter	Value						Units
		DPAK	IPAK	TO220	D2PAK	I2PAK	TO220F	
RθJC	Thermal Resistance, Junction-to-Case	1.9	1.9	1.9	1.9	1.9	4.2	°C/W
RθJS	Thermal Resistance, Case-to-Sink Typ.	-	-	0.5	0.5	0.5	-	°C/W
RθJA	Thermal Resistance, Junction-to-Ambient	100	100	62	62	62	80	°C/W

**Electrical Characteristics** ( TC = 25 °C unless otherwise noted )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BVDSS	Drain-Source Breakdown Voltage	VGS = 0V, ID = 250uA, TJ=25°C	800	-	-	V
		VGS = 0V, ID = 250uA, TJ=150°C	-	850	-	V
$\Delta$ BVDSS $\Delta$ TJ	Breakdown Voltage Temperature coefficient	ID = 250uA, referenced to 25°C	-	0.6	-	V/°C
IDSS	Drain-Source Leakage Current	VDS =800V, VGS = 0V	-	-	1	uA
		VDS =640V, TC = 125 °C	-	10	-	uA
IGSS	Gate-Source Leakage, Forward	VGS = 30V, VDS = 0V	-	-	100	nA
	Gate-source Leakage, Reverse	VGS = -30V, VDS = 0V	-	-	-100	nA

**On Characteristics**

VGS(th)	Gate Threshold Voltage	VDS = VGS, ID = 250uA	2.5	3.5	4.5	V
RDS(ON)	Static Drain-Source On-state Resistance	VGS =10 V, ID = 3.5A	-	0.8	0.85	$\Omega$

**Dynamic Characteristics**

Ciss	Input Capacitance	VGS =0 V, VDS =25V, f = 1MHz	-	380	-	pF
Coss	Output Capacitance		-	110	-	
Crss	Reverse Transfer Capacitance		-	7	-	

**Dynamic Characteristics**

td(on)	Turn-on Delay Time	VDD =400V, ID =7.0A, RG =25 $\Omega$	-	13	-	nS
tr	Rise Time		-	10	-	
td(off)	Turn-off Delay Time		-	85	-	
tf	Fall Time		-	14	-	
Qg	Total Gate Charge	VDS =640V, VGS =10V, ID =7.0A	-	25	-	nC
Qgs	Gate-Source Charge		-	2.0	-	
Qgd	Gate-Drain Charge(Miller Charge)		-	2.7	-	

**Source-Drain Diode Ratings and Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
IS	Maximum Continuous Drain-Source Diode Forward Current		-	-	7.0	A
ISM	Maximum Pulsed Drain-Source Diode Forward Current		-	-	13	
VSD	Diode Forward Voltage	IS =7.0A, VGS =0V	-	-	1.5	V
trr	Reverse Recovery Time	IS =7.0A, VGS=0V, dIF/dt=100A/us	-	190	-	nS
Qrr	Reverse Recovery Charge		-	2.3	-	uC

**NOTES**

1. Repeatability rating : pulse width limited by junction temperature
2. L =60mH, IAS =1.7A, VDD = 150V, RG = 25 $\Omega$ , Starting TJ = 25°C
3. ISD  $\leq$  7A, di/dt  $\leq$  200A/us, VDD  $\leq$  BVDSS, Starting TJ = 25°C
4. Pulse Test : Pulse Width  $\leq$  300us, Duty Cycle  $\leq$  2%
5. Essentially independent of operating temperature.

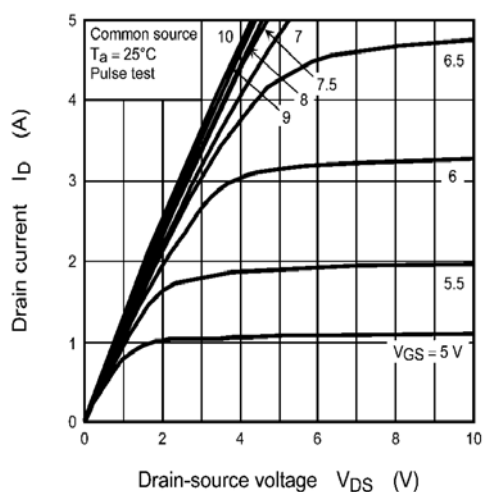


Figure 1: On-Region Characteristics@25°C

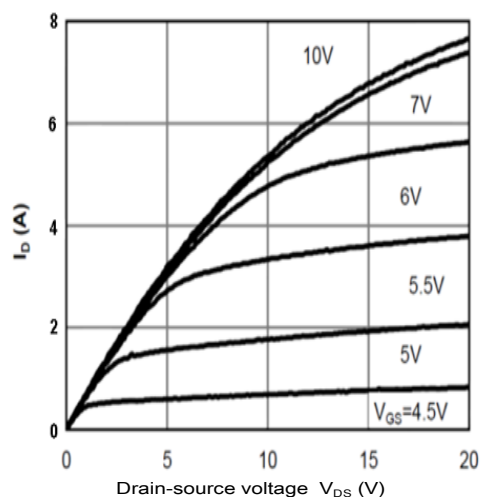


Figure 2: On-Region Characteristics@125°C

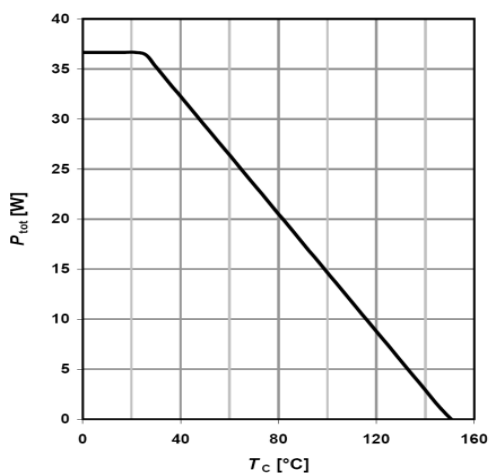


Figure 3: Power Dissipation (TO-220, TO-252)

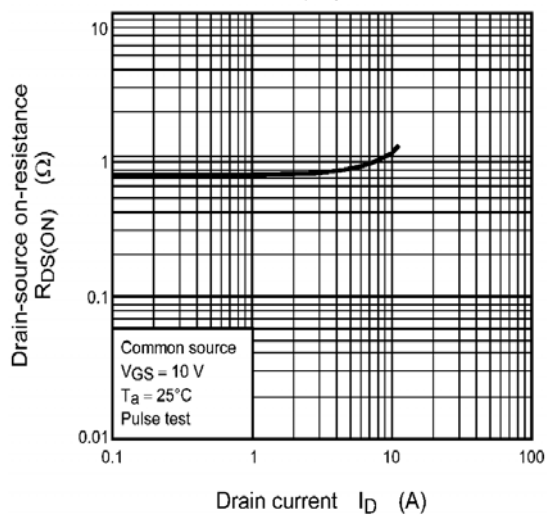


Figure 4: On-Resistance vs. Drain Current

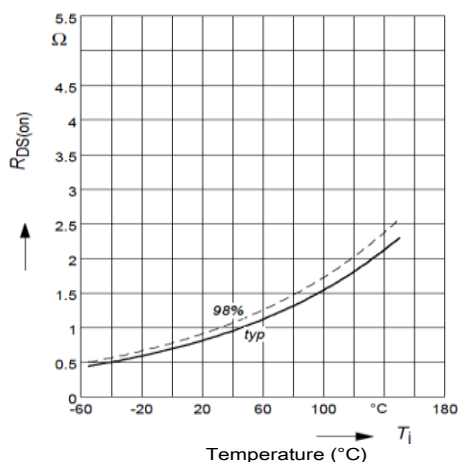


Figure 5: On-Resistance vs. Junction Temperature

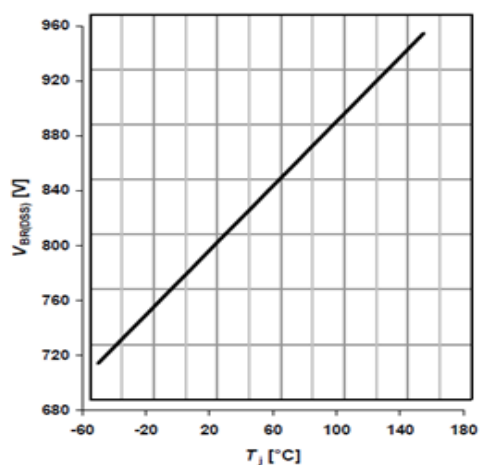


Figure 6: Break Down vs. Junction Temperature

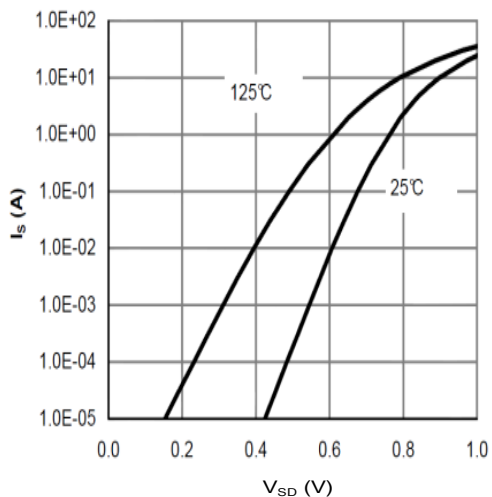


Figure 7: Body-Diode Characteristics

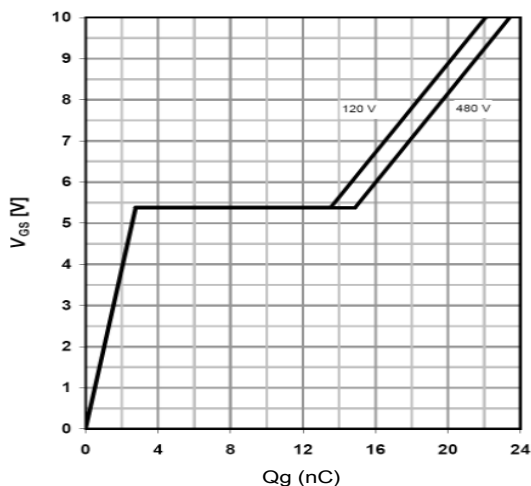


Figure 8: Gate-Charge Characteristics

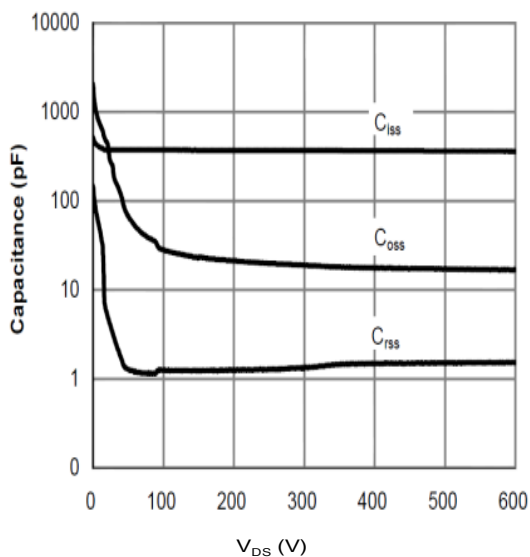


Figure 9: Capacitance Characteristics

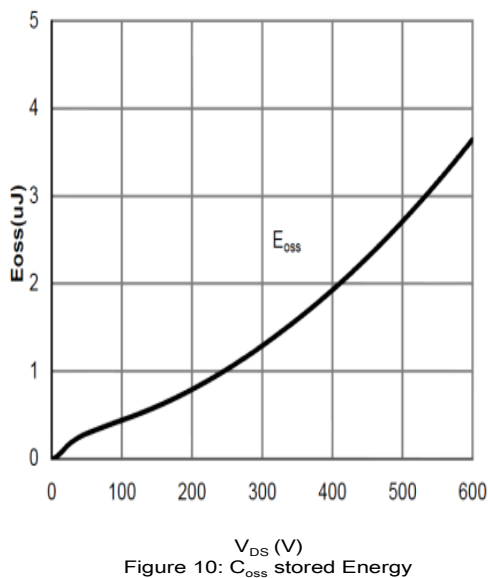


Figure 10:  $C_{oss}$  stored Energy

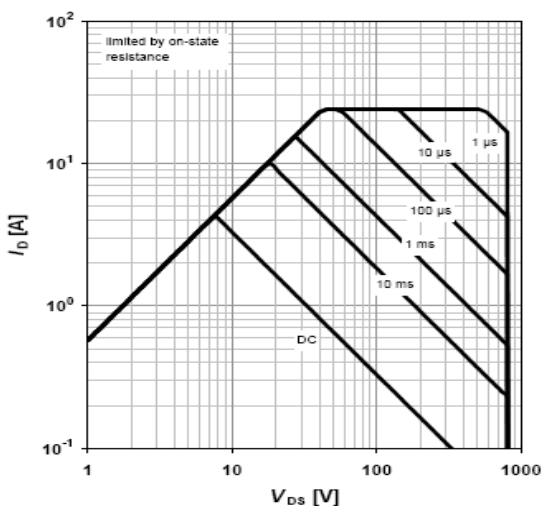


Figure 11: Maximum Forward Biased Safe Operating Area

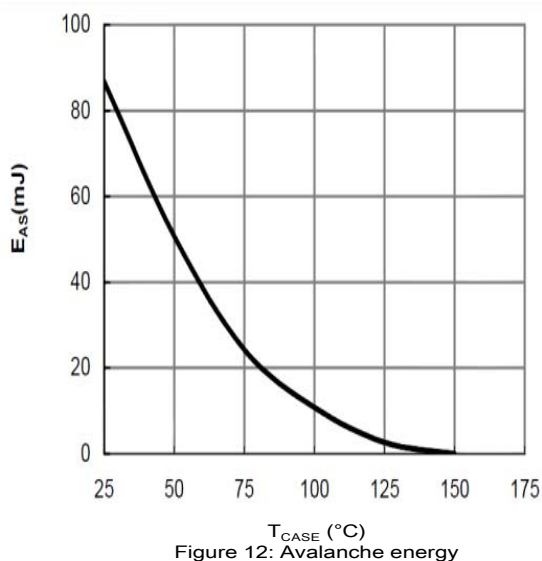
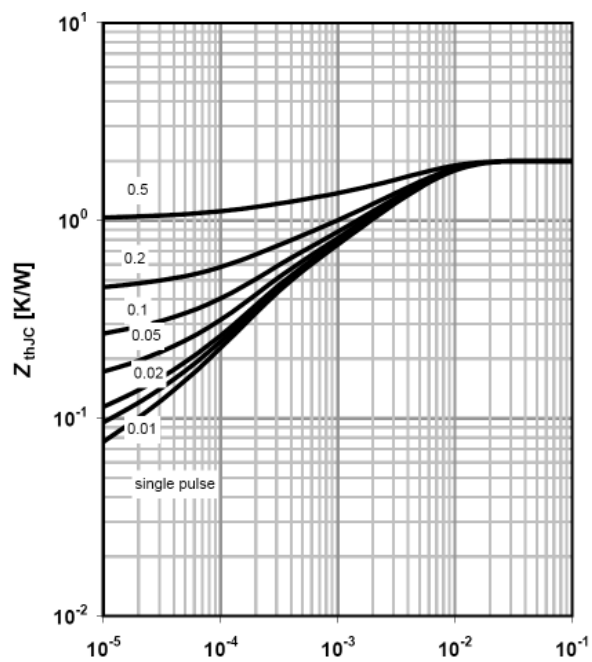
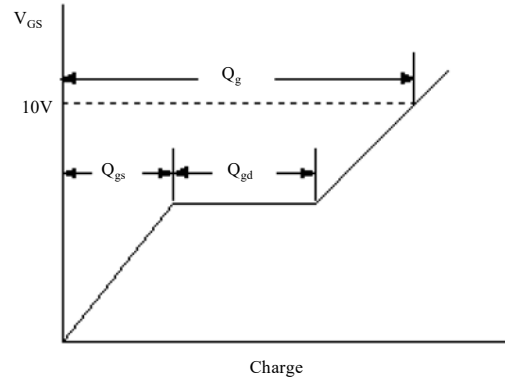
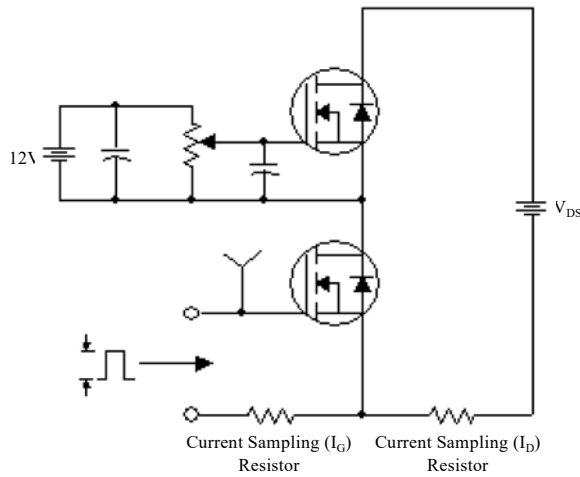


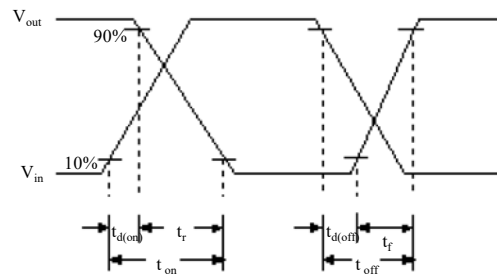
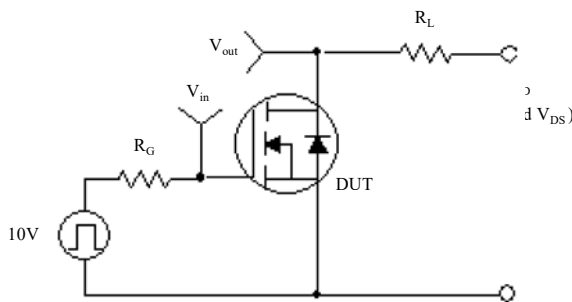
Figure 12: Avalanche energy



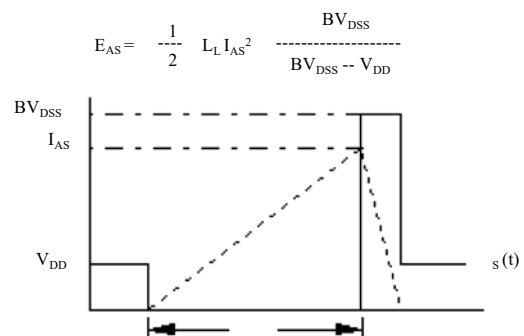
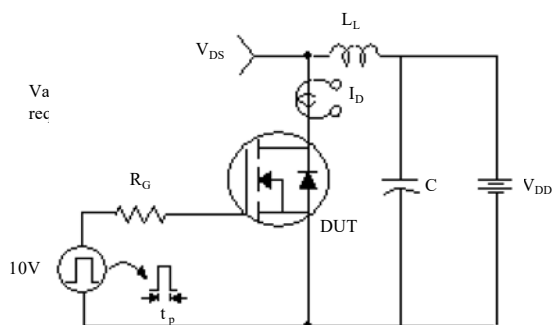
### Gate Charge Test Circuit & Waveform



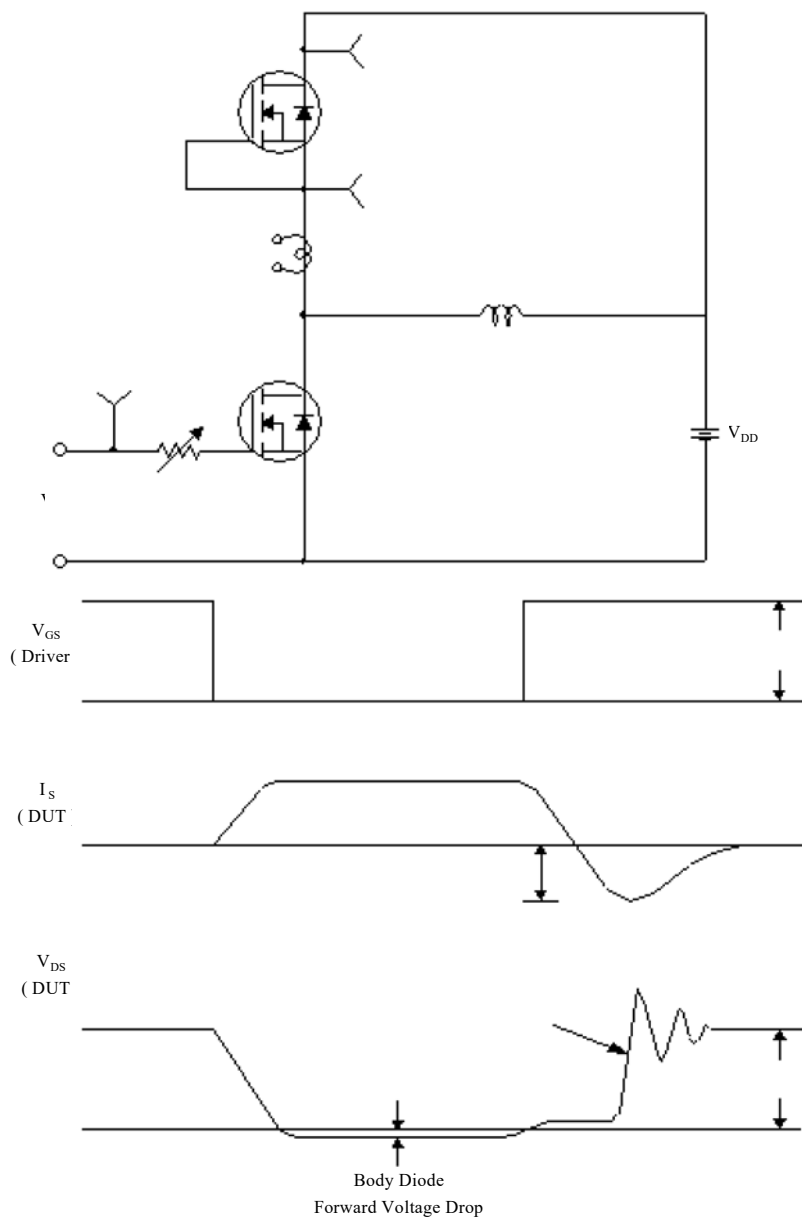
### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



### Peak Diode Recovery dv/dt Test Circuit & Waveforms



单击下面可查看定价，库存，交付和生命周期等信息

[>>Maplesemi\(美浦森半导体\)](#)