

## Features

- Split Gate Trench MOSFET Technology
- Excellent Package for Heat Dissipation
- High Density Cell Design for Low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Halogen Free. "Green" Device (Note 1)
- Epoxy Meets UL 94 V-0 Flammability Rating
- Lead Free Finish/RoHS Compliant ("P" Suffix Designates RoHS Compliant. See Ordering Information)

## Maximum Ratings

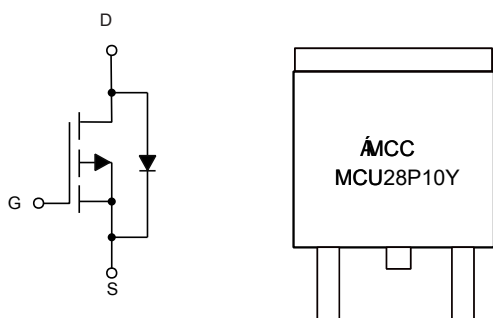
- Operating Junction Temperature Range : -55°C to +150°C
- Storage Temperature Range: -55°C to +150°C
- Thermal Resistance: 20°C/W Junction to Ambient( $t \leq 10s$ ) (Note 2)
- Thermal Resistance: 55°C/W Junction to Ambient(Steady-State) (Note 2)
- Thermal Resistance: 1.3°C/W Junction to Case(Steady-State)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	-100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	-28	A
Pulsed Drain Current (Note 3)	$I_{DM}$	-112	A
Total Power Dissipation (Note 4)	$P_D$	96	W
Single Pulsed Avalanche Energy (Note 5)	$E_{AS}$	220	mJ

Note:

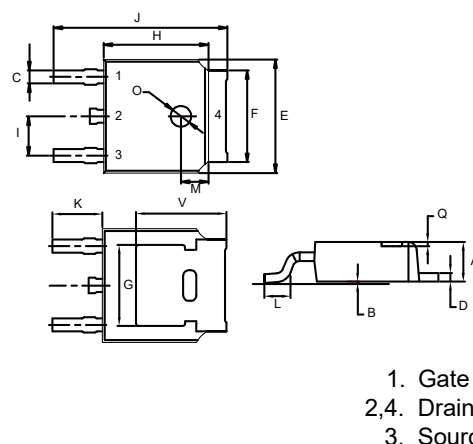
1. Halogen free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
2. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ C$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA} \ t \leq 10s$  and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Repetitive rating; pulse width limited by max. junction temperature.
4.  $P_D$  is based on max. junction temperature, using junction-case thermal resistance.
5.  $V_{DD}=50V$ ,  $R_G=25\Omega$ ,  $L=1mH$ ,  $I_{AS}=31A$ .

## Internal Structure and Marking Code



## P-CHANNEL MOSFET

### DPAK(TO-252)



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.087	0.094	2.20	2.40	
B	0.000	0.005	0.00	0.13	
C	0.026	0.034	0.66	0.86	
D	0.018	0.023	0.46	0.58	
E	0.256	0.264	6.50	6.70	
F	0.201	0.215	5.10	5.46	
G	0.190		4.83		TYP.
H	0.236	0.244	6.00	6.20	
I	0.086	0.094	2.18	2.39	
J	0.386	0.409	9.80	10.40	
K	0.114		2.90		TYP.
L	0.055	0.067	1.40	1.70	
M	0.063		1.60		TYP.
O	0.043	0.051	1.10	1.30	
Q	0.000	0.012	0.00	0.30	
V	0.211		5.35		TYP.

**Electrical Characteristics @ 25°C (Unless Otherwise Specified)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-100			V
Gate-Source Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-100V, V_{GS}=0V$			-1	$\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-15A$		42	58	m $\Omega$
		$V_{GS}=-4.5V, I_D=-7A$		46	65	
<b>Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$				-28	A
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S=-20A$			-1.3	V
Reverse Recovery Time	$t_{rr}$	$I_S=-5A, di_f/dt=100A/\mu s$		104		ns
Reverse Recovery Charge	$Q_{rr}$			280		nC
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=-50V, V_{GS}=0V, f=1MHz$		2100		pF
Output Capacitance	$C_{oss}$			236		
Reverse Transfer Capacitance	$C_{rss}$			48		
Total Gate Charge	$Q_g$	$V_{DS}=-50V, V_{GS}=-10V, I_D=-5A$		40		nC
Gate-Source Charge	$Q_{gs}$			7.8		
Gate-Drain Charge	$Q_{gd}$			8.6		
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-50V, V_{GEN}=-10V, R_G=6\Omega, I_{DS}=-5A$		13		ns
Turn-On Rise Time	$t_r$			39		
Turn-Off Delay Time	$t_{d(off)}$			100.1		
Turn-Off Fall Time	$t_f$			105.3		

**Curve Characteristics**

Fig. 1 - Typical Output Characteristics

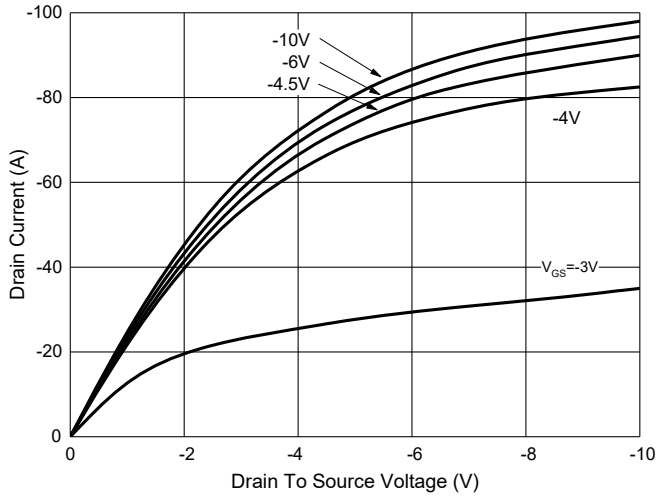


Fig. 2 - Transfer Characteristics

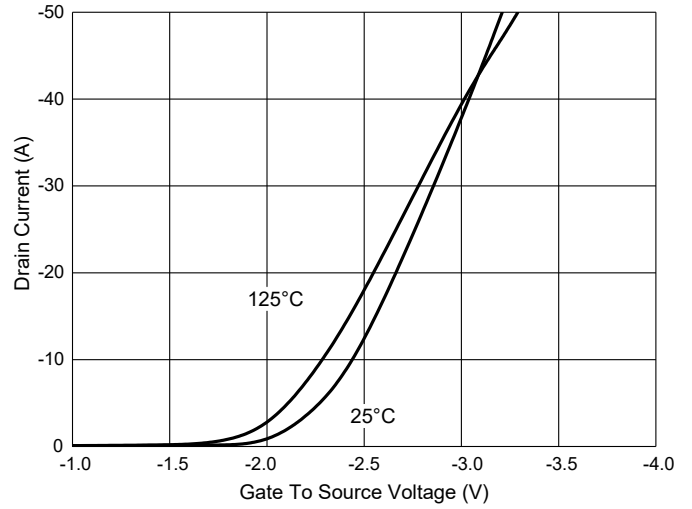


Fig. 3 -  $R_{DS(ON)} - I_D$

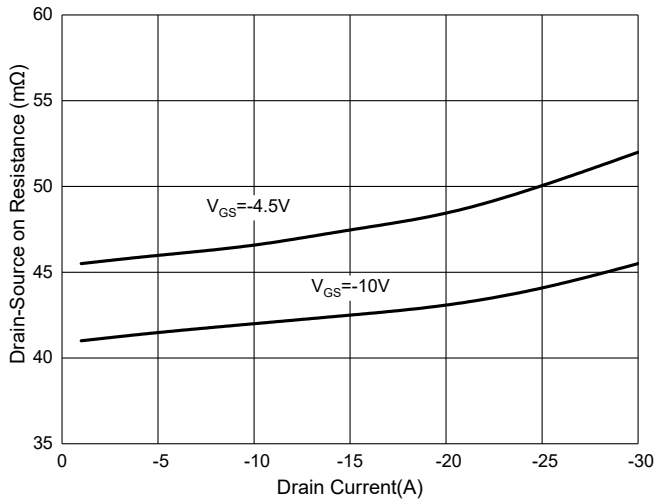


Fig. 4 - Normalized On Resistance Characteristics

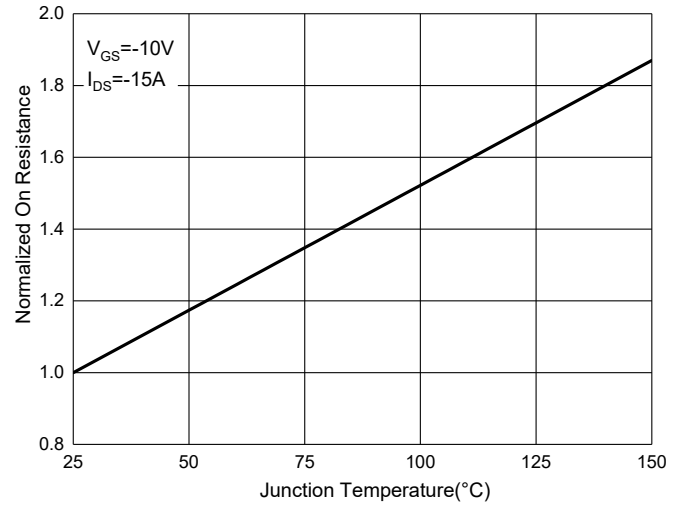


Fig. 5 -  $R_{DS(ON)} - V_{GS}$

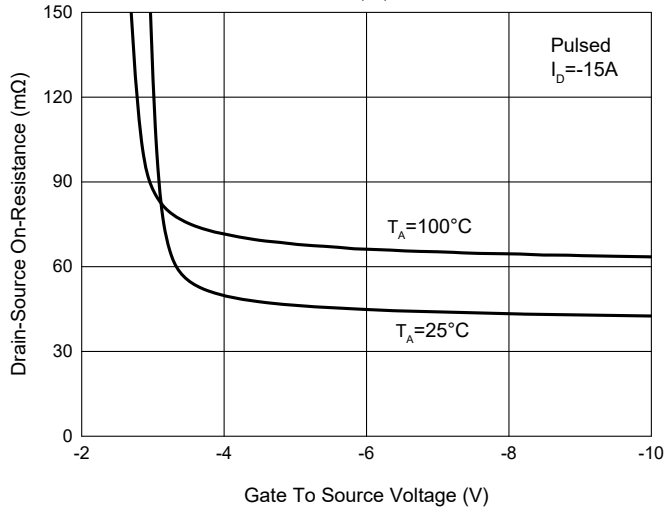
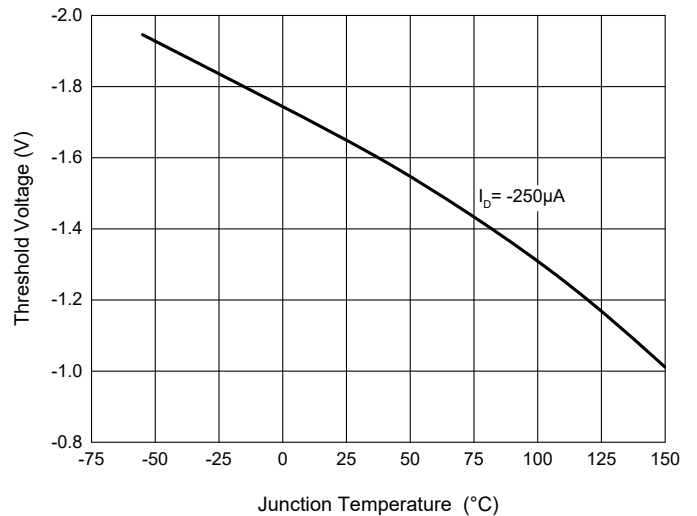


Fig. 6 - Threshold Voltage



**Curve Characteristics**

Fig. 7 - Capacitance Characteristics

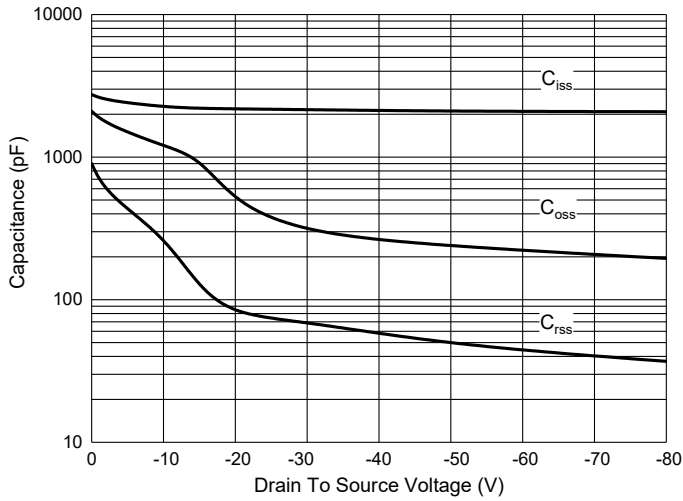


Fig. 8 - Gate Charge

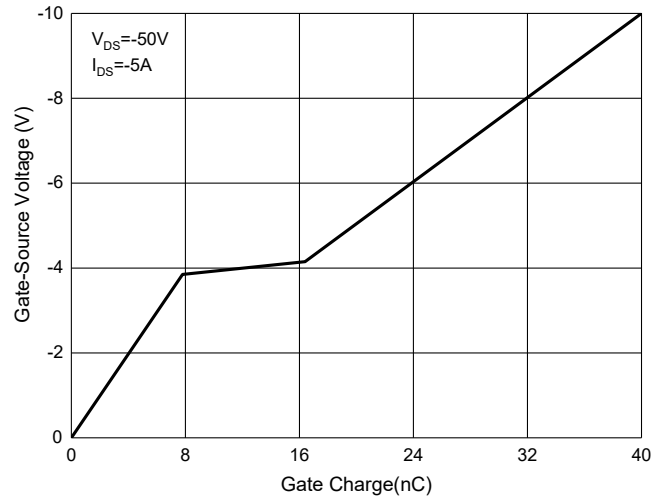


Fig. 9 - Safe Operation Area

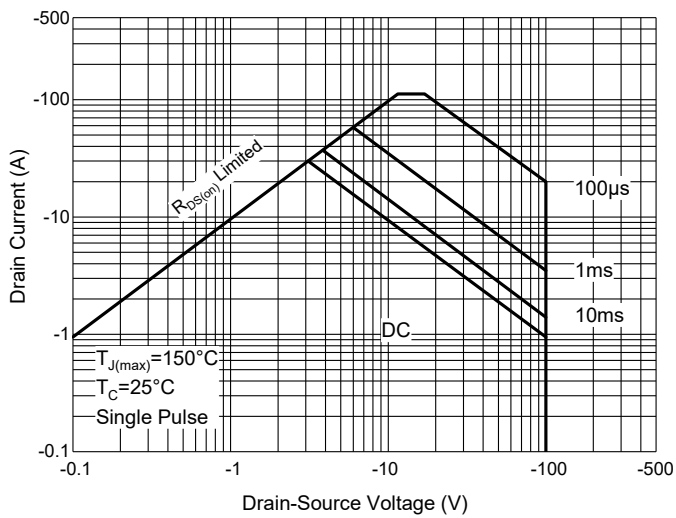


Fig. 10 -  $P_D - T_C$

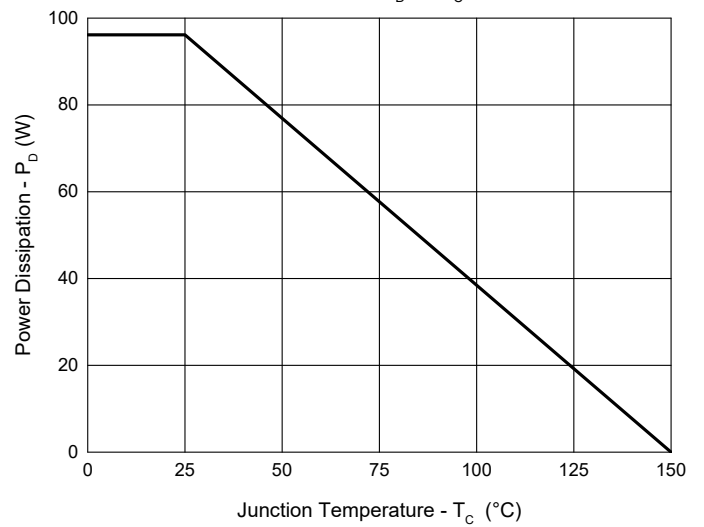
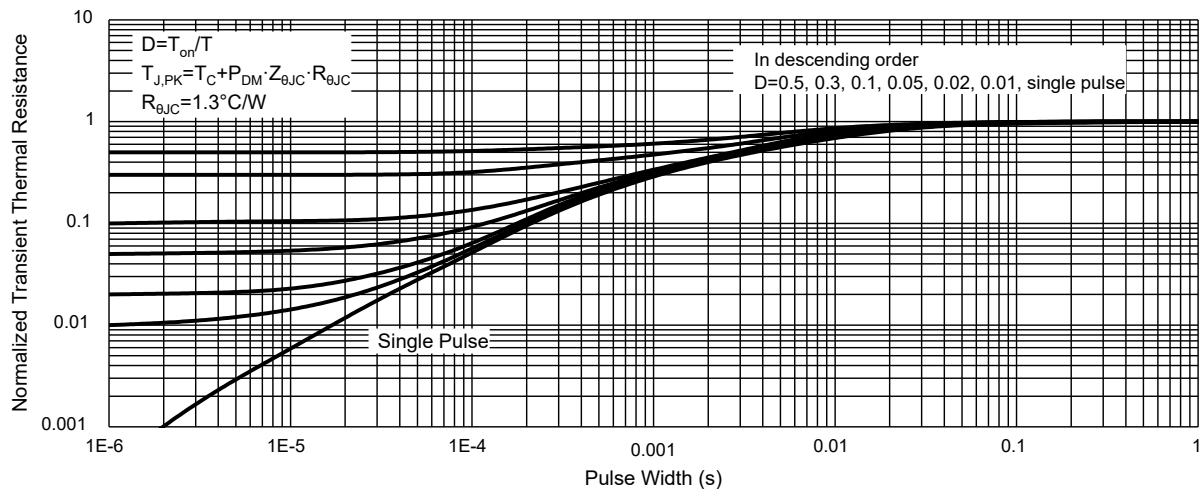


Fig. 11 - Normalized Transient Thermal Impedance



## Ordering Information

Device	Packing
Part Number-TP	Tape&Reel: 2.5Kpcs/Reel

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