1. 功能描述

- MCTDA408/MCTDA410/MCTDA412 系列为 4 通道 8/10/12 比特数模转换器
- 内部带输出电压驱动器
- 内部集成低功耗高速 3 线 SPI 接口

2. 芯片特点

- 2.5V-5.5V 供电
- 全系列产品保证全码单调性
- MCTDA408 积分非线性为±0.625LSB
- MCTDA410 积分非线性为±2.5LSB
- MCTDA412 积分非线性为±10LSB
- 3V 供电下功耗低至 120uA/通道
- 5V 供电下功耗低至 150uA/通道
- 芯片关断模式下功耗低至 200nA
- 参考电压支持 0 到 VDD
- 上电复位初始值为 0
- 片上集成轨到轨输出驱动器（1nF 负载稳定）
- 工作温度支持-40° 至+105°

3. 应用领域

- 工业控制信号产生
- 数字控制增益应用
- 数字控制直流偏差应用
- 数字电位器应用
- 可编程电压控制应用
- 可编程电流控制应用

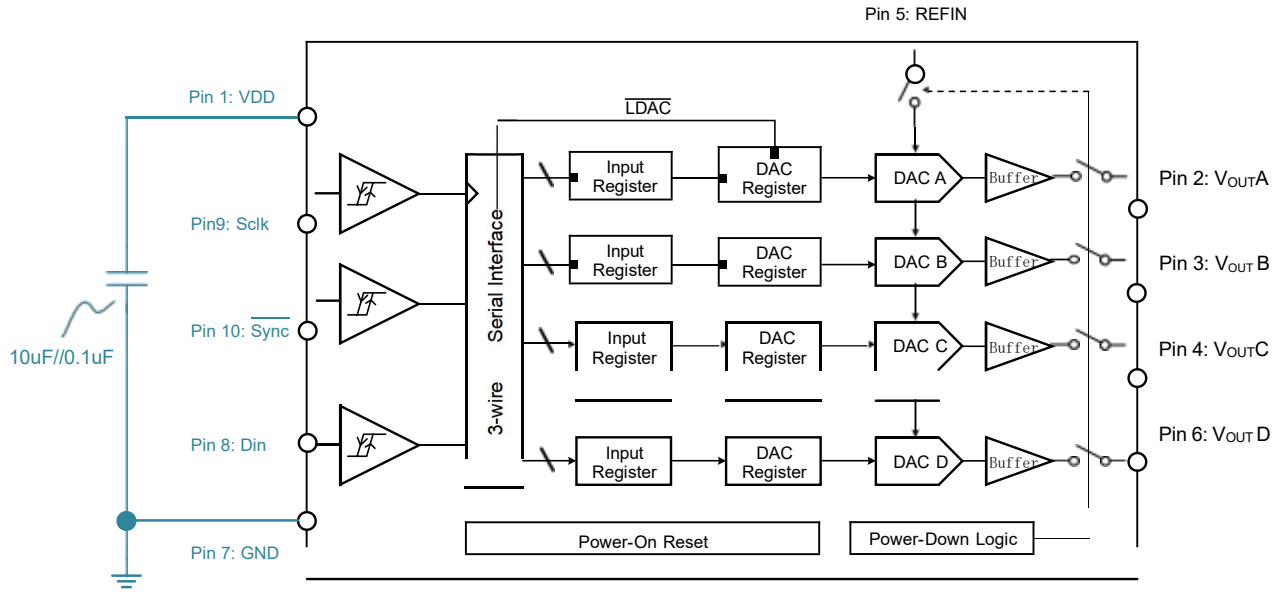
4. 器件选型指南

产品型号	功能定义
MCTDA408	4 通道，8 比特数模转换器
MCTDA410	4 通道，10 比特数模转换器
MCTDA412	4 通道，12 比特数模转换器

5. 器件封装信息

产品型号	封装形式	封装体尺寸
MCTDA408	MSOP-10L	3mm×3mm
MCTDA410	MSOP-10L	3mm×3mm
MCTDA412	MSOP-10L	3mm×3mm
MCTDA412	DFN-10L	3mm×3mm

6. 芯片功能框图



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7. 绝对工作条件

TA=25°C, unless otherwise noted.

电参数 [1]	电气符号	参数值
VDD to GND	VDDabs	-0.3V to+7V
Digital Input Voltage to GND	VDigabs	-0.3V to VDD+0.3V
Reference Input Voltage to GND	Vrefabs	-0.3V to VDD+0.30.3V
VOUTA through VOUTD to GND	Voutabs	-0.3V to VDD+0.30.3V
Operating Temperature Range Industrial Storage Temperature Range Junction Temperature TJmax	 TP TS TJmax	 -40°C to +105°C -65°C to +150°C 150C
Reflow Soldering Peak Temperature (Pb-free) Peak Temperature (non Pb-free) Time at Peak Temperature		 260°C 220°C 10 sec to 40 sec

1. Transient currents of up to 100mA do not cause SCR latch-up.

8. 推荐工作条件

电参数	电气符号	参数值		单位
		最小值	最大值	
供电电压	V_{DD}	2.5	5.5	V
供电电流	I_{DD}	400	600	μA
环境温度	T_a	-40	105	° C

9. 芯片静态特性参数

V_{DD}=2.5V to 5.5V; V_{REF}=2V; R_L=2KΩ to GND; C_L=200pF to GND; T_a=25°C; unless otherwise noted.

电参数	电气符号	测试条件	参数值			单位
			最小	典型	最大	
DC Performance[1,2] MCTDA408						
Resolution	Res_N			8		Bits
Relative Accuracy	INL			±0.125		LSB
Differential Nonlinearity	DNL	Monotonic Guaranteed		±0.05		LSB
DC Performance[1,2] MCTDA410						
Resolution	Res_N			10		Bits
Relative Accuracy	INL			±0.5		LSB
Differential Nonlinearity	DNL	Monotonic Guaranteed		±0.05		LSB
MCTDA412						
Resolution	Res_N			12		Bits
Relative Accuracy	INL			±2		LSB
Differential Nonlinearity	DNL	Monotonic Guaranteed		±0.2		LSB
Offset Error				±0.4		%of FSR
Gain Error				±0.15		%of FSR
Lower Dead Band		Lower dead band exists only if offset error is negative		20		mV
DC Power Supply Rejection Ratio[3]	PSRR	ΔV_{DD} = ±10%		-60		dB
DC Crosstalk[3]		R_L = 2KΩ to GND or VDD		200		μV
Reference Input[3]						
V_{REF} Input Range			0.25		V_{DD}	V
V_{REF} Input Impedance				45		KΩ
Reference Feedthrough		Frequency=10KHz		-80		dB
Output Characteristics[3]						
Minimum Output Voltage[4]				0		V
Maximum Output Voltage[4]				V_{DD}		V
DC Output Impedance				0.5		Ω
Short Circuit Current				25		mA
Power-Up Time				5		μS
Logic Input[3]						
Input Low Voltage	V_{IL}	V_{DD}=3V			0.6	V
Input High Voltage	V_{IH}	V_{DD}=3V			2.1	V

电参数	电气符号	测试条件	参数值			单位
			最小	典型	最大	
Pin Capacitance				3		pF
Power Requirements						
Power supply	V_{DD}		2.5		5.5	V
I_{DD} (Normal Mode)[4]						
V_{DD}=4.5V to 5.5V	I_{DD}	$V_{IH}=V_{DD}$ and V_{IL}=GND		600		μA
V_{REF} =2.5V to 3.6V		$V_{IH}=V_{DD}$ and V_{IL}=GND		500		μA
I_{DD} (Power-Down Mode)						
V_{DD} =4.5V to 5.5V		$V_{IH}=V_{DD}$ and V_{IL}=GND		0.2		μA
V_{DD} =2.5V to 3.6V		$V_{IH}=V_{DD}$ and V_{IL}=GND		0.08		μA

1 DC specifications tested with outputs unloaded.

2 Linearity is tested using a reduced code range: MCTDA408(Code 7 to Code 249); MCTDA410(Code 28 to Code 995); MCTDA412(Code 115 to Code 3981).

3 Guaranteed by design and characterization, not production tested.

4 For the amplifier output to reach its minimum voltage, offset error must be negative. For amplifier output to reach its maximum voltage, V_{REF} = V_{DD} and offset plus gain error must be positive.

5 I_{DD} specification is valid for all DAC codes; interface inactive; all DACs active; load currents excluded.

10. 芯片动态特性参数

V_{DD}=2.5V to 5.5V; V_{REF}=2V; R_L=2KΩ to GND; C_L=200pF to GND; T_a=25°C; unless otherwise noted.

电参数 [1]	电气符号	测试条件	参数值			单位
			最小	典型	最大	
Output Voltage Setting Time		1/4 scale to 3/4 scale change		8		μS
Slew Rate				0.7		V/μS
Major-Code Transition Glitch Energy		1 LSB change around major carry		40		nV-sec
Digital Feedthrough				1		nV-sec
Digital Crosstalk				1		nV-sec
DAC-to-DAC Crosstalk				3		nV-sec
Multiplying Bandwidth		V_{REF} = 2V± 0.1V_{p-p}		200		kHz
Total Harmonic Distortion		V_{REF} = 2.5V± 0.1V_{p-p} Frequency = 10 KHz		-70		dB

1 Guaranteed by design and characterization, not production tested.

11. 芯片管脚定义

11.1 管脚分布图

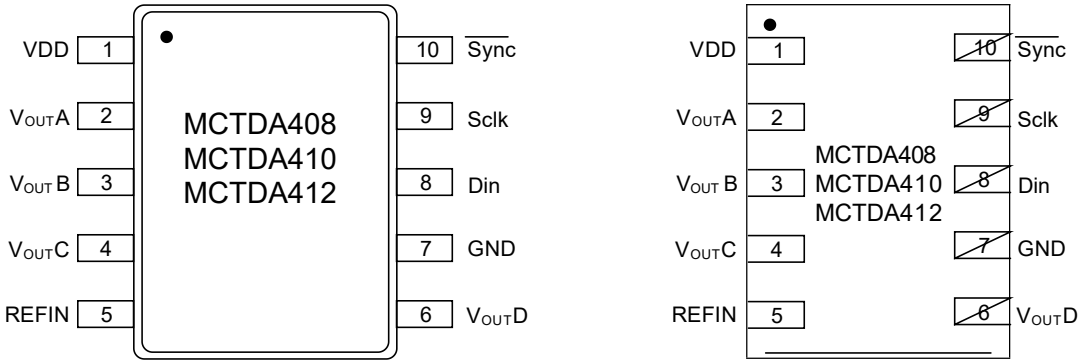

Figure 1: MSOP10L 和 DFN10L Pin Configuration

11.2 管脚功能描述

管脚名称	管脚编号	管脚功能	详细描述
VDD	1	Power	Power Supply Input. These parts can be operated from 2.5V to 5.5V and the supply can be decoupled to GND.
VOUTA	2	O	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
VOUTB	3	O	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
VOUTC	4	O	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
REFIN	5	I	Reference Input Pin for All Four DACs. It has an input range from 0.25V to VDD
VOUTD	6	O	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
GND	7	Ground	Ground Reference Point for All Circuitry on the Part.
Din	8	I	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input. The Din input buffer is powered down after each write cycle.
SCLK	9	I	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at clock speeds up to 30MHz. The SCLK input buffer is powered down after each write cycle.
SYNCb	10	I	Active Low Control Input. This is the frame synchronization signal for the input data. When SYNCb goes low, it enables the input shift register and data is transferred in on the falling edges of the following 16clocks. If SYNCb is taken high before the 16th falling edge of SCLK, the rising edge of SYNCb acts as an interrupt and the write sequence is ignored by the device.

- I：Input, O：Output

12. 芯片工作原理

12.1 原理描述

The MCTDA408/MCTDA410/MCTDA412 are quad, resistor-string DACs fabricated in a CMOS process with resolutions of 8bit,10bit and 12bit, respectively. Each contains four output buffer amplifiers and is written via a 3-wire serial interface. They operate from a single supply of 2.5V to 5.5V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/us. The four DACs share a single reference input pin. The devices have programmable power-down modes, in which all DACs can be turned off completely with a high impedance output.

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the REFIN pin provides the reference voltage for the DAC. The input coding to the DAC is straight binary.

There is a single reference input pin for the four DACs. The reference input is not buffered. The user can have a reference voltage as low as 0.25V or as high as VDD because there is no restriction due to the headroom or footroom requirements of any reference amplifier. It is recommended to use a buffered reference in the external circuit. The input impedance is 45kQ typical.
The output buffer amplifier is capable of generating rail-to-rail output voltages, giving an output range of 0V to VDD when the reference is VDD. It is capable of driving a load of 2kQ to GND or VDD, in parallel with 500pF to GND or VDD. The slew rate is 0.7V/μs with half-scale settling time to ± 0.5LSB (at 12 bits) of 8 μs.

The MCTDA408/MCTDA410/MCTDA412 are provided with power-on reset, so that they power up in a defined state. The power-on state uses normal operation and the output voltage is set to 0V. Both input and DAC registers are filled with zeros and remain so until a valid write sequence is entered to the device.

The MCTDA410/MCTDA412 are controlled over a versatile, 3-wire serial interface that operates at clock rates up to 30MHz and are compatible with SPI, QSPI, MICROWIRE, and DSP interface standards.

12.2 编程接口

12.2.1 可写寄存器描述

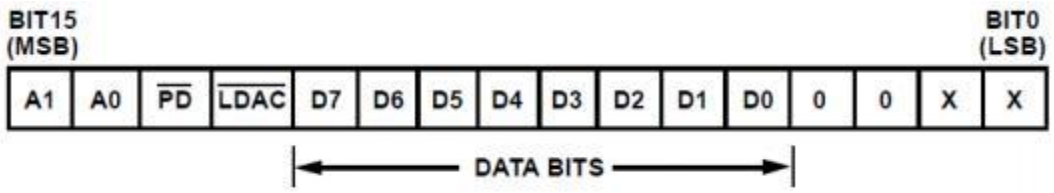

Figure 2: MCTDA408 Input Shift Register Contents

Figure 3: MCTDA410 Input Shift Register Contents

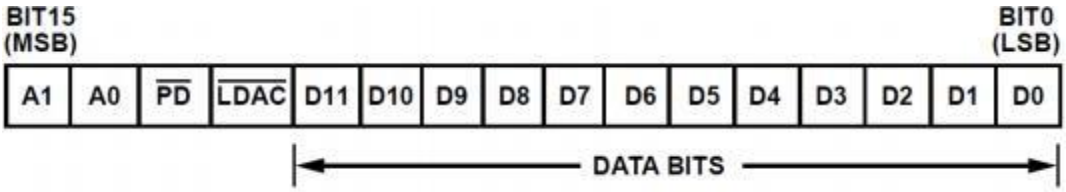

Figure 4: MCTDA412 Input Shift Register Contents

The input shift register is 16 bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The 16-bit word consists of four control bits followed by 10 or 12 bits of DAC data, depending on the device type. Data is loaded MSB first (Bit15) and the first two bits determine whether the data is for DAC A, DAC B, DAC C, or DCA D. Bit 13 and Bit 12 control the operating mode of the DAC. Bit13 is PDb, and determines whether the part is in normal or power-down mode. Bit12 is LDACb, and controls when DAC registers and outputs are updated.

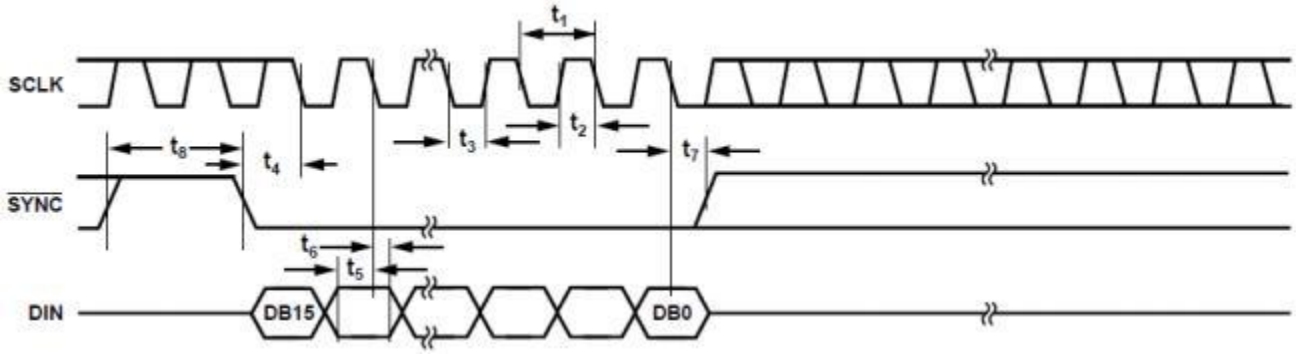

Figure 5: SPI Timing Diagram

Table 1: SPI Timing Constraint

Parameter	Limit	Unit	Test Conditions
t1	40	nS min	SCLK cycle time
t2	16	nS min	SCLK high time
t3	16	nS min	SCLK low time
t4	16	nS min	SYNCb to SCLK falling edge setup time
t5	5	nS min	Data setup time
t6	4.5	nS min	Data hold time
t7	0	nS min	SCLK falling edge to SYNCb rising time
t8	80	nS min	Minimum SYNCb high time

Table 2: Address Bits

A1	**A0**	**DAC Addressed**
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

Control Bits

PDb:

0: All four DACs go into power-down mode, consuming only 200nA @ 5V. The DAC outputs enter a high impedance state.

1: Normal operation.

LDACb:

0: All four DAC registers and, therefore, all DAC outputs updated simultaneously on completion of the write sequence.

1: Only addressed input register is updated. There is no change in the content of the DAC registers.

13. 芯片外观尺寸图

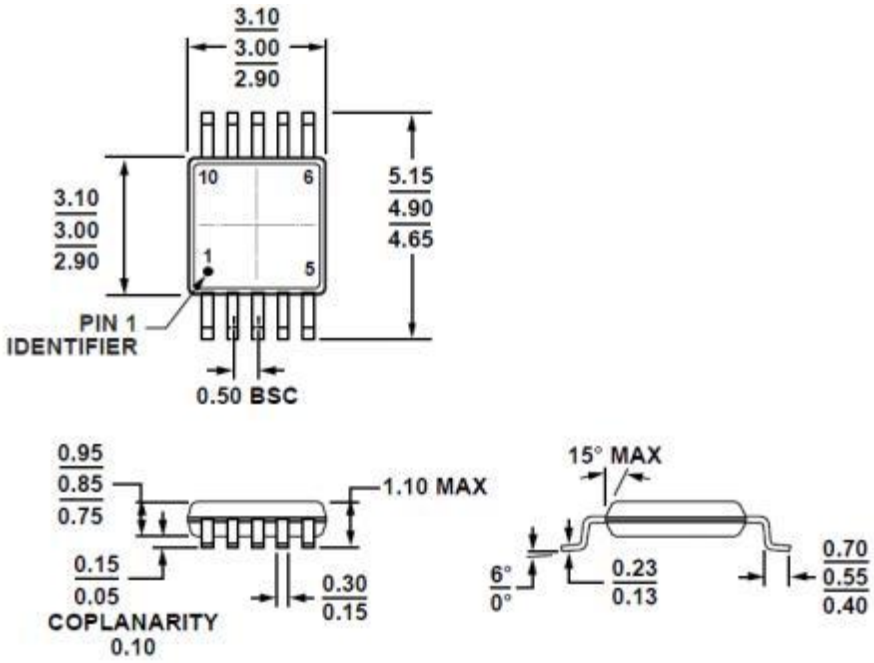

Figure 6: MSOP10L Dimensions shown in millimeters

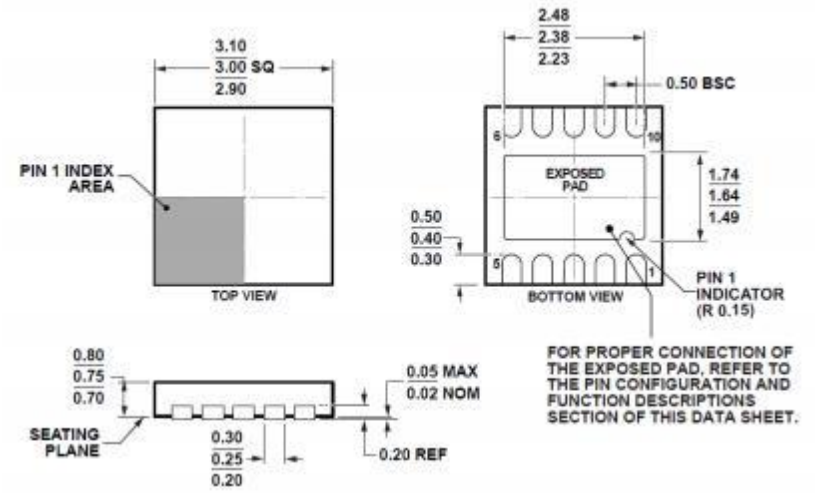

Figure 7: DFN10L Dimensions shown in millimeters

该集成电路可能会被ESD损坏。我们建议在处理所有集成电路时采取适当的预防措施。不遵守正确的处理和安装程序会导致损坏。ESD损害的范围从细微的性能下降到完全的器件故障。精密集成电路可能更容易损坏，因为非常小的参数变化都可能导致器件不符合其公布的规格。