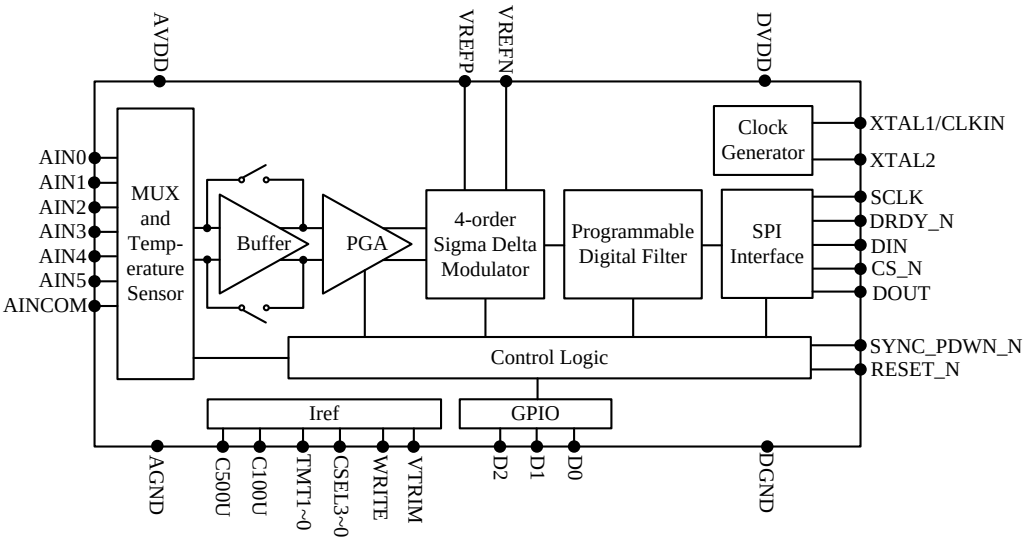
Features Description

- **24 Bits, No Missing Codes**
- **Up to 22 Bits Noise-Free Resolution**
- **±0.002% Nonlinearity**
- **Data Output Rates to 15kSPS**
- **Fast Channel Cycling**
- **One-Shot Conversions with Single-Cycle**
- **Flexible Input Multiplexer**
  −Three Differential Inputs
  −Six Single-Ended Inputs
- **Low-Noise PGA: 30nV Input-Referred Noise**
- **Chopper-Stabilized Input Buffer**
- **Self and System Calibration for All PGA Settings**
- **SPI™-Compatible Serial Interface**
- **Analog Supply: 5V, Digital Supply: 1.8-3.3V**
- **Power Dissipation**
  −As Low as 45mW in Normal Mode
  −0.45mW in Standby Mode

Applications

- **Industrial Process Control**
- **Scientific Instrumentation**
- **Medical Equipment**
- **Test and Measurement**
- **Weigh Scales**

The CP1266 is a high-accuracy data converter chip, with extremely low-noise 24-bit analog-to-digital (A/D) converters and a high-accuracy current source. It provides complete high-resolution measurement solutions for the most demanding applications. The A/D is comprised of a 4th-order, delta-sigma (ΔΣ) modulator followed by a programmable digital filter. The selectable input buffer greatly increases the input impedance and the low-noise programmable gain amplifier (PGA) provides gains from 1 to 64 in binary steps. The programmable filter allows the user to optimize between a resolution of up to 22 bits noise-free and a data rate of up to 15k samples per second (SPS).The converters offer fast channel cycling for measuring multiplexed inputs and can also perform one-shot conversions that settle in just a single cycle. Communication is handled over an SPI-compatible serial interface that can operate with a 2-wire connection. Onboard calibration supports both self and system correction of offset and gain errors for all the PGA settings. A programmable clock output driver is provided for general use. The CP1266 is packaged in an QFN40L.



ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1).

	CP1266	UNIT
AVDD to AGND	−0.3 to +6	V
DVDD to DGND	−0.3 to +3.6	V
AGND to DGND	−0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog inputs to AGND	−0.3 to AVDD + 0.3	V
Digital inputs	−0.3 to DVDD + 0.3	V
Operating Temperature Range	−55 to +105	℃
Storage Temperature Range	−60 to +150	℃
Lead Temperature (soldering, 10s)	+300	℃

(1)Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. We recommend that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at −40°C to +85°C, AVDD = +5V, DVDD = +1.8V, f_{CLKIN}= 7.68MHz, PGA = 1, and VREF= +2.5V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Inputs					
Full-scale input voltage (AIN_P −AIN_N)			±2V_{REF}/PGA		V
Absolute input voltage (AIN0-7, AINCOM to AGND)	Buffer off	AGND −0.1		AVDD + 0.1	V
	Buffer on	AGND + 0.1		AVDD −2.0	V
Programmable gain amplifier		1		64	
Differential input impedance	Buffer off, PGA=1,2,4,8,16		130/PGA		KΩ
	Buffer off, PGA=32,64		5		KΩ
	Buffer on		70		MΩ
System Performance					
Resolution		24			Bit
No missing codes	All data rates and PGA settings	24			Bit
Data rate	f_{CLKIN}= 7.68MHz	2.5		15,000	SPS(1)
Integral nonlinearity	Differential input, PGA = 1		±0.001		%FSR(2)
	Differential input, PGA = 64		±0.002		%FSR
Offset error	After calibration		On the level of the noise		
Offset drift	PGA = 1		±110		nV/°C
	PGA = 64		±5		nV/°C
Gain error	After calibration, PGA = 1, Buffer on		±0.005		%
	After calibration, PGA = 64, Buffer on		±0.03		%
Gain drift	PGA = 1 to 64		±1		ppm/°C
Common-mode rejection			105		dB
Noise			See Noise Performance Tables		
AVDD power-supply rejection	±5% Δ in AVDD		70		dB
DVDD power-supply rejection	±10% Δ in DVDD		102		dB
Voltage Reference Inputs					
Reference input voltage (V_{REF})	V_{REF} =VREFP −VREFN	0.5	2.5	2.6	V
Negative reference input (VREFN)	Buffer off	AGND −0.1		VREFP −0.5	V
	Buffer on(5)	AGND + 0.5		VREFP −0.5	V
Positive reference input (VREFP)	Buffer off	VREFN + 0.5		AVDD + 0.1	V
	Buffer on(5)	VREFN + 0.5		AVDD −2.0	V
Voltage reference impedance	f_{CLKIN}= 7.68MHz		18		KΩ
Current Reference output					
Reference output value		-4%	500(100)	+4%	uA

ELECTRICAL CHARACTERISTICS (continued)

All specifications at −40°C to +85°C, AVDD = +5V, DVDD = +1.8V, f_{CLKIN}= 7.68MHz, PGA = 1, and VREF= +2.5V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output					
V_{IH}		0.8 DVDD		DVDD	V
V_{IL}		DGND		0.2 DVDD	V
V_{OH}	I_{OH}= 5mA	0.8 DVDD			V
V_{OL}	I_{OL}= 5mA			0.2 DVDD	V
Input hysteresis			0.5		V
Input leakage	0 < $V_{DIGITAL\ INPUT}$< DVDD			±10	μA
Master clock rate	External crystal between XTAL1 and XTAL2	2	7.68	8	MHz
	External oscillator driving CLKIN	0.1	7.68	8	MHz
Power-Supply					
AVDD		4.75		5.25	V
DVDD		1.8		3.6	V
AVDD current	Power-down mode		1		μA
	Standby mode		25		μA
	Normal mode, PGA = 1, Buffer off		7		mA
	Normal mode, PGA = 64, Buffer off		16		mA
	Normal mode, PGA = 1, Buffer on		14		mA
	Normal mode, PGA = 64, Buffer on		38		mA
DVDD current	Power-down mode		1		μA
	Standby mode, CLKOUT off, DVDD = 3.3V		100		μA
	Normal mode, CLKOUT off, DVDD = 3.3V		3		mA
Power dissipation	Normal mode, PGA = 1, Buffer off, DVDD = 3.3V		45		mW
	Standby mode, DVDD = 3.3V		0.45		mW
Temperature Range					
Specified		−40		+85	℃
Operating		−55		+105	℃
Storage		−60		+150	℃

(1)SPS = samples per second.

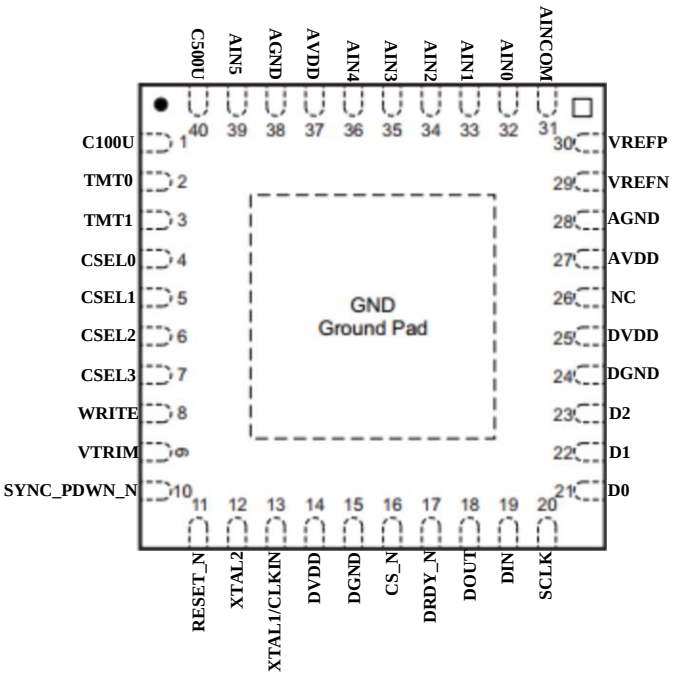
(2) FSR = full-scale range = $4V_{REF}$/PGA.

(3)f_{CM} is the frequency of the common-mode input signal.

(4)Placing a notch of the digital filter at 60Hz (setting f_{DATA}= 60SPS, 30SPS, 15SPS, 10SPS, 5SPS, or 2.5SPS) will further improve the common-mode rejection of this frequency.

(5)The reference input range with Buffer on is restricted only if self-calibration or gain self-calibration is to be used. If using system calibration or writing calibration values directly to the registers, the entire Buffer off range can be used.

PIN ASSIGNMENT QFN40L PACKAGE(TOP VIEW)



Pin Descriptions

Name	Pin NO.	Function	Description
C100U	1	Analog	100uAcurrent output
TMT0	2	Analog	Temperature coefficient adjusting signal
TMT1	3	Analog	Temperature coefficient adjusting signal
CSEL0	4	Analog	Output current adjusting signal
CSEL1	5	Analog	Output current adjusting signal
CSEL2	6	Analog	Output current adjusting signal
CSEL3	7	Analog	Output current adjusting signal
WRITE	8	Analog	Inner OTP write enable , active high
VTRIM	9	Analog	Virtual trimming enable, active high
SYNC_PDWM_N	10	Digital input(1)	Synchronization / power down input, active low
RESET_N	11	Digital input(1)	Reset input, active low
XTAL2	12	Digital(2)	Crystal oscillator connection
XTAL1/CLKIN	13	Digital/Digital input	Crystal oscillator connection / external clock input
DVDD	14	Digital	Digital power supply
DGND	15	Digital	Digital ground
CS_N	16	Digital input(1)	Chip select, active low
DRDY_N	17	Digital output	Data ready output, active low
DOUT	18	Digital output	Serial data output
DIN	19	Digital input(1)	Serial data input
SCLK	20	Digital input(1)	Serial clock input
D0	21	Digital IO	Digital I/O 0, test only, not for custom use.
D1	22	Digital IO	Digital I/O 1, test only, not for custom use.
D2	23	Digital IO	Digital I/O 2, test only, not for custom use.
DGND	24	Digital	Digital ground
DVDD	25	Digital	Digital power supply
NC	26	/	Not Connect

AVDD	27	Analog	Analog power supply
AGND	28	Analog	Analog ground
VREFN	29	Analog input	Negative reference input
VREFP	30	Analog input	Positive reference input
AINCOM	31	Analog input	Analog input common
AIN0	32	Analog input	Analog input 0
AIN1	33	Analog input	Analog input 1
AIN2	34	Analog input	Analog input 2
AIN3	35	Analog input	Analog input3
AIN4	36	Analog input	Analog input 4
AVDD	37	Analog	Analog power supply
AGND	38	Analog	Analog ground
AIN5	39	Analog input	Analog input 5
C500U	40	Analog	500uAcurrent output

(1) Schmitt-Trigger digital input.

(2)Leave disconnected if external clock input is applied to XTAL1/CLKIN.

PARAMETER MEASUREMENT INFORMATION

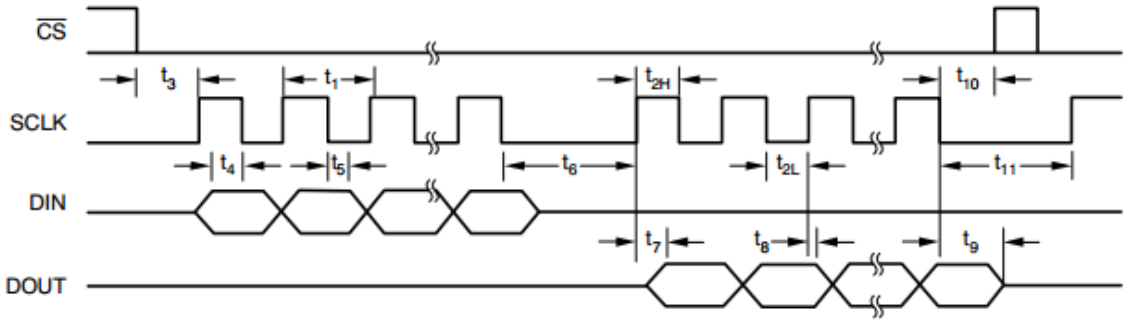


Figure 1. Serial Interface Timing

TIMING CHARACTERISTICS FOR FIGURE 1

SYMBOL	DESCRIPTION		MIN	MAX	UNIT
t_1	SCLK period		4		T_{CLKIN}(1)
				10	T_{DATA}(2)
t_{2H}	SCLK pulse width: high		200		ns
				9	T_{DATA}
t_{2L}	SCLK pulse width: low		200		ns
t_3	CS_N low to first SCLK: setup time(3)		0		ns
t_4	Valid DIN to SCLK falling edge: setup time		50		ns
t_5	Valid DIN to SCLK falling edge: hold time		50		ns
t_6	Delay from last SCLK edge for DIN to first SCLK rising edge for DOUT: RDATA, RDATAC, RREG Commands		50		T_{CLKIN}
t_7	SCLK rising edge to valid new DOUT: propagation delay(4)			50	ns
t_8	SCLK rising edge to DOUT invalid: hold time		0		ns
t_9	Last SCLK falling edge to DOUT high impedance NOTE: DOUT goes high impedance immediately when CS_N goes high		6 10		T_{CLKIN}
t_{10}	CS_N low after final SCLK falling edge		8		T_{CLKIN}
t_{11}	Final SCLK falling edge of command to first SCLK rising edge of next command.	RREG, WREG, RDATA	4		T_{CLKIN}
		RDATAC, SYNC_N	24		T_{CLKIN}
		RDATAC, RESET_N, STANDBY, SELFOCAL, SYSOCAL, SELFGCAL, SYSGCAL, SELFCAL	Wait for DRDY_N to go low		

(1) T_{CLKIN}= master clock period = $1/f_{CLKIN}$.

(2) T_{DATA}= output data period $1/f_{DATA}$.

(3) CS_N can be tied low.

(4) DOUT load = 20pF || 100kΩ to DGND.

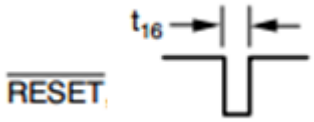


Figure 2. RESET_N Timing

TIMING CHARACTERISTICS FOR FIGURE 2

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{16}	RESET_N pulse width	4		T_{CLKIN}(1)

(1)T_{CLKIN}= master clock period = 1/f_{CLKIN}.

Figure 3. SYNC_PDWN_N Timing

TIMING CHARACTERISTICS FOR FIGURE 3

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{16}	SYNC_PDWN_N , pulse width	4		T_{CLKIN}(1)
t_{16B}	SYNC_PDWN_N rising edge to CLKIN rising edge	-25	25	ns

(1)T_{CLKIN}= master clock period = 1/f_{CLKIN}.

Figure 4. DRDY_N Update Timing

TIMING CHARACTERISTICS FOR FIGURE 4

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{17}	Conversion data invalid while being updated (DRDY_N shown with no data retrieval)	16		T_{CLKIN}(1)

(1) τ_{CLKIN}= master clock period = 1/f_{CLKIN}.

OVERVIEW

The CP1266 is very low-noise A/D converters. It supports three differential or six single-ended inputs.

Figure 5 shows a block diagram of the CP1266. The input multiplexer selects which input pins are connected to the A/D converter. A selectable on board input buffer greatly reduces the input circuitry loading by providing up to 70MΩof impedance. A low-noise PGA provides a gain of 1, 2, 4, 8, 16, 32, or 64. The CP1266 converter is comprised of a 4th-order, delta-sigma modulator followed by a programmable digital filter. The modulator measures the amplified differential input signal, V_{IN}= (AIN_P– AIN_N), against the differential reference, V_{REF}= (VREFP −VREFN). The differential reference is scaled internally by a factor of two so that the full-scale input range is ±2V_{REF}(for PGA = 1).

The digital filter receives the modulator signal and provides a low-noise digital output. The data rate of the filter is programmable from 2.5SPS to 15kSPS and allows tradeoffs between resolution and speed.

Communication is done over an SPI-compatible serial interface with a set of simple commands providing control of the CP1266. Onboard registers store the various settings for the input multiplexer, input buffer enable, PGA setting, data rate, etc. Either an external crystal or clock oscillator can be used to provide the clock source. The device can also offer two accuracy current sources with value of 100uA and 500uA.

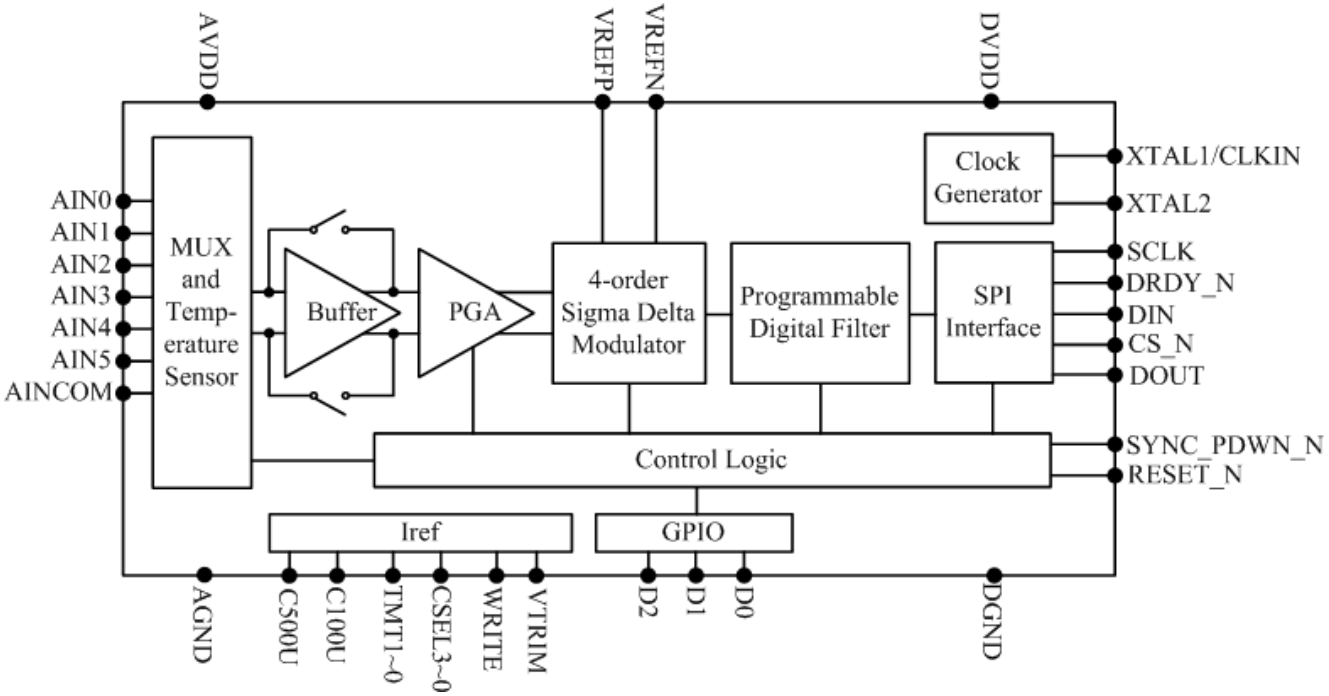


Figure 5. Block Diagram

NOISE PERFORMANCE

The CP1266 offer outstanding noise performance that can be optimized by adjusting the data rate or PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. The PGA reduces the input-referred noise when measuring lower level signals. Table 1 through Table 6 summarize the typical noise performance with the inputs shorted externally. In all six tables, the following conditions apply: T = +25°C, AVDD = 5V, DVDD = 1.8V, V_{REF}= 2.5V, and f_{CLKIN}= 7.68MHz. Table 1 to Table 3 reflect the device input buffer disabled. Table 1 shows the rms value of the input-referred noise in volts. Table 2 shows the effective number of bits of resolution (ENOB), using the noise data from Table 1. ENOB is defined as:

ENOB=ln(FSR/RMS_NOISE)/ln2

where FSR is the full-scale range. Table 3 shows the noise-free bits of resolution. It is calculated with the same formula as ENOB except the peak-to-peak noise value is used instead of rms noise. Table 4 through Table 6 show the same noise data, but with the input buffer enabled.

Table 1. Input Referred Noise (μV, rms) with Buffer Off

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	0.36	0.2	0.16	0.1	0.06	0.04	0.03
5	0.38	0.24	0.17	0.12	0.06	0.05	0.04
10	0.43	0.26	0.18	0.12	0.07	0.06	0.05
15	0.45	0.3	0.18	0.14	0.08	0.07	0.07
25	0.54	0.36	0.2	0.17	0.10	0.08	0.09
30	0.63	0.36	0.25	0.18	0.11	0.09	0.1
50	0.72	0.49	0.3	0.19	0.14	0.11	0.12
60	0.81	0.5	0.36	0.2	0.15	0.13	0.14
100	1.08	0.68	0.52	0.26	0.22	0.2	0.18
500	2.7	1.6	0.9	0.71	0.56	0.49	0.43
1000	3.6	1.9	1.6	1	0.77	0.68	0.78
2000	5.04	3.1	2.2	1.7	1.12	1.1	1.3
3750	10.4	5.1	3.7	2.8	2.2	2.1	1.9
7500	16.3	9.9	5.8	5.2	4.5	3.6	3.2
15,000	18.9	13.1	9.4	6.8	4.8	4.3	4.1

Table 2. Effective Number of Bits (ENOB, rms)with Buffer Off

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	24.7	24.3	24	23.6	23.2	22.8	22.3
5	24.6	24.2	23.9	23.2	23.2	22.7	21.6
10	24.5	24.1	23.8	23.2	23	22.3	21.5
15	24.4	23.8	23.7	23.1	22.8	22.1	21
25	24	23.7	23.4	22.8	22.6	21.8	20.7
30	23.9	23.7	23.2	22.7	22.4	21.7	20.5
50	23.6	23.3	23	22.6	22.1	21.3	20.3
60	23.5	23.2	22.7	22.5	21.9	21.1	20
100	23	22.8	22.2	22.2	21.4	20.7	19.5
500	21.8	21.5	21.4	20.7	20	19.3	18.4
1000	21.4	21.3	20.6	20.2	19.6	18.8	17.6
2000	20.9	20.6	20.1	19.4	19	18.1	16.8
3750	19.8	19.9	19.3	18.7	18.1	17.2	16.3
7500	19.2	18.9	18.7	17.8	17.1	16.4	15.6
15,000	19	18.6	18	17.5	17	16.2	15.2

Table 3. Noise-Free Resolution (bits) with Buffer Off

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	21.9	21.5	21.2	20.8	20.4	20	19.5
5	21.8	21.4	21.1	20.4	20.3	19.9	18.8
10	21.6	21.3	21.0	20.3	20.2	19.5	18.7
15	21.3	21.0	20.9	20.2	20.0	19.3	18.2
25	21.2	20.9	20.6	20.0	19.8	19	17.9
30	21.1	20.8	20.4	19.9	19.6	18.9	17.7
50	20.8	20.5	20.2	19.8	19.3	18.5	17.5
60	20.7	20.4	19.9	19.7	19.1	18.3	17.2
100	20.2	20.0	19.4	19.4	18.6	17.9	16.7
500	19.0	18.7	18.6	17.9	17.2	16.5	15.6
1000	18.6	18.5	17.8	17.4	16.8	16	14.8
2000	18.1	17.8	17.3	16.6	16.2	15.3	14.0
3750	17.0	17.1	16.5	15.9	15.3	14.4	13.5
7500	16.4	16.1	15.9	15.0	14.3	13.6	12.8
15,000	16.2	15.8	15.2	14.7	14.2	13.4	12.4

Table 4. Input Referred Noise (μV, rms) with Buffer On

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	0.38	0.25	0.18	0.11	0.06	0.04	0.04
5	0.39	0.29	0.19	0.13	0.07	0.06	0.05
10	0.44	0.3	0.2	0.14	0.08	0.07	0.06
15	0.46	0.34	0.21	0.15	0.09	0.07	0.08
25	0.56	0.41	0.22	0.17	0.11	0.08	0.1
30	0.64	0.39	0.28	0.19	0.12	0.1	0.11
50	0.74	0.53	0.31	0.2	0.15	0.12	0.13
60	0.84	0.54	0.37	0.23	0.16	0.14	0.14
100	1.1	0.71	0.54	0.29	0.24	0.21	0.19
500	2.73	1.66	0.91	0.78	0.58	0.51	0.46
1000	3.64	1.97	1.63	1.1	0.78	0.7	0.8
2000	5.08	3.16	2.21	1.73	1.15	1.2	1.4
3750	10.5	5.2	3.73	2.9	2.24	2.3	2.0
7500	16.5	10.05	5.82	5.24	4.6	3.7	3.5
15,000	19.4	13.2	9.47	6.85	5.0	4.4	4.2

Table 5. Effective Number of Bits (ENOB, rms)with Buffer On

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	24.6	24.2	23.8	23.5	23.1	22.7	22.2
5	24.5	24.1	23.8	23.2	23	22.6	21.5
10	24.4	24.0	23.7	23.1	22.9	22.2	21.3
15	24.3	23.8	23.6	23	22.7	22	20.8
25	24	23.7	23.4	22.7	22.5	21.7	20.6
30	23.8	23.6	23.1	22.6	22.4	21.6	20.4
50	23.6	23.2	22.9	22.5	22	21.2	20.2
60	23.4	23.1	22.6	22.4	21.9	21	19.8
100	22.8	22.6	22.1	22.1	21.2	20.5	19.4
500	21.7	21.4	21.2	20.5	19.9	19.2	18.1
1000	21.4	21.2	20.5	20.1	19.5	18.6	17.4
2000	20.8	20.4	20	19.3	19	18	16.6
3750	19.6	19.8	19.2	18.6	18	17.1	16.2
7500	19.1	18.7	18.6	17.8	16.9	16.2	15.5
15,000	18.9	18.5	17.9	17.4	16.7	16	15

Table 6. Noise-Free Resolution (bits) with Buffer On

DATA RATE (SPS)	PGA						
	1	2	4	8	16	32	64
2.5	21.8	21.4	21.0	20.7	20.3	19.9	19.4
5	21.7	21.3	21.0	20.4	20.2	19.8	18.7
10	21.6	21.2	20.9	20.3	20.1	19.4	18.5
15	21.5	21.0	20.8	20.2	19.9	19.2	18.0
25	21.2	20.9	20.6	19.9	19.7	18.9	17.8
30	21.0	20.8	20.3	19.8	19.6	18.8	17.6
50	20.8	20.4	20.1	19.7	19.2	18.4	17.4
60	20.6	20.3	19.8	19.6	19.1	18.2	17.0
100	20.0	19.8	19.3	19.3	18.4	17.7	16.6
500	18.9	18.6	18.4	17.7	17.1	16.4	15.3
1000	18.6	18.4	17.7	17.3	16.7	15.8	14.6
2000	18.0	17.6	17.2	16.5	16.2	15.2	13.8
3750	16.8	17.0	16.4	15.8	15.2	14.3	13.4
7500	16.3	15.9	15.8	15.0	14.1	13.4	12.7
15,000	16.1	15.7	15.1	14.6	13.9	13.2	12.2

INPUT MULTIPLEXER

Figure 6 shows a simplified diagram of the input multiplexer. This flexible block allows any analog input pinto be connected to either of the converter differential inputs. That is, any pin can be selected as the positive input (AIN_P); likewise, any pin can be selected as the negative input (AIN_N). The pin selection is controlled by the multiplexer register.

The CP1266 offers seven analog inputs, which can be configured as three independent differential inputs, six single-ended inputs, or a combination of differential and single-ended inputs.

In general, there are no restrictions on input pin selection. However, for optimum analog performance, the following recommendations are made:

1. For differential measurements use AIN0 through AIN5, preferably adjacent inputs. For example, use AIN0 and AIN1. Do not use AINCOM.
2. For single-ended measurements use AINCOM as common input and AIN0 through AIN5 as single-ended inputs.
3. Leave any unused analog inputs floating. This minimizes the input leakage current.

ESD diodes protect the analog inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below AGND by more than 100mV, and likewise do not exceed AVDD by more than 100mV.

When using CP1266 for single-ended measurements, it is important to note that common input AINCOM does not need to be tied to ground. For example, AINCOM can be tied to a midpoint reference such as +2.5V or even AVDD.

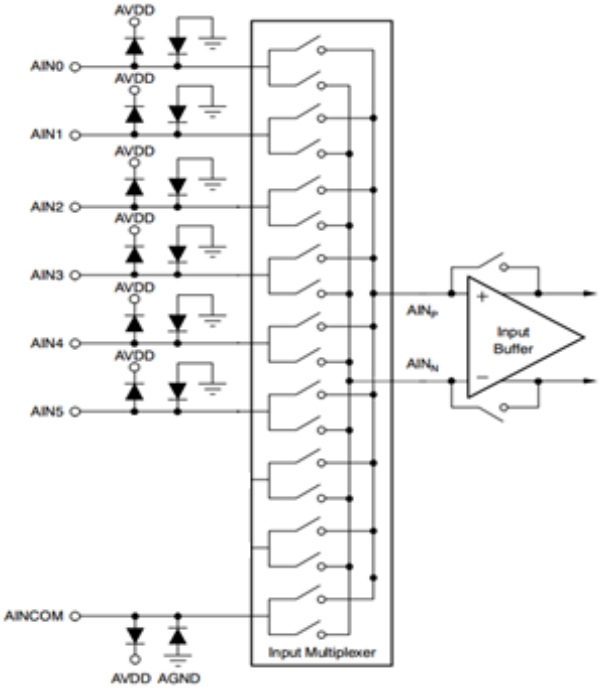


Figure 6. Simplified Diagram of the Input Multiplexer

ANALOG INPUT BUFFER

To dramatically increase the input impedance presented by the CP1266, the low-drift chopper-stabilized buffer can be enabled. The input impedance with the buffer enabled can be modeled by a resistor, as shown in Figure 8. Table 7 lists the values of Zeff for the different data rate settings. The input impedance scales inversely with the frequency of CLKIN. For example, if f_{clkin} is reduced by half to 3.84MHz, Zeff for a data rate of 50SPS will double from 70MΩto 140MΩ.

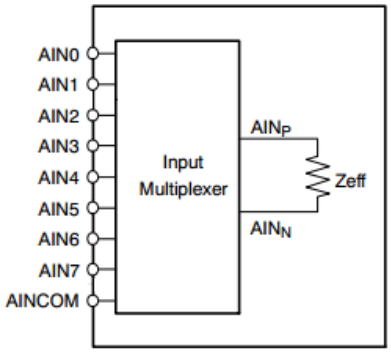


Figure 8. Effective Impedance with Buffer On

Table 7. Input Impedance with Buffer On

DATA RATE (SPS)	Zeff (MΩ)
≤50	70
60	40
100	40
500	40
1000	20
2000	10
3750	10
7500	10
15,000	10

NOTE: f_{CLKIN}= 7.68MHz.

With the buffer enabled, the voltage on the analog input swith respect to ground (listed in the Electrical Characteristics as Absolute Input Voltage) must remain between AGND+0.5 and AVDD −2.0V. Exceeding this range reduces performance, in particular the linearity of the CP1266. This same voltage range, AGND+0.5 toAVDD−2.0V, applies to the reference inputs when performing a self gain calibration with the buffer enabled.

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The CP1266 is a very high resolution converter. To further complement its performance, the low-noise PGA provides even more resolution when measuring smaller input signals. For the best resolution, set the PGA to the highest possible setting. This will depend on the largest input signal to be measured. The CP1266 full-scale input voltage equals $\pm 2V_{REF}/PGA$. Table 8 shows the full-scale input voltage for the different PGA settings for V_{REF} = 2.5V. For example, if the largest signal to be measured is 1.0V, the optimum PGA setting would be 4, which gives a full-scale input voltage of 1.25V. Higher PGAs can not be used since they cannot handle a 1.0V input signal.

Table 8. Full-Scale Input Voltage vs PGA Setting

PGA SETTING	FULL-SCALE INPUT VOLTAGE VIN(1) (V_{REF}= 2.5V)
1	±5V
2	±2.5V
4	±1.25V
8	±0.625V
16	±312.5mV
32	±156.25mV
64	±78.125mV

(1) The input voltage is the difference between the positive and negative inputs. Make sure neither input violates the absolute input voltage with respect to ground, as listed in the Electrical Characteristics. The PGA is controlled by the ADCON register. Recalibrating the A/D converter after changing the PGA setting is recommended. The time required for self-calibration is dependent on the PGA setting. See the Calibration section for more details. The analog current and input impedance (when the buffer is disabled) vary as a function of PGA setting.

MODULATOR INPUT CIRCUITRY

The CP1266 modulator measures the input signal using internal capacitors that are continuously charged and discharged. Figure 9 shows a simplified schematic of the CP1266 input circuitry with the input buffer disabled. Figure 10 shows the on/off timings of the switches of Figure 9. S1 switches close during the input sampling phase. With S1 closed, C_{A1} charges to AIN_P, C_{A2} charges to AIN_N, and C_B charges to (AIN_P–AIN_N). For the discharge phase, S1 opens first and then S2 closes. C_{A1} and C_{A2} discharge to approximately AVDD/2 and C_B discharges to 0V. This two-phase sample/discharge cycle repeats with a period of τ_{SAMPLE}. This time is a function of the PGA setting as shown in Table 9 along with the values of the capacitor C_{A1}= C_{A2} = C_A and C_B.

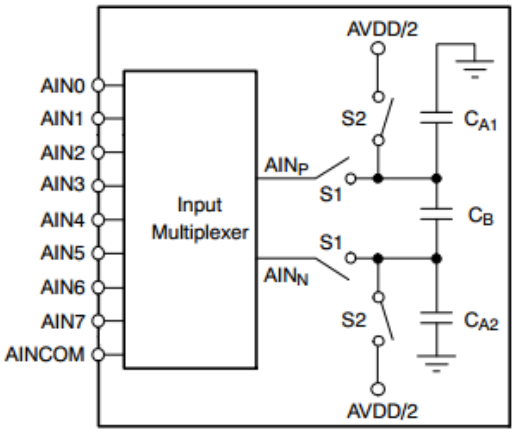


Figure 9. Simplified Input Structure with Buffer Off

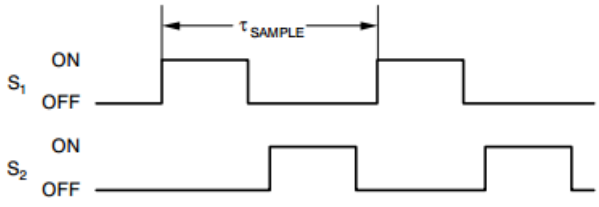


Figure 10. S1 and S2 Switch Timing for Figure 9

Table 9. Input Sampling Time, t_{SAMPLE}[1], and C_A and C_B vs PGA

PGA SETTING	t_{SAMPLE}	C_A	C_B
1	$f_{CLKIN}/4$ (260ns)	2.1pF	2.4pF
2	$f_{CLKIN}/4$ (260ns)	4.2pF	4.9pF
4	$f_{CLKIN}/4$ (260ns)	8.3pF	9.7pF
8	$f_{CLKIN}/4$ (260ns)	17pF	19pF
16	$f_{CLKIN}/4$ (260ns)	33pF	39pF
32	$f_{CLKIN}/2$ (260ns)	33pF	39pF
64	$f_{CLKIN}/2$ (260ns)	33pF	39pF

[1] t_{SAMPL} for f_{CLKIN} = 7.68MHz.

The charging of the input capacitors draws a transient current from the sensor driving the CP1266 inputs. The average value of this current can be used to calculate an effective impedance Zeff where Zeff = $V_{IN}/I_{AVERAGE}$. Figure 11 shows the input circuitry with the capacitors and switches of Figure 9 replaced by their effective impedances. These impedances scale inversely with the CLKIN frequency. For example, if f_{CLKIN} is reduced by a factor of two, the impedances will double. They also change with the PGA setting. Table 10 lists the effective impedances with the buffer off for f_{CLKIN}= 7.68MHz.

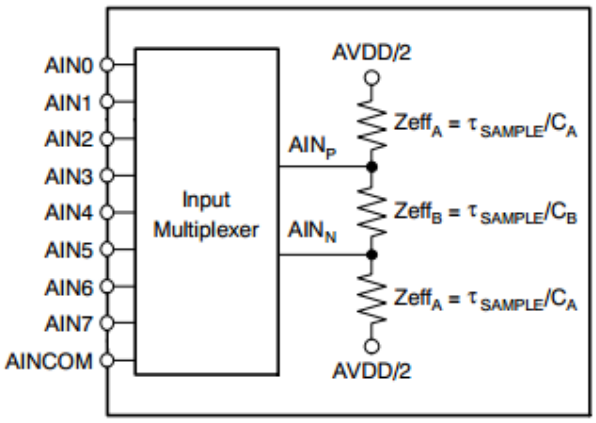


Figure 11. Analog Input Effective Impedances with Buffer Off

Table 10. Analog Input Impedances with Buffer Off

PGA SETTING	$Zeff_A$ (kΩ)	$Zeff_B$ (kΩ)
1	260	220
2	130	110
4	65	55
8	33	28
16	16	14
32	8	7
64	8	7

NOTE: f_{CLKIN}= 7.68MHz.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the CP1266 is the differential voltage between VREFP and VREFN: V_{REF}= VREFP −VREFN. The reference inputs use a structure similar to that of the analog inputs with the circuitry on the reference inputs of Figure 12. The load presented by the switched capacitor can be modeled with an effective impedance (Zeff) of 18kΩ for f_{CLKIN}= 7.68MHz. The temperature coefficient of the effective impedance of the voltage reference inputs is approximately 35ppm/°C.

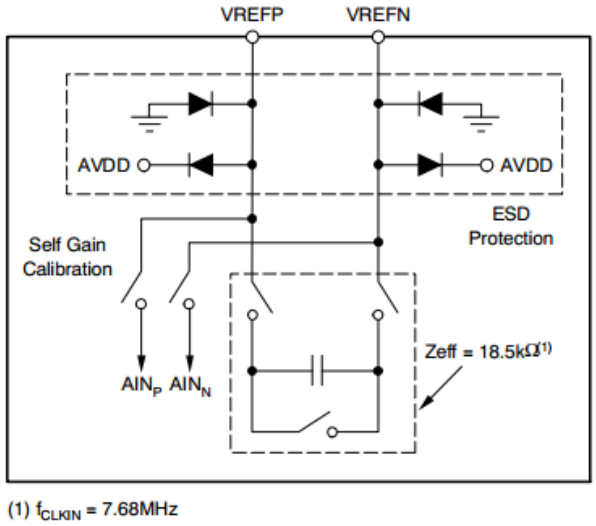


Figure 12. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AGND by more than 100mV, and likewise do not exceed AVDD by 100mV. During self gain calibration, all the switches in the input multiplexer are opened, VREFN is internally connected to AIN_N, and VREFP is connected to AIN_P. The input buffer may be disabled or enabled during calibration. When the buffer is disabled, the reference pins will be driving the circuitry shown in Figure 9 during self gain calibration, resulting in increased loading. To prevent this additional loading from introducing gain errors, make sure the circuitry driving the reference pins has adequate drive capability. When the buffer is enabled, the loading on the reference pins will be much less, but the buffer will limit the allowable voltage range on VREFP and VREFN during self or selfgain calibration as the reference pins must remain within the specified input range of the buffer in order to establish proper gain calibration.

A high-quality reference voltage capable of driving the switched capacitor load presented by the CP1266 is essential for achieving the best performance. Noise and drift on the reference degrade overall system performance. It is especially critical that special care be given to the circuitry generating the reference voltages and their layout when operating in the low-noise settings (that is, with low data rates) to prevent the voltage reference from limiting performance. See the Applications section for more details.

DIGITAL FILTER

The programmable low-pass digital filter receives the modulator output and produces a high-resolution digital output. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate. The filter is comprised of two sections, a fixed filter followed by a programmable filter. Figure 13 shows the block diagram of the analog modulator and digital filter. Data is supplied to the filter from the analog modulator at a rate of $f_{CLKIN}/4$.The fixed filter is a 5th-order sinc filter with a decimation value of 64 that outputs data at a rate of $f_{CLKIN}/256$. The second stage of the filter is a programmable average (1st-order sinc filter) with the number of averages set by the DRATE register. The data rate is a function of the number of averages (Num_Ave) and is given by Equation 1.

$$DataRate = \frac{f_{CLKIN}}{256} \cdot \frac{1}{Num\_Ave} \quad (1)$$

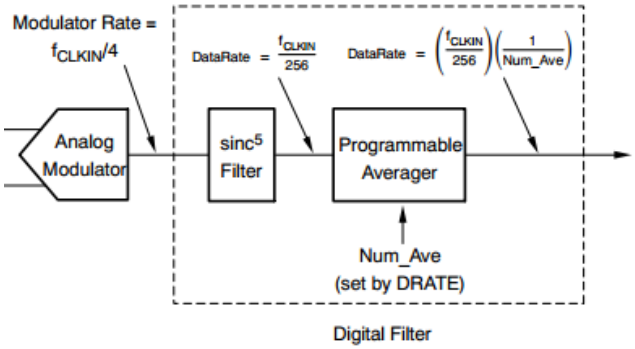


Figure 13. Block Diagram of the Analog Modulator and Digital Filter

Table 11 shows the averaging and corresponding data rate for each of the 16 valid DRATE register settings when f_{CLKIN}= 7.68MHz. Note that the data rate scales directly with the CLKIN frequency. For example, reducing f_{CLKIN} from 7.68MHz to 3.84MHz reduces the data rate for DR[7:0] =0000 0000 from 15,000SPS to 7,500SPS.

Table 11. Number of Averages and Data Rate for Each Valid DRATE Register Setting

DRATEDR[7:0]	NUMBER OF AVERAGES FOR PROGRAMMABLE FILTER(Num_Ave)	DATA RATE(1)(SPS)
00000010	2	15,000
00000011	4	7500
00000100	8	3750
00000101	15	2000
00000110	30	1000
00000111	60	500
00001000	300	100
00001001	500	60
00001010	600	50
00001011	1000	30
00001100	1200	25
00001101	2000	15
00001110	3000	10
00001111	6000	5
00010000	12,000	2.5

(1)for f_{CLKIN}= 7.68MHz.

FREQUENCY RESPONSE

The low-pass digital filter sets the overall frequency response for the CP1266. The filter response is the product of the responses of the fixed and programmable filter sections and is given by Equation 2.

$$|H(f)| = |H_{\sin c^5}(f)| \cdot |H_{Averager}(f)| = \left| \frac{\sin(\frac{256\pi \cdot f}{f_{CLKIN}})}{64 \cdot \sin(\frac{4\pi \cdot f}{f_{CLKIN}})} \right| \cdot \left| \frac{\sin(\frac{256\pi \cdot Num\_Ave \cdot f}{f_{CLKIN}})}{Num\_Ave \cdot \sin(\frac{256\pi \cdot f}{f_{CLKIN}})} \right| \quad (2)$$

The digital filter attenuates noise on the modulator output, including noise from within the CP1266 and external noise present on the

CP1266 input signal. Adjusting the filtering by changing the number of averages used inthe programmable filter changes the filter bandwidth. With a higher number of averages, bandwidth is reduced and more noise is attenuated.

The low-pass filter has notches (or zeros) at the data output rate and multiples thereof. At these frequencies, the filter has zero gain. This feature can be useful when trying to eliminate a particular interference signal. For example, to eliminate 60Hz (and the harmonics) pickup, set the datarate equal to 2.5SPS, 5SPS, 10SPS, 15SPS, 30SPS, or 60SPS. To help illustrate the filter characteristics, Figure 14 and Figure 15 show the responses at the datarate extremes of 15kSPS and 2.5SPS respectively. Table 12 summarizes the first-notch frequency and −3dBbandwidth for the different data rate settings.

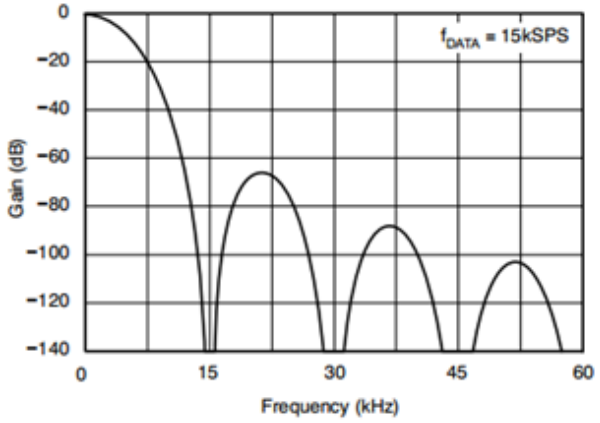


Figure 14. Frequency Response for Data Rate = 15kSPS

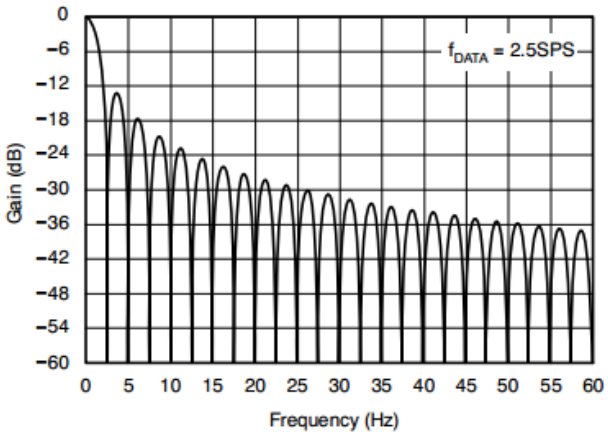


Figure 15. Frequency Response for Data Rate = 2.5SPS

Table 12. First Notch Frequency and −3dB Filter Bandwidth

DATA RATE(SPS)	FIRST NOTCH (Hz)	−3dB BANDWIDTH (Hz)
15,000	15,000	4807
7500	7500	3003
3750	3750	1615
2000	2000	878
1000	1000	441
500	500	221
100	100	44.2
60(1)	60	26.5
50(2)	50	22.1
30(1)	30	13.3
25(2)	25	11.1
15(1)	15	6.63
10(3)	10	4.42
5(3)	5	2.21
2.5(3)	2.5	1.1

NOTE: f_{CLKIN}= 7.68MHz.

(1) Notch at 60Hz.

(2) Notch at 50Hz.

(3) Notch at 50Hz and 60Hz.

The digital filter low-pass characteristic repeats at multiples of the modulator rate of $f_{CLKIN}/4$. Figure 16 and Figure 17 show the responses plotted out to 7.68MHz at the data rate extremes of 15kSPS and 2.5SPS. Notice how the responses near DC, 1.92MHz, 3.84MHz, 5.76MHz, 7.68MHz, are the same. The digital filter will attenuate high-frequency noise on the CP1266 inputs up to the frequency where the

response repeats. If significant noise on the inputs is present above this frequency, make sure to remove with external filtering. Fortunately, this can be done on the CP1266 with a simple RC filter, as shown in the Applications Section (see Figure 25).

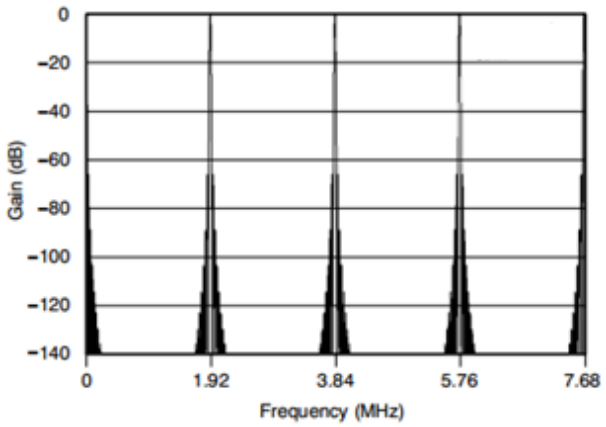


Figure 16. Frequency Response Out to 7.68MHzfor Data Rate = 15kSPS

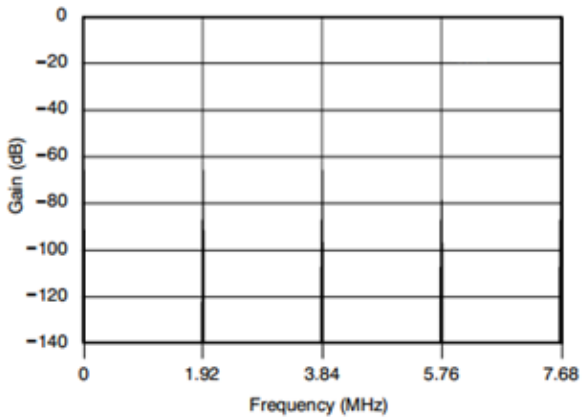


Figure 17. Frequency Response Out to 7.68MHzfor Data Rate = 2.5SPS

SETTLING TIME

The CP1266 features a digital filter optimized for fast settling. The settling time (time required for a step change on the analog inputs to propagate through the filter) for the different data rates is shown in Table 13. The following sections highlight the single-cycle settling ability of the filter and show various ways to control the conversion process.

Table 13. Settling Time vs Data Rate

DATA RATE(SPS)	SETTLING TIME (t_{18})(ms)
15,000	0.25
7500	0.31
3750	0.44
2000	0.68
1000	1.18
500	2.18
100	10.18
60	16.84
50	20.18
30	33.51
25	40.18
15	66.84
10	100.18
5	200.18
2.5	400.18

NOTE: f_{CLKIN}= 7.68MHz.

NOTE: One−shot mode requires a small additional delay to powerup the device from standby.

Settling Time Using Synchronization

The SYNC_PDWN_N pin allows direct control of conversion timing. Simply issue a Sync command or strobe the SYNC_PDWN_N pin after changing the analog inputs (seethe Synchronization section for more information). The conversion begins when SYNC_PDWN_N is taken high, stopping the current conversion and restarting the digital filter. As soon as SYNC_PDWN_N goes low, the DRDY_N output goes high and remains high during the conversion. After the settling time (T_{18}), DRDY_N goes low, indicating that data is available. The CP1266 settles in a single

cycle，there is no need to ignore or discard data after synchronization. Figure 18 shows the data retrieval sequence following synchronization.

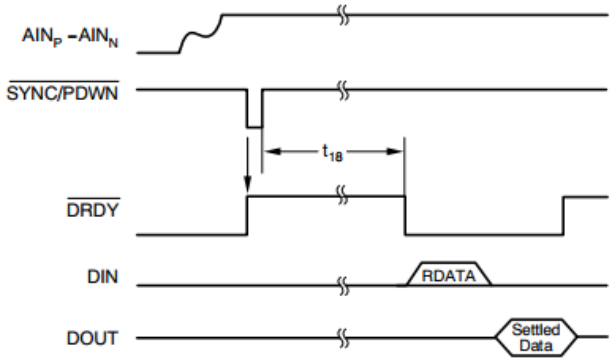


Figure 18. Data Retrieval After Synchronization

Settling Time Using the Input Multiplexer

The most efficient way to cycle through the inputs is to change the multiplexer setting (using a WREG command to the multiplexer register MUX) immediately after DRDY_N goes low. Then, after changing the multiplexer, restart the conversion process by issuing the SYNC and WAKEUP commands, and retrieve the data with the RDATA command. Changing the multiplexer before reading the data allows the CP1266 to start measuring the new input channel sooner. Figure 19 demonstrates efficient input cycling. There is no need to ignore or discard data while cycling through the channels of the input multiplexer because the CP1266 fully settles before DRDY_N goes low, indicating data is ready.

Step 1: When DRDY_N goes low, indicating that data is ready for retrieval, update the multiplexer register MUX using the WREG command. For example, setting MUX to 23h gives AIN_P = AIN2, AIN_N = AIN3.

Step 2: Restart the conversion process by issuing a SYNC command immediately followed by a WAKEUP command. Make sure to follow timing specification t_{11} between commands.

Step 3: Read the data from the previous conversion using the RDATA command.

Step 4: When DRDY_N goes low again, repeat the cycle by first updating the multiplexer register, then reading the previous data.

Table 14 gives the effective overall throughput ($1/t_{19}$) when cycling the input multiplexer. The values for throughput ($1/t_{19}$) assume the multiplexer was changed with a 3-byteWREG command and f_{SCLK}= f_{CLKIN}/4.

Table 14. Multiplexer Cycling Throughput

DATA RATE(SPS)	CYCLING THROUGHPUT ($1/t_{19}$)(Hz)
15,000	3817
7500	3043
3750	2165
2000	1438
1000	837
500	456
100	98
60	59
50	50
30	30
25	25
15	15
10	10
5	5
2.5	2.5

NOTE: f_{CLKIN}= 7.68MHz.

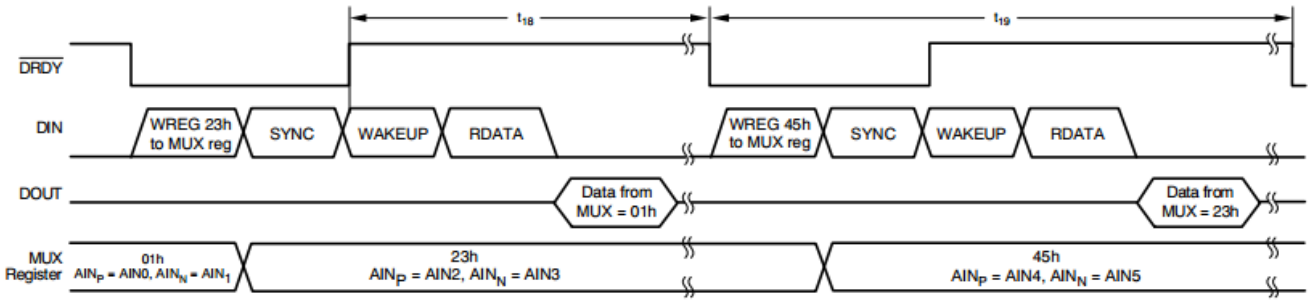


Figure 19. Cycling the CP1266 Input Multiplexer

Settling Time Using One-Shot Mode

A dramatic reduction in power consumption can be achieved in the CP1266 by performing one-shot conversions using the STANDBY command; the sequence for this is shown in Figure 20. Issue the WAKEUP command from Standby mode to begin a one-shot conversion. When using one−shot mode, an additional delay is required for the modulator to power up and settle. This delay may be up to 64 modulator clocks (64 x 4 x τ_{CLKIN}) or 33.3μs for a 7.68MHz master clock. Following the settling time (t_{18} + 256 x τ_{CLKIN}), DRDY_N will go low, indicating that the conversion is complete and data can be read using the RDATA command. TheCP1266 settles in a single cycle—there is no need to ignore or discard data. Following the data read cycle, issue another STANDBY command to reduce power consumption. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

Settling Time while Continuously Converting

After a synchronization, input multiplexer change, or wakeup from Standby mode, the CP1266 will continuously convert the analog input. The conversion is coincide with the falling edge of DRDY_N. While continuously converting, it is often more convenient to consider settling times in terms of DRDY_N periods, as shown in Table 15.The DRDY_N period equals the inverse of the data rate. If there is a step change on the input signal while continuously converting, performing a synchronization operation to start a new conversion is recommended. Otherwise, the next data will represent a combination of the previous and current input signal and should therefore be discarded. Figure 21 shows an example of readback in this situation.

Table 15. Data Settling Delay vs Data Rate

DATA RATE(SPS)	SETTLING TIME (DRDY_N Periods)
15,000	3
7500	2
3750	1
2000	1
1000	1
500	1
100	1
60	1
50	1
30	1
25	1
15	1
10	1
5	1
2.5	1

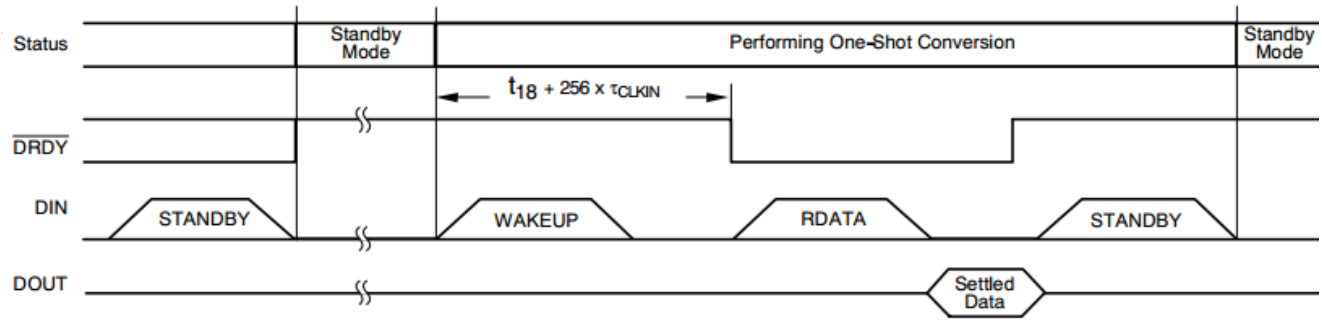


Figure 20. One-Shot Conversions Using the STANDBY Command

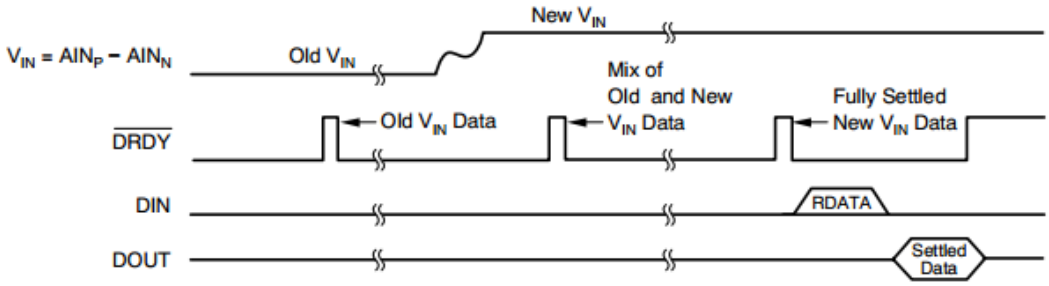


Figure 21. Step Change on V_{IN} while Continuously Converting for Data Rates ⩽3750SPS

DATA FORMAT

The CP1266 output 24 bits of data in Binary true format. The LSB has a weight of $2V_{REF}/(PGA(2^{23}-1))$. Table 16 summarizes the ideal output codes for different input signals.

Table 16. Ideal Output Code vs Input Signal

INPUT SIGNAL VIN(AIN_P −AIN_N)	TRUE FORM(1)
$\geq \frac{+2V_{REF}}{PGA}$	7FFFFFh
$\frac{+2V_{REF}}{PGA}\left(\frac{2^{23}-2}{2^{23}-1}\right)$	7FFFFEh
$\frac{+2V_{REF}}{PGA(2^{23}-1)}$	000001h
0	000000h
$\frac{-2V_{REF}}{PGA(2^{23}-1)}$	800001h
$\frac{-2V_{REF}}{PGA}$	FFFFFFh
$\leq \frac{-2V_{REF}}{PGA}\left(\frac{2^{23}}{2^{23}-1}\right)$	800000h

(1)Ideal output codes excluding effects of noise, INL, offset, and gain errors.

CLOCK GENERATION

The master clock source for the CP1266 can be provided using an external crystal or clock generator. When the clock is generated using crystal, external capacitors must be provided to ensure start-up and as table clock frequency, as shown in Figure 22. Any crystal should work with the CP1266. Table 17 lists two crystals that have been verified to work. Long leads should be minimized with the crystal placed close to theCP1266 pins.

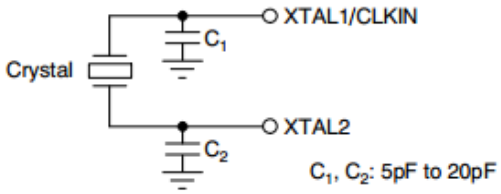


Figure 22. Crystal Connection

Table 17. Sample Crystals

MANUFACTURER	FREQUENCY	PART NUMBER
Citizen	7.68MHz	CIA/53383
ECS	8.0MHz	ECS-80-5-4

When using a crystal, neither the XTAL1/CLKIN nor XTAL2 pins can be used to drive any other logic. If other devices need a clock source, the D0 pin is available for this function. When using an external clock generator, supply the clock signal to XTAL1/CLKIN and leave XTAL2 floating. Make sure the external clock generator supplies a clean clock waveform. Overshoot and glitches on the clock will degrade overall performance.

CALIBRATION

Offset and gain errors can be minimized using the CP1266 onboard calibration circuitry. Figure 23 shows the calibration block diagram. Offset errors are corrected with the Offset Calibration (OFC) register and, likewise, full-scale errors are corrected with the Full-Scale Calibration (FSC) register. Each of these registers is 24-bits and can be read from or written to.

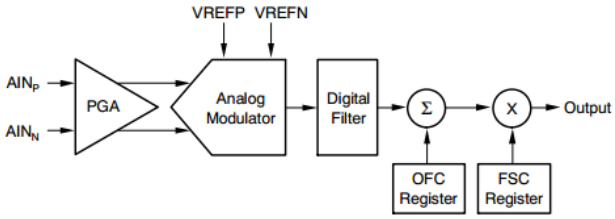


Figure 23. Calibration Block Diagram

The output of the CP1266 after calibration is shown in Equation 3.

Output=(Vin*PGA/(2*VREF)-OFC/α)*FSC*β (3)

where α and β vary with data rate settings shown in Table 18 along with the ideal values (assumes perfect analog performance) for OFC and FSC.

The CP1266 supports both self-calibration and system calibration for any PGA setting using a set of five commands: SELFOCAL, SELFGCAL, SELFCAL, SYSOCAL, and SYSGCAL. Calibration can be done at any time, though in many applications the CP1266driftperformance is low enough that a single calibration is all that is needed. DRDY_N goes high when calibration begins and remains so until settled data is ready afterwards. There is no need to discard data after a calibration. After a reset, the CP1266 performs self-calibration. Calibration must be performed whenever the data rate changes and should be performed when the buffer configuration or PGA changes.

Self-Calibration

Self-calibration corrects internal offset and gain errors. During self-calibration, the appropriate calibration signals are applied internally to the analog inputs. SELFOCAL performs a self offset calibration. The analog inputs AIN_P and AIN_N are disconnected from the signal source and connected to AVDD/2. See Table 19 for the time required for self offset calibration for the different data rate settings. As with most of the CP1266 timings, the calibration time scales directly with f_{CLKIN}. Self offset calibration updates the OFC register.

Table 19. Self Offset and System Offset Calibration Timing

DATA RATE(SPS)	SELF OFFSET CALIBRATION AND SYSTEM OFFSET CALIBRATION TIME
15,000	453µs
7500	587µs
3750	853µs
2000	1.3ms
1000	2.3ms
500	4.3ms
100	20.3ms
60	33.7ms
50	40.3ms
30	67.0ms
25	80.3ms
15	133.7ms
10	200.3ms
5	400.3ms
2.5	800.3ms

NOTE: f_{CLKIN}= 7.68MHz.

SELFGCAL performs a self gain calibration. The analog inputs AIN_P and AIN_N are disconnected from the signal source and AIN_P is connected internally to VREFP while AIN_N is connected to VREFN. Self gain calibration can be used with any PGA setting, and the CP1266 has excellent gain calibration even for the higher PGA settings, as shown in the Typical Characteristics section. Using the buffer will limit the common-mode range of the reference inputs during self gain calibration since they will be connected to the buffer inputs and must be within the specified analog input range. When the voltage on VREFP or VREFN exceeds the buffer analog input range (AVDD – 2.0V), the buffer must be turned off during self gain calibration. Otherwise, use system gain calibration or write the gain coefficients directly to the FSC register. Table 20 shows the time required for self gain calibration for the different data rate and PGA settings. Self gain calibration updates the FSC register.

Table 20. Self Gain Calibration Timing

DATA RATE(SPS)	SELF GAIN CALIBRATION TIME
15,000	484µs
7500	617µs
3750	884µs
2000	1.4ms
1000	2.3ms
500	4.3ms
100	20.3ms
60	33.7ms
50	40.3ms
30	67.0ms
25	80.3ms
15	133.7ms
10	200.3ms
5	400.3ms
2.5	800.3ms

NOTE: f_{CLKIN}= 7.68MHz.

SELFCAL performs first a self offset and then a self gain calibration. The analog inputs are disconnected from the signal source during self-calibration. When using the input buffer with self-calibration, make sure to observe the common-mode range of the reference inputs as described above. Table 21 shows the time required for self-calibration for the different data rate settings. Self-calibration updates both the OFC and FSC registers.

Table 21. Self-Calibration Timing

DATA RATE(SPS)	SELF GAIN CALIBRATION TIME
15,000	696μs
7500	896μs
3750	1.3ms
2000	2.0ms
1000	3.6ms
500	6.6ms
100	31.2ms
60	50.9ms
50	61.8ms
30	101.3ms
25	123.2ms
15	202.1ms
10	307.2ms
5	613.8ms
2.5	1227.2ms

NOTE: f_{CLKIN}= 7.68MHz.

System Calibration

System calibration corrects both internal and external offset and gain errors using the SYSOCAL and SYSGCAL commands. During system calibration, the appropriate calibration signals must be applied by the user to the inputs.

SYSOCAL performs a system offset calibration. The user must supply a zero input differential signal. The CP1266 then computes a value that will nullify the offset in the system. Table 19 shows the time required for system offset calibration for the different data rate settings. Note this timing is the same for the self offset calibration. System offset calibration updates the OFC register.

SYSGCAL performs a system gain calibration. The user must supply a full-scale input signal to the CP1266.The CP1266 then computes a value to nullify the gain error in the system. System gain calibration can correct inputs that are 80% of the full-scale input voltage and larger. Make sure not to exceed the full-scale input voltage when using system gain calibration. Table 22 shows the time required for system gain calibration for the different data rate settings. System gain calibration updates the FSC register

Table 22. System Gain Calibration Timing

DATA RATE(SPS)	SELF GAIN CALIBRATION TIME
15,000	484μs
7500	617μs
3750	884μs
2000	1.4ms
1000	2.3ms
500	4.3ms
100	20.3ms
60	33.7ms
50	40.3ms
30	67.0ms
25	80.3ms
15	133.7ms
10	200.3ms
5	400.3ms
2.5	800.3ms

NOTE: f_{CLKIN}= 7.68MHz.

SERIAL INTERFACE

The SPI-compatible serial interface consists of four signals: CS_N, SCLK, DIN, and DOUT, and allows a controller to communicate with the CP1266. The programmable functions are controlled using a set of on-chip registers. Data is written to and read from these registers via the serial interface The DRDY_N output line is used as a status signal to indicate when a conversion has been completed. DRDY_N goes low when new data is available. The Timing Specification shows the timing diagram for interfacing to the CP1266.

CHIP SELECT (CS_N)

The chip select (CS_N) input allows individual selection of a CP1266 device when multiple devices share the serial bus. CS_N must remain low for the duration of the serial communication. When CS_N is taken high, the serial interface is reset and DOUT enters a high impedance state. CS_N may be permanently tied low.

SERIAL CLOCK (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT pins into and out of the CP1266. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

DATA INPUT (DIN) AND DATA OUTPUT (DOUT)

The data input pin (DIN) is used along with SCLK to send data to the CP1266. The data output pin (DOUT) along with SCLK is used to read data from the CP1266. Data on DIN is shifted into the part on the falling edge of SCLK while data is shifted out on DOUT on the rising edge of SCLK.

DATA READY (DRDY_N)

The DRDY_N output is used as a status signal to indicate when conversion data is ready to be read. DRDY_N goes low when new conversion data is available. It is reset high when all 24 bits have been read back using Read Data (RDATA) or Read Data Continuous (RDATAC) command. It also goes high when the new conversion data is being updated. Do not retrieve during this update period as the data is invalid. If data is not retrieved, DRDY_N will only be high during the update time as shown in Figure 24.

Figure 24. DRDY_N with No Data Retreival

After changing the PGA, data rate, buffer status, writing to the OFC or FSC registers, perform a synchronization operation to force DRDY_N high. It will stay high until valid data is ready. Exiting from Reset, Synchronization, Standby or Power-Down mode will also force DRDY_N high. DRDY_N will go low as soon as valid data are ready.

SYNCHRONIZATION

Synchronization of the CP1266 is available to coordinate the A/D conversion with an external event and also to speed settling after an instantaneous change on the analog inputs (see Conversion Time using Synchronization section).

Synchronization can be achieved either using the SYNC_PDWN_N pin or with the SYNC command. To use the SYNC_PDWN_N pin, take it low and then high, making sure to meet timing specification t_{16} and t_{16B}.

Synchronization occurs after SYNC_PDWN_N is taken high. No communication is possible on the serial interface while SYNC_PDWN_N is low. If the SYNC_PDWN_N pin is held low for 20 DRDY_N periods the CP1266 will enter Power-Down mode.

To synchronize using the SYNC command, first shift in all eight bits of the SYNC command. This stops the operation of the CP1266. When ready to synchronize, issue the WAKEUP command. Synchronization occurs on the first rising edge of the master clock after the first SCLK used to shift in the WAKEUP command. After a synchronization operation, either with the SYNC_PDWN_N pin or the SYNC command, DRDY_N stays high until valid data is ready.

STANDBY MODE

The standby mode shuts down all of the analog circuitry and most of the digital features. The oscillator continues to run to allow for fast wakeup. To enter Standby mode, issue the STANDBY command. To exit Standby mode, issue the WAKEUP command. DRDY_N will stay high after exiting Standby mode until valid data is ready. Standby mode can be used to perform one-shot conversions; see Settling Time Using One-Shot Mode section for more details.

POWER-DOWN MODE

Holding the SYNC_PDWN_N pin low for 20 DRDY_N cycles activates the Power-Down mode. During Power-Down mode, all circuitry is disabled including the oscillator and the clock output. To exit Power-Down mode, take the SYNC_PDWN_N pin high. Upon exiting from Power-Down mode, the CP1266 crystal oscillator typically requires 30ms to wake up. If using an external clock source, 8192 CLKIN cycles are needed before conversions begin.

RESET

There are two methods to reset the CP1266: the RESET_N input pin, and RESET command.

When using the RESET_N pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the RESET_N pin back high.

The RESET command takes effect after all eight bits have been shifted into DIN. Afterwards, the reset releases automatically. On reset, the configuration registers are initialized to their default state. After releasing from RESET, self-calibration is recommended.

POWER-UP

All of the configuration registers are initialized to their default state at power-up. A self-calibration is then performed automatically. For the best performance, it is strongly recommended to perform an additional self-calibration by issuing the SELFCAL command after the power supplies and voltage reference have had time to settle to their final values.

APPLICATIONS INFORMATION

The CP1266 is a very high-resolution A/D converter. Getting the optimal performance from them requires careful attention to their support circuitry and printed circuit board (PCB) design. Figure 25 shows the basic connections for the CP1266. It is recommended to use a single ground plane for both the analog and digital supplies. This ground plane should be shared with the bypass capacitors and analog conditioning circuits. However, avoid using this ground plane for noisy digital components such as microprocessors. If a split ground plane is used with the CP1266, make sure the analog and digital planes are tied together. There should not be a voltage difference between the CP1266 analog and digital ground pins (AGND and DGND).

As with any precision circuit, use good supply bypassing techniques. A smaller value ceramic capacitor in parallel with a larger value tantalum or a larger value low-voltage ceramic capacitor works well. Place the capacitors, in particular the ceramic ones, close to the supply pins. Run the digital logic off as low of voltage as possible. This helps reduce coupling back to the analog inputs. Avoid ringing on the digital inputs. Small resistors ($\approx 100\,\Omega$) in series with the digital pins can help by controlling the trace impedance. When not using the RESET_N or SYNC_PDWN_N inputs, tie directly to the CP1266 DVDD pin.

Pay special attention to the reference and analog inputs. These are the most critical circuits. On the voltage reference inputs, bypass with low equivalent series resistance (ESR) capacitors. Make these capacitors as large as possible to maximize the filtering on the reference. With the outstanding performance of the CP1266, it is easy for the voltage reference to limit overall performance if not carefully selected. When using a stand-alone reference, make sure it is very low noise, very low drift, and capable of driving the CP1266 reference inputs. For voltage references not suited for driving the CP1266 directly (for example, high output impedance references or resistive voltage dividers), use the recommended buffer circuit shown in Figure 26. Ratiometric measurements, where the input signal and reference track each other, are somewhat less sensitive, but verify the reference signal is clean.

Often times, only a simple RC filter (as shown in Figure 25) is needed on the inputs. This circuit limits the high-frequency noise near the modulator frequency; see the Frequency Response section. Avoid low-grade dielectrics for the capacitors to minimize temperature variations and leakage. Keep the input traces as short as possible and place the components close to the input pins, and make sure to filter all the input channels being used.

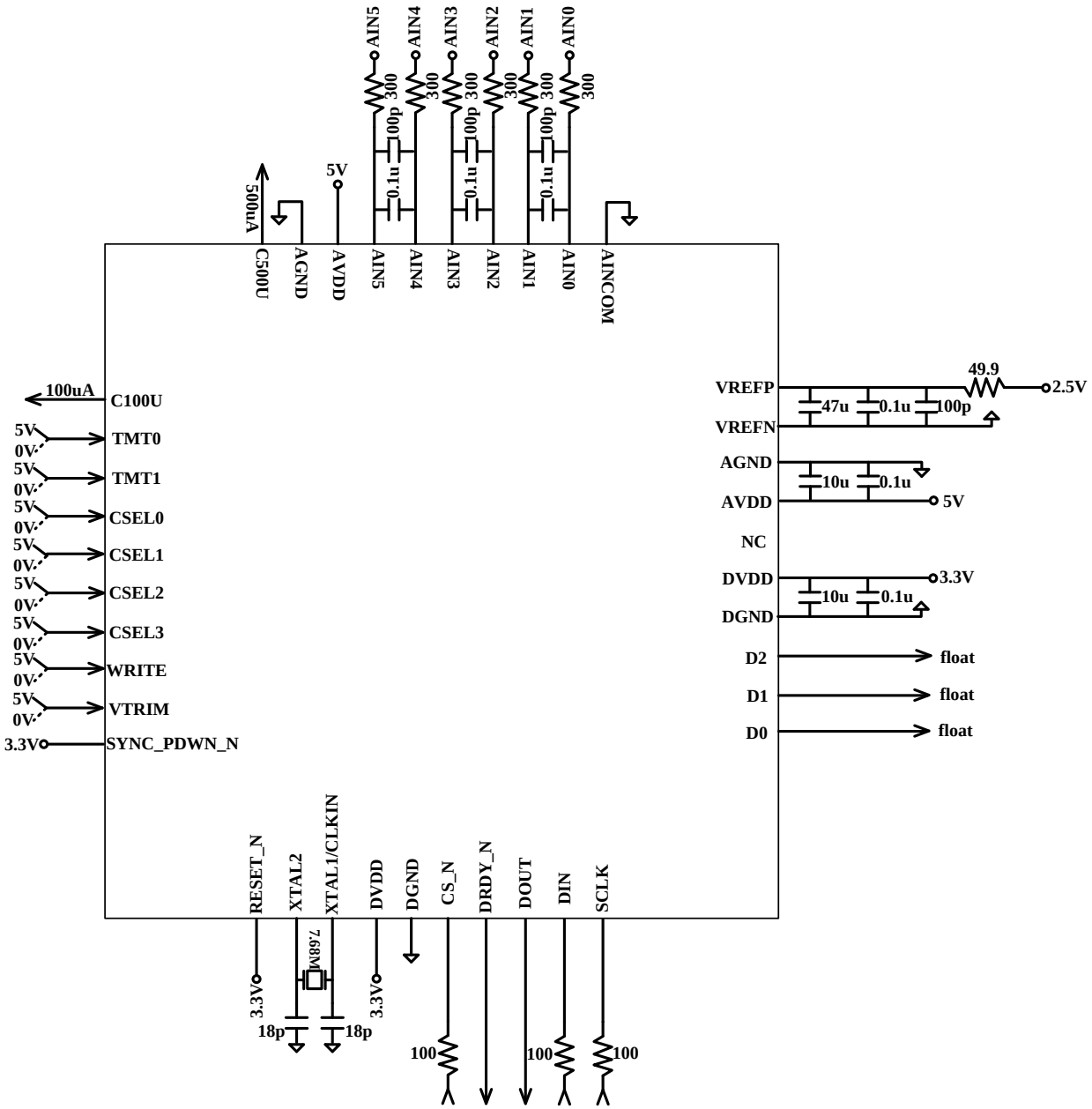


Figure 25. CP1266 Basic Connections

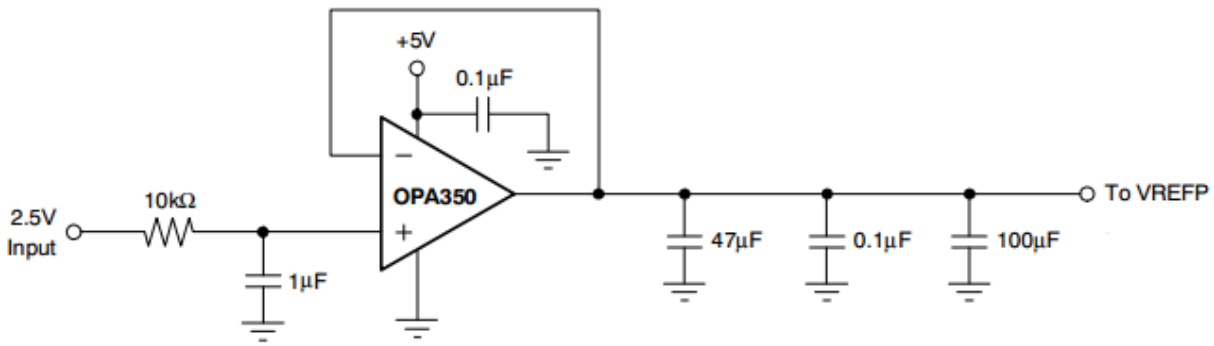


Figure 26. Recommended Voltage Reference Buffer Circuit

DIGITAL INTERFACE CONNECTIONS

The CP1266 SPI, QSPI™, and MICROWIRE™-compatible interface easily connects to a wide variety of microcontrollers. Figure 27 shows the basic connection to TI's MSP430 family of low-power microcontrollers. Figure 28 shows the connection to microcontrollers with an SPI interface like TI's MSC12xxfamily or the 68HC11 family. Note that the MSC12xx includes a high-resolution A/D converter; the CP1266 can be used to add additional channels of measurement or provide higher-speed conversions.

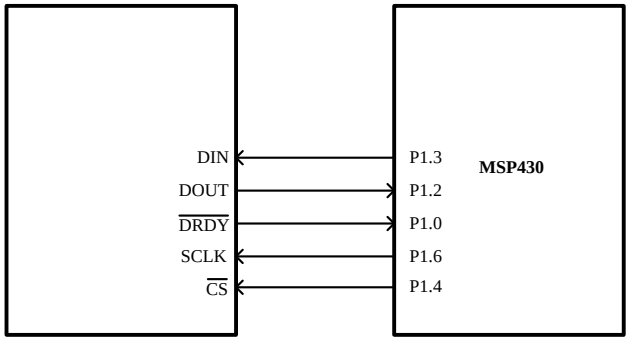


Figure 27. Connection to MSP430 Microcontroller

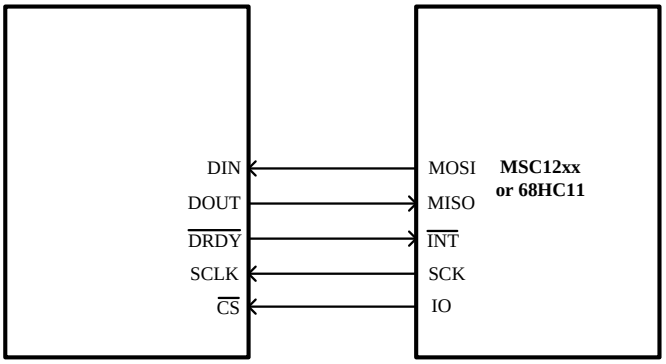


Figure 28. Connection to Microcontrollers withan SPI Interface

REGISTER MAP

The operation of the CP1266 is controlled through a set of registers. Collectively, the registers contain all the information needed to configure the part, such as data rate, multiplexer settings, PGA setting, calibration, etc., and are listed in Table 23.

Table 23. Register Map

ADDRESS	REGISTER	RESET VALUE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	STATUS	$A0_H$	ID3	ID2	ID1	ID0	--	--	BUFEN	--
01h	MUX	01_H	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02h	ADCON1	20_H	--	--	--	--	--	PGA2	PGA1	PGA0
03h	DRATE	02_H	DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0
05h	OFC0	xx_H	OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00
06h	OFC1	xx_H	OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08
07h	OFC2	xx_H	OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16
08h	FSC0	xx_H	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
09h	FSC1	xx_H	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
0Ah	FSC2	xx_H	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
83H	ADCON2	00H	--	--	--	--	--	PGACON	--	--

STATUS : STATUS REGISTER (ADDRESS 00h)

Reset Value = A1h

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ID3	ID2	ID1	ID0	--	--	BUFEN	--

Bits 7-4 ID3, ID2, ID1, ID0 Factory Programmed Identification Bits (Read Only)

Bit 3-2 Reserved, always 0 (Read Only)

Bit 1 BUFEN: input buffer control bit:

0 = disable the input buffer (default)

1 = enable the input buffer.

Bit 0 Reserved, always 1 (Read Only)

MUX : Input Multiplexer Control Register (Address 01h)

Reset Value = 01h

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

Bits 7-4 PSEL3, PSEL2, PSEL1, PSEL0: Positive Input Channel (AINP) Select

0000 = AIN0 (default)

0001 = AIN1

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = Reserved

0111 = Reserved

1xxx = AINCOM (when PSEL3 = 1, PSEL2, PSEL1, PSEL0 are “don’t care”)

Bits 3-0 NSEL3, NSEL2, NSEL1, NSEL0: Negative Input Channel (AINN)Select

0000 = AIN0

0001 = AIN1 (default)

0010 = AIN2

0011 = AIN3

0100 = AIN4

0101 = AIN5

0110 = Reserved

0111 = Reserved

1xxx = AINCOM (when NSEL3 = 1, NSEL2, NSEL1, NSEL0 are “don’t care”)

ADCON1: A/D Control Register 1 (Address 02h)

Reset Value = 20h

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
--	--	--	--	--	PGA2	PGA1	PGA0

Bit 7-3 Reserved, (Read Only)

Bits 2-0 PGA2, PGA1, PGA0: Programmable Gain Amplifier Setting

000 = 1 (default)

001 = 2

010 = 4

011 = 8

100 = 16

101 = 32

110 = 64

111 = 64

DRATE: A/D Data Rate (Address 03h)

Reset Value = 02h

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

The 16 valid Data Rate settings are shown below. Make sure to select a valid setting as the invalid settings may produce unpredictable results.

Bits 7-0 DR[7: 0]: Data Rate Setting(1)

00000010 = 7,500SPS (default)

00000011 = 3,750SPS

00000100 = 1875 SPS

00000101 = 1,000SPS

00000110 = 500SPS

00000111 = 250SPS

00001000 = 50SPS

00001001 = 30SPS

00001010 = 25 SPS

00001011 = 15 SPS

00001100 = 12.5 SPS

00001101 = 7.5 SPS

00001110 = 5 SPS

00001111 = 2.5SPS

00010000 = 1.25SPS

(1)for f_{CLKIN}= **3.84**MHz. Data rates scale linearly with f_{CLKIN}.

OFC0: Offset Calibration Byte 0, least significant byte (Address 05h)

Reset value depends on calibration results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00

OFC1: Offset Calibration Byte 1 (Address 06h)

Reset value depends on calibration results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08

OFC2: Offset Calibration Byte 2, most significant byte (Address 07h)

Reset value depends on calibration results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16

FSC0: Full−scale Calibration Byte 0, least significant byte (Address 08h)

Reset value depends on calibration results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSC 07	FSC 06	FSC 05	FSC 04	FSC 03	FSC 02	FSC 01	FSC 00

FSC1: Full−scale Calibration Byte 1 (Address 09h)

Reset value depends on calibration results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSC 15	FSC 14	FSC 13	FSC 12	FSC 11	FSC 10	FSC 09	FSC 08

FSC2: Full−scale Calibration Byte 2, most significant byte (Address 0Ah)

Reset value depends on calibration results.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FSC 23	FSC 22	FSC 21	FSC 20	FSC 19	FSC 18	FSC 17	FSC 16

ADCON2: A/D Control Register2 (Address 83h)

Reset Value = 00h

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
--	--	--	--	--	PGACON	--	--

Bit 7-3, 1-0 Reserved, always 0 (Read Only)

Bits 2 PGACON: PGA control bit:

0 = when PGA=1,2,4,8,16 (default)

1 = Set the bit to 1 when the PGA=32 and 64.

COMMAND DEFINITIONS

The commands summarized in Table 24 control the operation of the CP1266. All of the commands are stand-alone except for the register reads and writes (RREG, WREG) which require a second command byte plus data. Additional command and data bytes may be shifted in without delay after the first command byte. CS_N must stay low during the entire command sequence.

Table 24. Command Definitions

COMMAND	DESCRIPTION	1ST COMMAND BYTE	2ND COMMAND BYTE	3RD COMMAND BYTE
WAKE UP	Completes SYNC and Exits Standby Mode	0000 0000 (00h)	--	--
RDATA	Read Data	0000 0001 (01h)	--	--
RDATAC	Read Data Continuously	0000 0011 (03h)	--	--
SDATAC	Stop Read Data Continuously	0000 1111 (0Fh)	--	--
RREG	Read from REG rrr	0001 adrh(1) (1xh)	adrl(2)xxxx(3)	dddddddd(4)
WREG	Write to REG rrr	0101 adrh (5xh)	adrlxxxx	dddddddd
SELFCAL	Offset and Gain Self-Calibration	0101 0010 (52h)	1110 0000 (E0h)	0000 0101 (05h)
SELFOCAL	Offset Self-Calibration	0101 0010 (52h)	1110 0000 (E0h)	0000 0001 (01h)
SELFGCAL	Gain Self-Calibration	0101 0010 (52h)	1110 0000 (E0h)	0000 0010 (02h)
SYSOCAL	System Offset Calibration	0101 0010 (52h)	1110 0000 (E0h)	0000 0011 (03h)
SYSGCAL	System Gain Calibration	0101 0010 (52h)	1110 0000 (E0h)	0000 0100 (04h)
SYNC	Synchronize the A/D Conversion	1111 1100 (FCh)	--	--
STANDBY	Begin Standby Mode	1111 1101 (FDh)	--	--
RESET	Reset to Power-Up Values	1111 1110 (FEh)	--	--
WAKE UP	Completes SYNC and Exits Standby Mode	1111 1111 (FFh)	--	--

NOTE:

(1) adrh = high four bits of the target register address.

(2) adrl = low four bits of the target register address.

(3) xxxx = can be set to any value.

(4) dddddddd = the data to be read or to be written.

RDATA: Read Data

Description: Issue this command after DRDY_N goes low to read a single conversion result. After all 24 bits have been shifte dout on DOUT, DRDY_N goes high. It is not necessary to read back all 24 bits, but DRDY_N will then not return high until new data is being updated. See the Timing Characteristics for the required delay between the end of the RDATA command and the beginning of shifting data on DOUT: t_6.

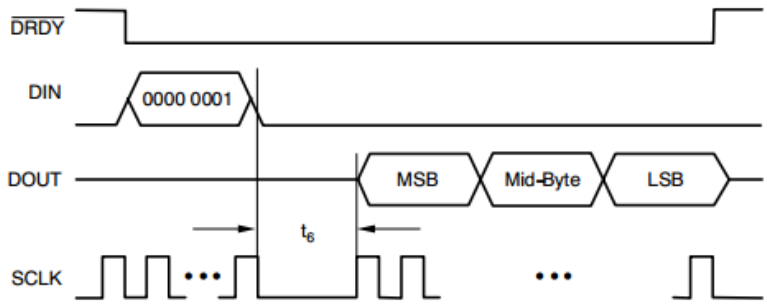


Figure 30a. RDATA Command Sequence

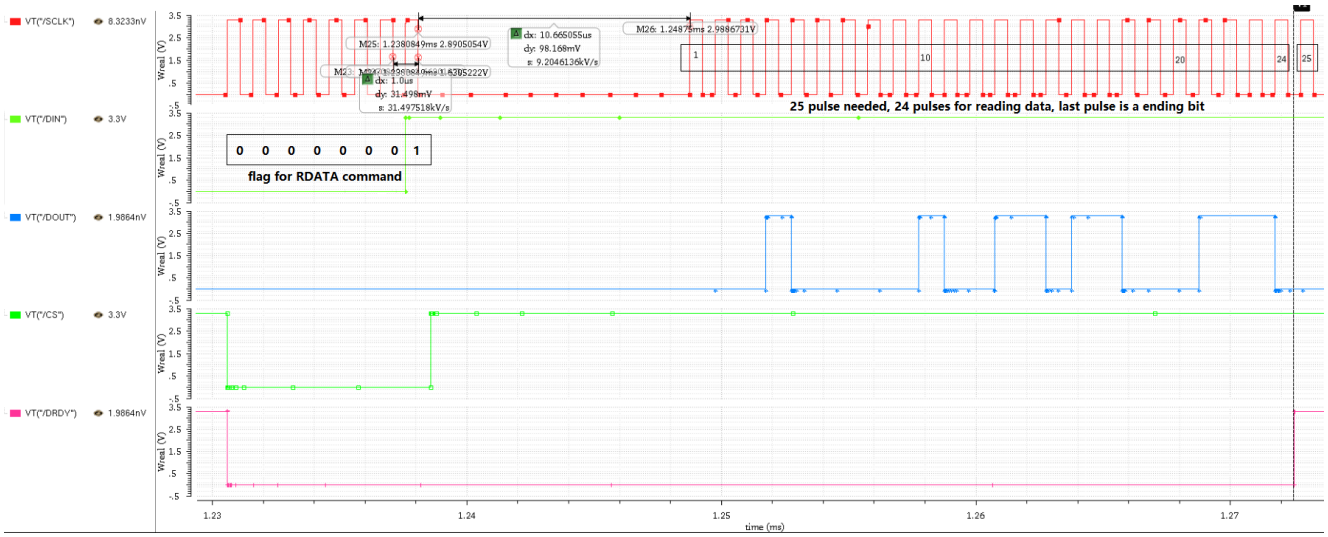


Figure 30b. RDATA Command Sequence (Detailed timing)

RDATAC: Read Data Continuous

Description: Issue command after DRDY_N goes low to enter the Read Data Continuous mode. This mode enables the continuous output of new data on each DRDY_N without the need to issue subsequent read commands. After all 24 bits have been read, DRDY_N goes high. It is not necessary to read back all 24 bits, but DRDY_N will then not return high until new data is being updated. This mode may be terminated by the Stop Read Data Continuous command (SDATAC). Because DIN is constantly being monitored during the Read Data Continuous mode for the SDATAC or RESET command, do not use this mode if DIN and DOUT are connected together.

In figure31, the delay between the second falling edge of DRDY_N and the next rising edge of SCLK: t_{18}, should be at least 500ns.

See the Timing Characteristics for the required delay between the end of the RDATAC command and the beginning of shifting data on DOUT: t_6.

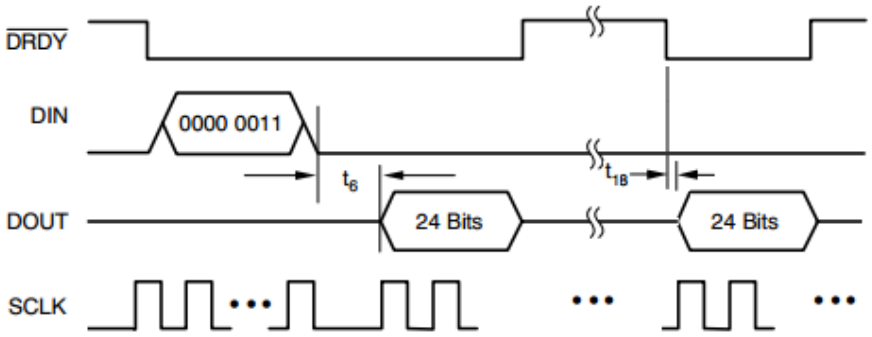


Figure 31a. RDATAC Command Sequence

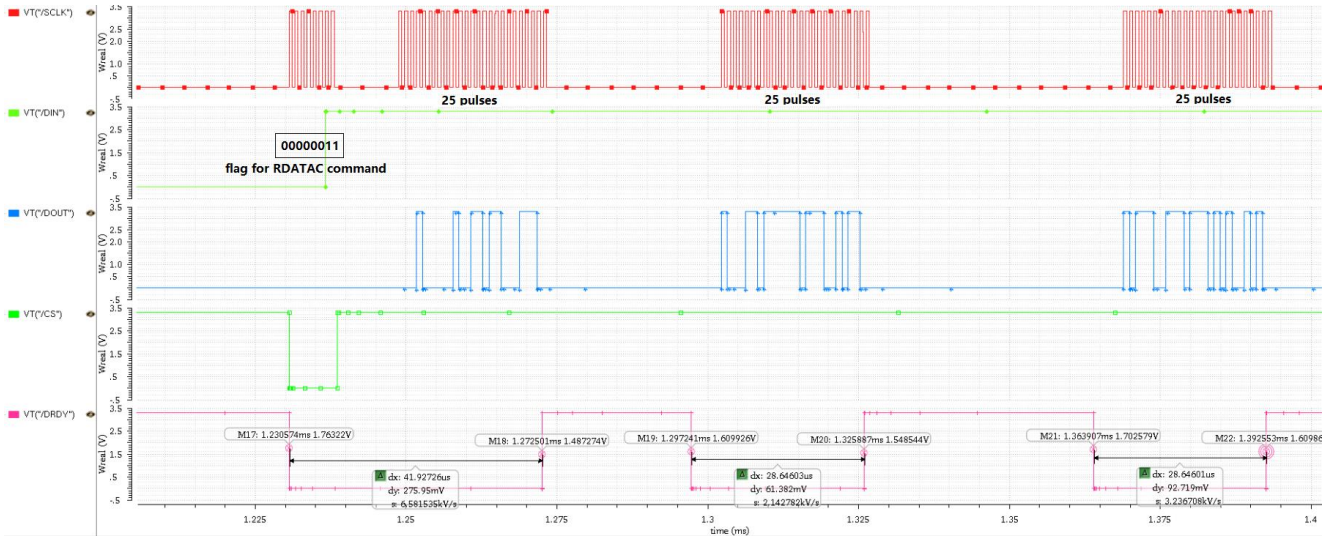


Figure 31b. RDATAC Command Sequence (Detailed timing)

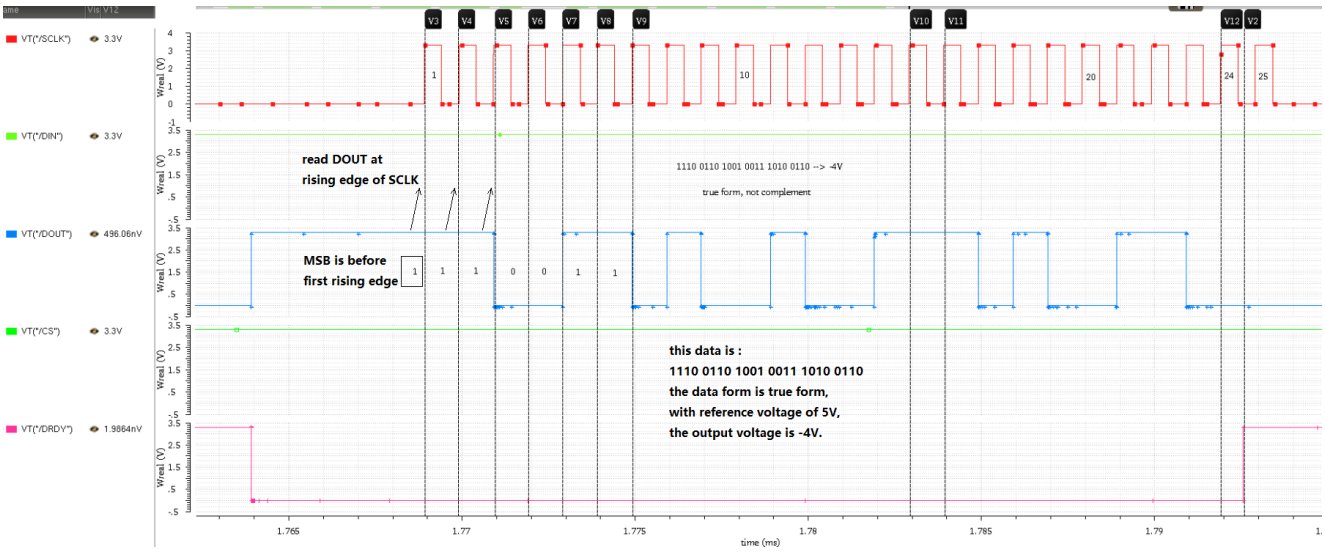


Figure 31c. RDATAC Command Sequence (Time pattern of reading one set of data)

On the following DRDY_N, shift out data by applying SCLKs. The Read Data Continuous mode terminates if input_data equals the SDATAC or RESET command in any of the three bytes on DIN.

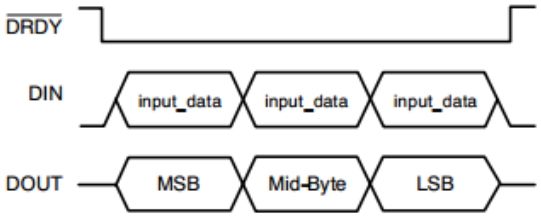


Figure 32. DIN and DOUT Command Sequence During Read Continuous Mode

SDATAC: Stop Read Data Continuous

Description: Ends the continuous data output mode. (see RDATAC). The command must be issued after DRDY_N goes low and completed before DRDY_N goes high.

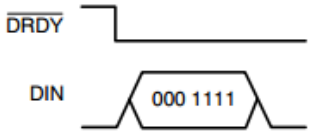


Figure 33. SDATAC Command Sequence

RREG: Read from Registers

Description: Output the data from registers.

1st Command Byte: 0001 adrh, where adrh is the high four bits of address of the register to read.

2nd Command Byte: adrl xxxx, where adrl is the low four bits of address of the register to read, and xxxx can be set to any value.

See the Timing Characteristics for the required delay between the end of the RREG command and the beginning of shifting data on DOUT: t6.

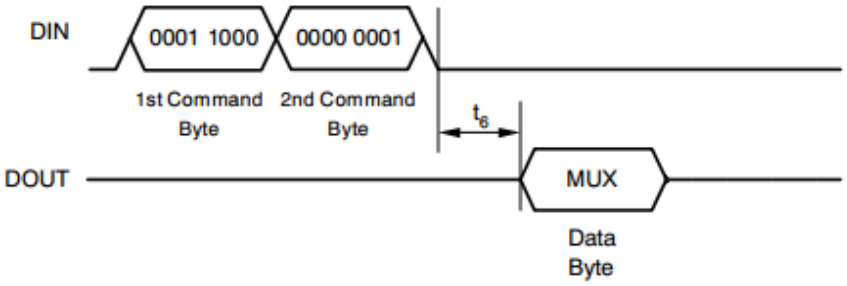


Figure 34a. RREG Command Example: Read from Register 80h (Multiplexer)

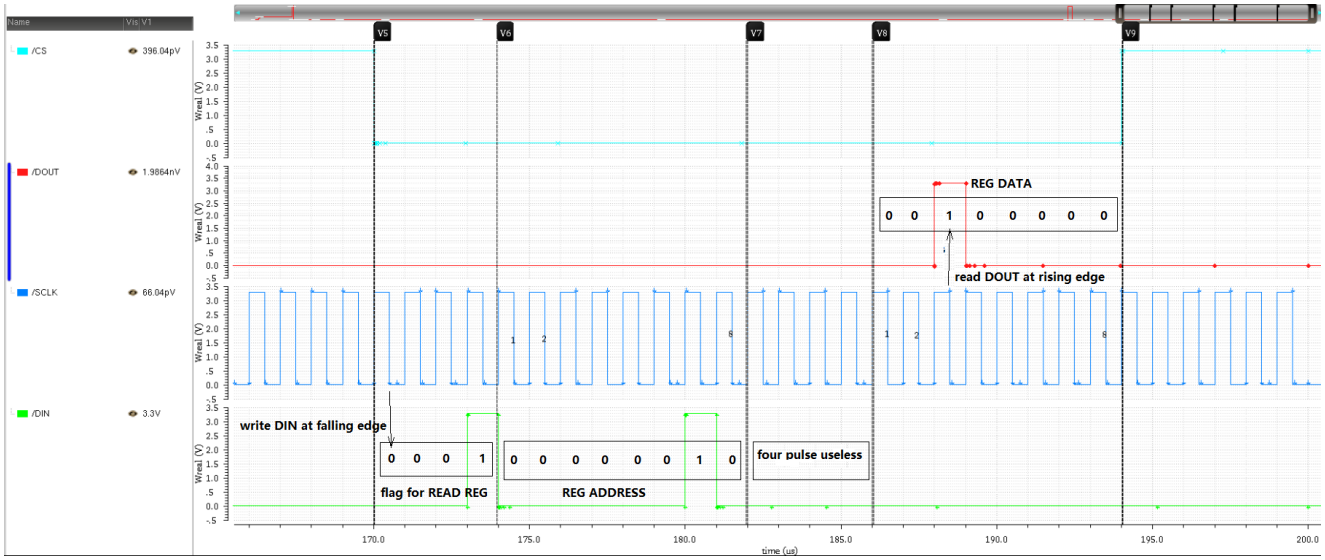


Figure 34b. RREG Command Example: Read from Register 02h (Data:20h,SCLK runs at 1MHz)

WREG: Write to Register

Description: Write to the register specified with three command bytes.

1st Command Byte: 0101 adrh, where adrh is the high four bits of address of the register to be written.

2nd Command Byte: adrl xxxx, where adrl is the low four bits of address of the register to be written, and xxxx can be set to any value.

3rd Command Byte (Data Byte): data to be written to the register.

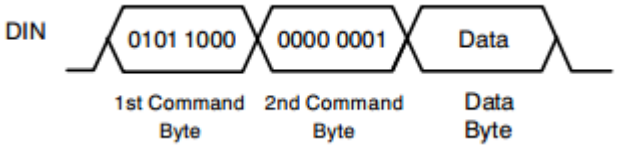


Figure 35a. WREG Command Example: Write Data to 80h (Multiplexer)

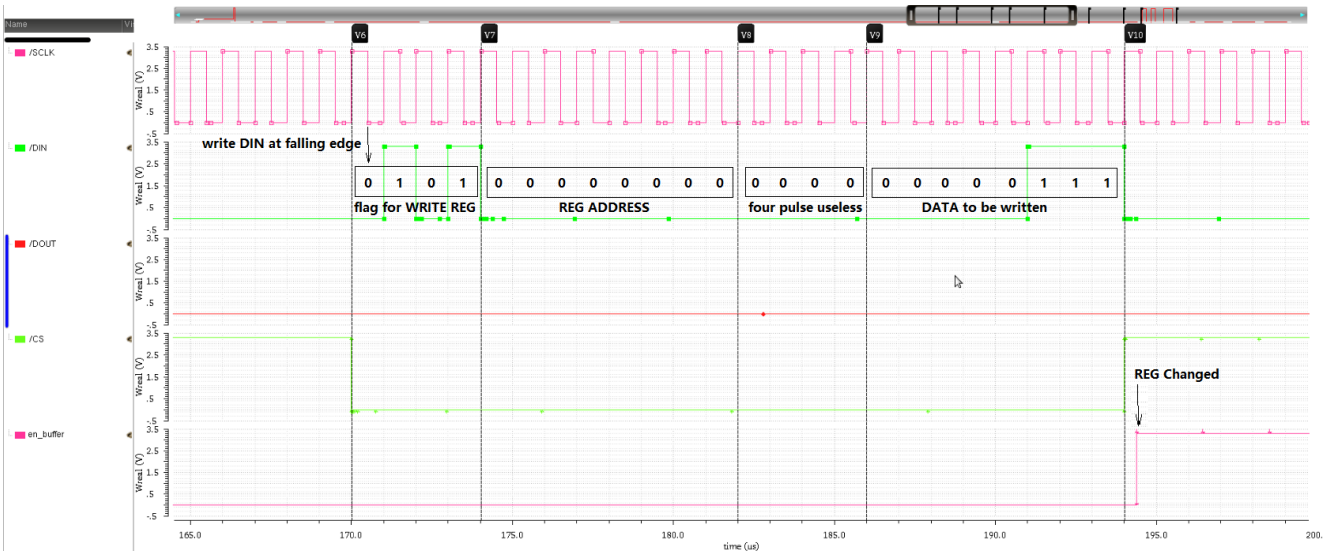


Figure 35b. WREG Command Example: Write Data to 00h (Data:07h, SCLK runs at 1MHz)

SELFCAL: Self Offset and Gain Calibration

Description: Performs a self offset and self gain calibration. The Offset Calibration Register (OFC) and Full-Scale Calibration Register (FSC) are updated after this operation. DRDY_N goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until DRDY_N goes low indicating that the calibration is complete.

SELFOCAL: Self Offset Calibration

Description: Performs a self offset calibration. The Offset Calibration Register (OFC) is updated after this operation. DRDY_N goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until DRDY_N goes low indicating that the calibration is complete.

SELFGCAL: Self Gain Calibration

Description: Performs a self gain calibration. The Full-Scale Calibration Register (FSC) is updated with new values after this operation. DRDY_N goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until DRDY_N goes low indicating that the calibration is complete.

SYSOCAL: System Offset Calibration

Description: Performs a system offset calibration. The Offset Calibration Register (OFC) is updated after this operation. DRDY_N goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until DRDY_N goes low indicating that the calibration is complete.

SYSGCAL: System Gain Calibration

Description: Performs a system gain calibration. The Full-Scale Calibration Register (FSC) is updated after this operation. DRDY_N goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until DRDY_N goes low indicating that the calibration is complete.

SYNC: Synchronize the A/D Conversion

Description: This command synchronizes the A/D conversion. To use, first shift in the command. Then shift in the WAKEUP command. Synchronization occurs on the first CLKIN rising edge after the first SCLK used to shift in the WAKEUP command.

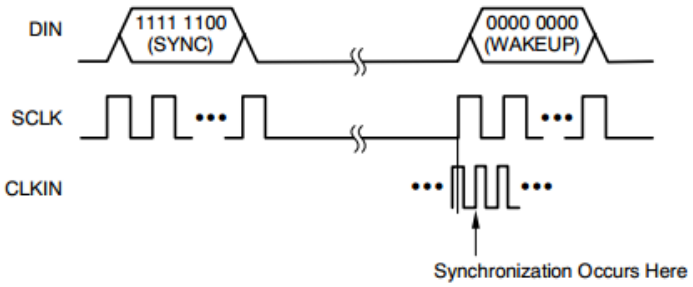


Figure 36. SYNC Command Sequence

STANDBY: Standby Mode / One-Shot Mode

Description: This command puts the CP1266 into a low-power Standby mode. After issuing the STANDBY command, make sure there is no more activity on SCLK while CS_N is low, as this will interrupt Standby mode. If CS_N is high, SCLK activity is allowed during Standby mode. To exit Standby mode, issue the WAKEUP command. This command can also be used to perform single conversions (see One-Shot Mode section).

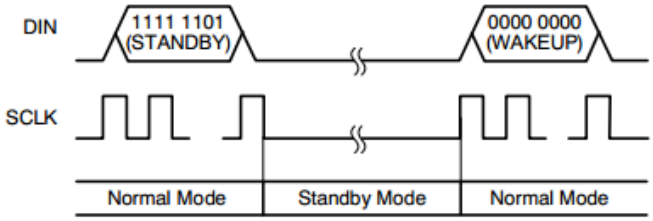


Figure 37. STANDBY Command Sequence

WAKEUP: Complete Synchronization or Exit Standby Mode

Description: Used in conjunction with the SYNC and STANDBY commands. Two values (all zeros or all ones) are available for this command.

RESET: Reset Registers to Default Values

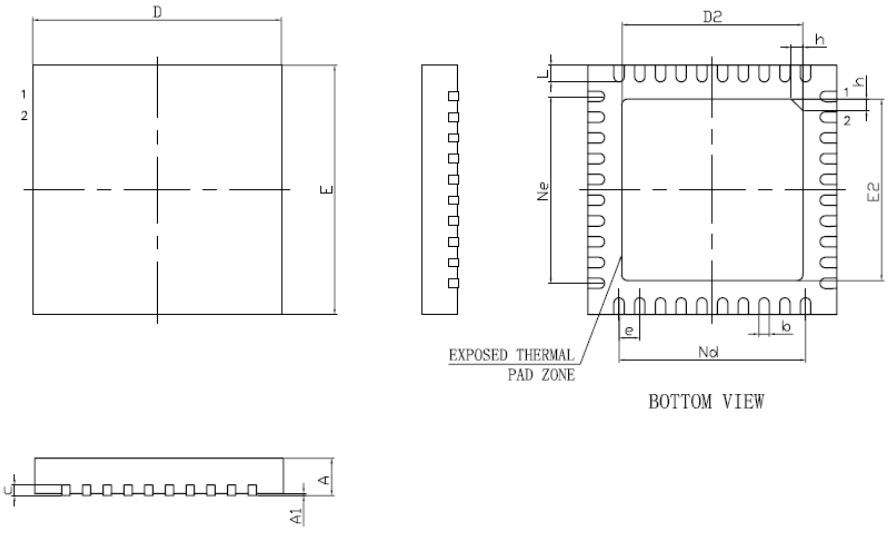
Description: Returns all registers except the CLK0 and CLK1 bits in the ADCON1 register to their default values. This command will also stop the Read Continuous mode: in this case, issue the RESET command after DRDY_N goes low.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION

PACKAGE INFORMATION

40 PINSQFN PACKAGE



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	177*177		