List of Figures

List of Tables

1. General Overview

1.1 Block Diagram

Figure 1 shows the principle block diagram of MLX80104/5.

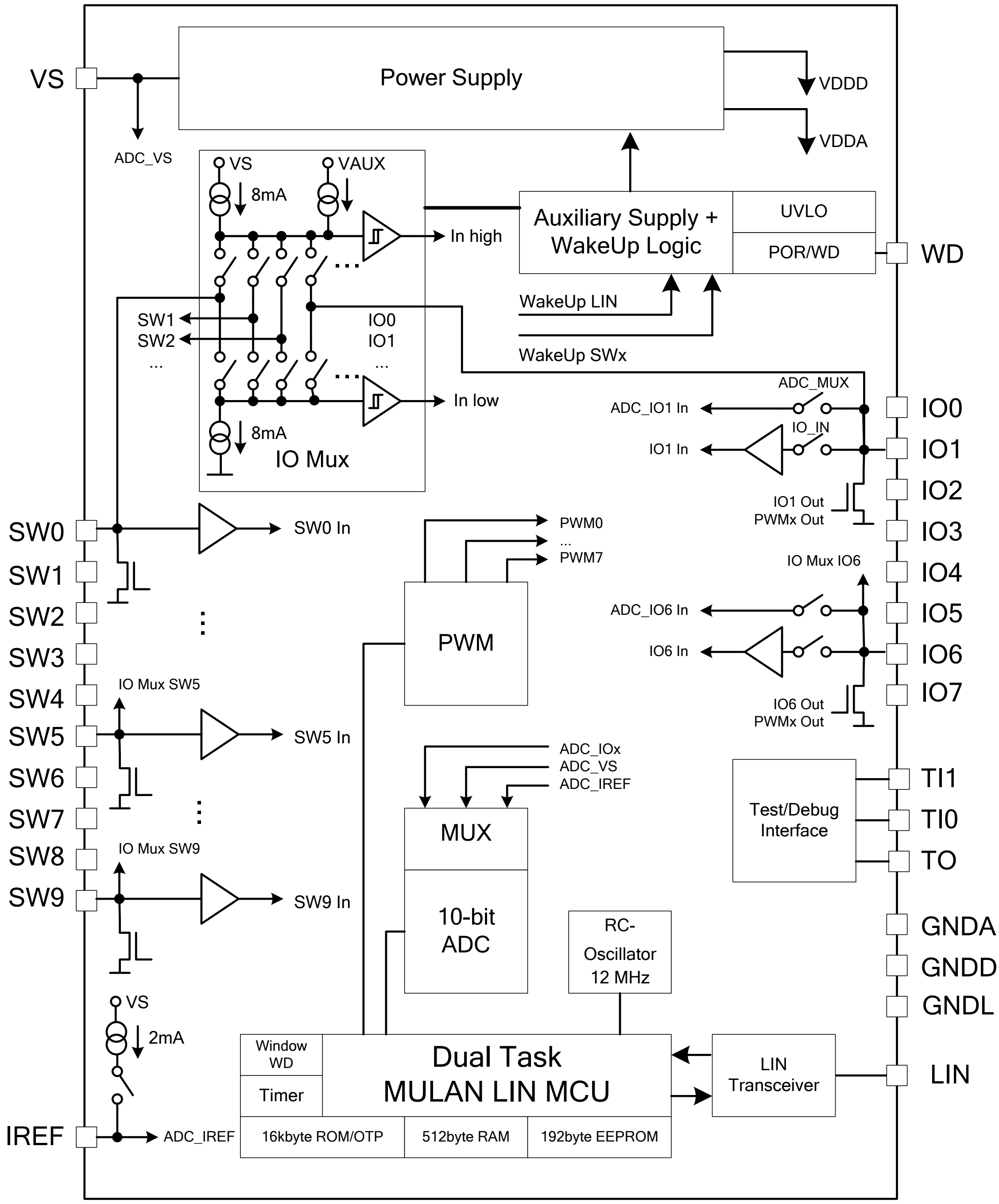


Figure 1 - Block Diagram

2. Electrical Characteristics

All voltages are referenced to ground (GND). Positive currents flow into the IC.

2.1 Absolute Maximum Ratings

In accordance with the Maximum Rating System (IEC 60134). The absolute maximum ratings given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may affect the reliability of the device.

Parameter	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S		-0.3	40	V
Short term supply voltage	V_{S_ld}	ISO 7637/2 pulse 5; t < 400 ms	-0.3	40	V
Transients at supply voltage	V_{S_tr1}	ISO 7637/2 pulse 1[1]	-100		V
Transients at supply voltage	V_{S_tr2}	ISO 7637/2 pulses 2 [1]		+50	V
Transients at high voltage signal pins	V_{LINx_tr1}	ISO 7637/3 pulse 1 [2]	-100		V
Transients at high voltage signal pins	V_{LINx_tr2}	ISO 7637/3 pulses 2 [2]		+50	V
Transient at high voltage signal and power supply pins	V_{HV_tr3}	ISO 7637/2 pulses 3A, 3B [3]	-150	+100	V
DC voltage on LIN, SWx, IOx pins	V_{LIN_DC}	T<500ms, V_S = 18V V_S = 0V	-22 -40	40	V
DC voltage on IREF, AWD pin	V_{logic_DC}		-0.3	7	V
ESD capability	V_{ESDIEC}	IEC 61000-4-2 Pin LIN, VS to GND	-6	6	kV
	V_{ESDHBM}	HBM (AEC-Q100-002) [4] Pin LIN, VS to GND Other pins	-8 -2	8 2	kV kV
	V_{ESDCDM}	CDM (AEC-Q100-011)	-750	750	V
Maximum latch – up free current at any pin	I_{LATCH}		-500	500	mA
Maximum power dissipation	P_{tot}	T_{amb} = +125 °C		0.78	W
		T_{amb} = + 85 °C		2	
Thermal impedance	Θ_{JA}	JEDEC 1s2p board, none air flow		32	K/W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_{vj}		-40	+150	°C

Table 1 - Absolute Maximum Ratings

[1] ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[2] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 100nF.
[3] ISO 7637/3 test pulses are applied to LIN via a coupling capacitance of 1nF.
ISO 7637/2 test pulses are applied to VS via a reverse polarity diode and >2uF blocking capacitor.
[4] Equivalent to discharging a 100pF capacitor through a 1.5Kohm resistor conforms to AEC-Q100-002

2.2 Operating Conditions

Parameter	Symbol	Min	Max	Unit
Battery supply voltage [1]	V_S	5	18	V
Short time battery supply voltage [2]	V_{S_S}	18	27	V
Operating ambient temperature	T_{amb}	-40	+125	°C

Table 2 - Operating Conditions

[1] V_s is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4…1V, V_{BAT_ECU} = 6…27V.
[2] Short time: t < 1 min

2.3 Static Characteristics

(V_S = 5 to 27V, T_A = -40 to +125°C, unless otherwise specified)

	Parameter	Symbol	Condition	Min	Typ	Max	Unit
	Pin VS						
3.00	Supply current, active without switch current	I_S			6	20	mA
3.01	Undervoltage lockout	V_{S_UV}				5	V
3.02	Supply current, sleep mode	I_{Ssl_typ}	V_S = 12V		25	50	µA
3.03	Supply current, sleep mode	I_{Ssl}	V_S = 18V			90	µA
	PIN LIN						
3.10	Short circuit bus current	I_{BUS_LIM}	V_{LIN}= V_S = 18V, TxD = 0	40	120	200	mA
3.11	Pull up resistor LIN	R_{SLAVE}	V_{LIN}=0, TxD open	20	30	60	kΩ
3.12	Pull up current LIN, Sleep mode	$I_{BUS\_PU\_Sleep}$	V_{LIN}=0, V_S=12V, sleep mode	-100	-75		µA
3.13	LIN reverse current, recessive	$I_{BUS\_PAS\_rec}$	V_{LIN}>V_S , 5V <V_{LIN} <18V, 5V <V_S <18V , TxD open			20	µA
	Receiver input leakage current	$I_{BUS\_PAS\_dom}$	V_S = 12V, V_{LIN}=0	-1			mA
3.14	LIN reverse current loss of battery	$I_{BUS\_NO\_BAT}$	V_S=0V, 0V < V_{LIN} < 18V			23	µA
3.15	LIN current during loss of Ground [3]	$I_{BUS\_NO\_GND}$	V_S=V_{GND}=12V, 0V<V_{LIN}<18V	-100		20	µA
3.16	Transmitter dominant voltage	V_{ol_LIN}	load=500Ω, TxD=0			0.2	Vs
3.17	Recessive output voltage	V_{oh_LIN}	TxD open	0.8		1	Vs
3.18	Lin input capacitance [1]	C_{LIN}	Pulse response via 1kΩ, V_{Pulse}=12V, V_S=14V		25	35	pF
3.19	Voltage drop serial diode [1]	$C_{SerDiode}$		0.4	0.7	1.0	V
3.30	Receiver dominant voltage	V_{BUSdom}				0.4*V_S	V
3.31	Receiver recessive voltage	V_{BUSrec}		0.6*V_S			V
3.32	Centre point of receiver threshold	V_{BUS_cnt}	V_{BUS_cnt} =(V_{th_dom} + V_{th_rec})/2	0.475*Vs	0.5*Vs	0.525*Vs	V
3.33	Receiver hysteresis	V_{HYS}	V_{HYS} =(V_{th_dom} -V_{th_rec})			0.175*Vs	V

Parameter		Symbol	Condition	Min	Typ	Max	Unit
PIN SWx, IOx in normal mode							
3.40	Central current source on resistance pull up configuration	R_{ih_SWx}	Pull up mode, voltage shift max 0.1*Vs			1	KΩ
3.41	Central current source on resistance pull down configuration	R_{il_SWx}	Pull down mode, voltage shift max 0.1*Vs			1	KΩ
3.42	High level input voltage	V_{ih_SWx}	Input mode	1.4			V
3.43	Low level input voltage	V_{il_SWx}	Input mode			0.9	V
3.44	On resistance SWx	R_{ON_IO}	Low side mode, V_{SWx}=0.5V		50	100	Ω
3.45	Source current central current source	I_{ih_SWx}	Vs=5V Vs=13V (T_A = 25°C) Vs=18V	1.5 7		 12	mA
3.46	Sink current central current source	I_{il_SWx}	Vs=5V Vs=13V (T_A = 25°C) Vs=18V	1.5 7		 12	mA
3.47	Leakage current low level input	I_{leakl_SWx}	V_{il_SWx} = 0, V_S = 18V	-10		10	µA
3.48	Leakage current high level input	I_{leakh_SWx}	V_{ih_SWx} = 18V, V_S = 18V	-10		10	µA
PIN IREF							
3.60	Input voltage range	V_{IREF}		0		Vs	V
3.61	Output current	I_{IREF}		1.3	2	3.1	mA
3.62	Leakage current low level input	I_{leakl_IREF}	V_{IREF} = 0, V_S = 18V	-10		10	µA
3.63	Leakage current high level input	I_{leakh_IREF}	V_{IREF} = 3.4V, V_S = 18V	-10		10	µA
PIN AWD							
3.70	Input voltage range	V_{AWD}		0		3.4	V
3.71	Pull down current	I_{PD_AWD}			2		µA
3.72	Pull up current	I_{PU_AWD}			20		µA
3.73	RESET threshold	V_{AWD_IRQ}			0.5		V
3.74	Interrupt threshold	V_{AWD_Int}			1.5		V
3.75	Down threshold	V_{AWD_d}			2.5		V
Wakeup capability SWx,IOx							
3.80	Wake up pull up resistance SWx, IOx [4]	$R_{ih\_WU\_SWx}$	Pull up mode, voltage shift max 0.1Vs	500		1000	Ω
3.81	Wake up pull down resistance SWx, IOx [4]	$R_{il\_WU\_SWx}$	Pull down mode, voltage shift max 0.1Vs	500		1000	Ω
3.82	High level input voltage	$V_{ih\_WU\_SWx}$	Input mode	1.4			V
3.83	Low level input voltage	$V_{il\_WU\_SWx}$	Input mode			0.9	V
3.84	On resistance in sleep mode SWx/IOx	$R_{ON\_WU\_IO}$	Low side mode (S3x), $V_{SWx/IOx}$=0.5V		50	100	Ω

Parameter		Symbol	Condition	Min	Typ	Max	Unit
Thermal Protection							
3.90	Thermal shutdown [1]	T_{sd}		155		180	°C
3.91	Thermal recovery [1]	T_{rec}		126		150	°C

ADC Resolution (INL)							
3.67	ADC accuracy	V_{mess_diff}	One time measurement			5	LSB
3.68			Three time measurement			2	LSB
Switches							
On - resistance [2] [5]		R_{SW_on}	carbon on gold	0	150	1000	Ω
Off - resistance [2]		R_{SW_off}	Open switch	500			KΩ

Table 3 - Static Characteristics

[1] Parameter not tested in production, guaranteed by qualification.
[2] Switch parameter not determined by the IC, values are calculation basis for all currents and thresholds
[3] The current is determined by the master pull-up. To prevent discharging of the battery, the master pull up will be disconnected under Loss of Ground conditions
[4] Resistance is valid for the sum of switch resistance and the ESD protection resistance
[5] A 500Ohm series resistor is required in case of the remote switch outside of the module and the switch is in this case directly supplied from the battery

2.4 Dynamic Characteristics

(V_S = 7 to 27V, T_A = -40 to +125°C, unless otherwise specified)

Parameter		Symbol	Condition	Min	Typ	Max	Unit
PIN LIN							
4.01	Propagation delay receiver [1]	t_{rx_pdf}	C_{RxD} = 25pF, rising and Falling edge			6	µs
4.02	Propagation delay receiver symmetry [2]	t_{rx_sym}	$t_{tx\_pdf} - t_{rx\_pdr}$	-2		2	µs
4.03	Receiver debounce time [2]	t_{rx_deb}	LIN rising and falling edge	0.5		4	µs
4.04	LIN duty cycle 1 [3,4]	D1	20kbps operation, normal mode t_{Bit} = 50µs, D1=$t_{LIN\_rec(min)}$/(2*t_{Bit})	0.396			
4.05	LIN duty cycle 2 [3,4]	D2	20kbps operation, normal mode t_{Bit} = 50µs, D2=$t_{LIN\_rec(max)}$/(2*t_{Bit})			0.581	
4.06	LIN duty cycle 3 [3,4]	D3	10.4kbps operation, low speed, t_{Bit} = 96µs, D3=$t_{LIN\_rec(min)}$/(2*t_{Bit})	0.417			
4.07	LIN duty cycle 4 [3,4]	D4	10.4kbps operation, low speed, t_{Bit} = 96µs, D3=$t_{LIN\_rec(max)}$/(2*t_{Bit})			0.590	
4.08	$t_{rec(max)} - t_{dom(min)}$	Δt3	10.4kbps operation, low speed mode			15.9	µs
4.09	$t_{rec(min)} - t_{dom(max)}$	Δt4	10.4kbps operation, low speed mode			17.28	µs
4.12	Wake up filter time	t_{WU}	Sleep mode, LIN rising and falling edge	15		150	µs
PIN SWx/IOx							
4.21	Local wake-up filter time	t_{wu_local}	Sleep mode rising and falling edge	10	25	50	µs
ADCx							
4.22	Conversion time ADC	t_{conv}		12			µs
PIN IOx							
4.24	Slew Rate IOx[5]	t_{Slew_IOx}	Low side mode, V_S=6V, R_{pullup} =2.5kΩ, C_{load} = 20pF			2.5	µs
General							
	Device start up time [6] [7]	t_{SUP}	After POR,UVR, Wakeup	3	5	10	ms

Table 4 - Dynamic Characteristics

[1] This parameter is tested by applying a square wave signal to the LIN. The minimum slew rate for the LIN rising and falling edges is 50V/us
[2] See figure – Receiver debounce and propagation delay
[3] See figure – Duty cycle measurement and calculation
[4] Standard loads for duty cycle measurements are 1KΩ/1nF, 660Ω/6.8nF, 500Ω/10nF, internal termination disabled
[5] Only information
[6] Only characterization, guaranteed by design
[7] This time contains the activation time of hardware components and the software initialisation time. To get first valid switch status information, the programmed switch debouncing time must be added.

3. MULAN – MULtiple CPU with Analog and Network support

3.1 General

The MULAN CPU is a dual task implementation of the Melexis LIN Controller (MLX4) and the MLX16-8 CPU core. It is possible to run two tasks simultaneously with this architecture, one task for communication and the other task is free for the customer application. The communication between both tasks is done via API commands. The complete firmware including API for the LIN controller is supported by Melexis. The Customer only needs to program the application software on the MLX16-8 CPU. For a detailed description of this CPU please see the MLX16-8 data book.

3.2 MULAN Block Diagram

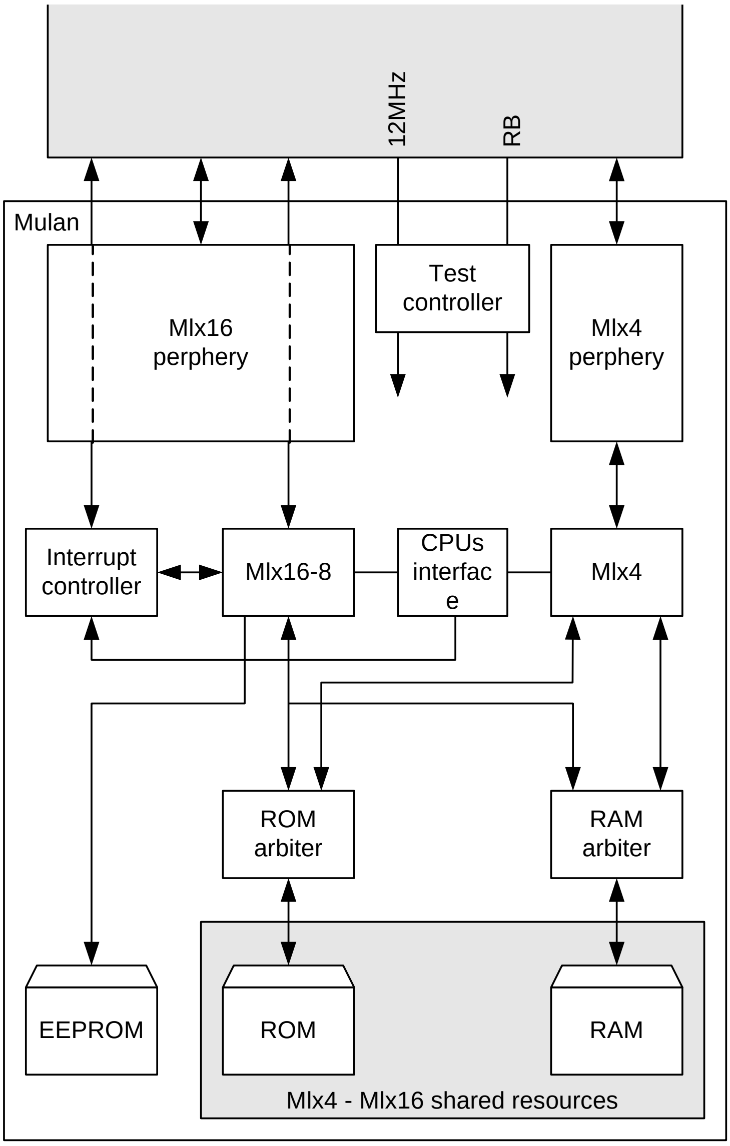


Figure 2 - Block Diagram of MULAN CPU

3.3 CPU Timing

MULAN use two CPUs:
A 4 bit CPU to handle a low speed protocol such as LIN.
A 16 bit CPU for an application firmware.

This construction has the following advantages:
The user does not need to take care of the real time problems of a protocol.
The protocol is handled by a Melexis firmware that can be updated when the protocol evolves.
The application CPU throughput is not affected by the protocol handling.
There is a native inter-task protection, e.g. an application crash does not affect the protocol handling.

Both CPUs share a common 12 MHz clock, a common ROM for program memory and a common RAM for data. Two memory arbiters are used for resolving conflicts with a common strategy: The Mlx4 always has priority.
Most of the time there is no conflict as the CPUs are interleaved as shown on Figure 3.

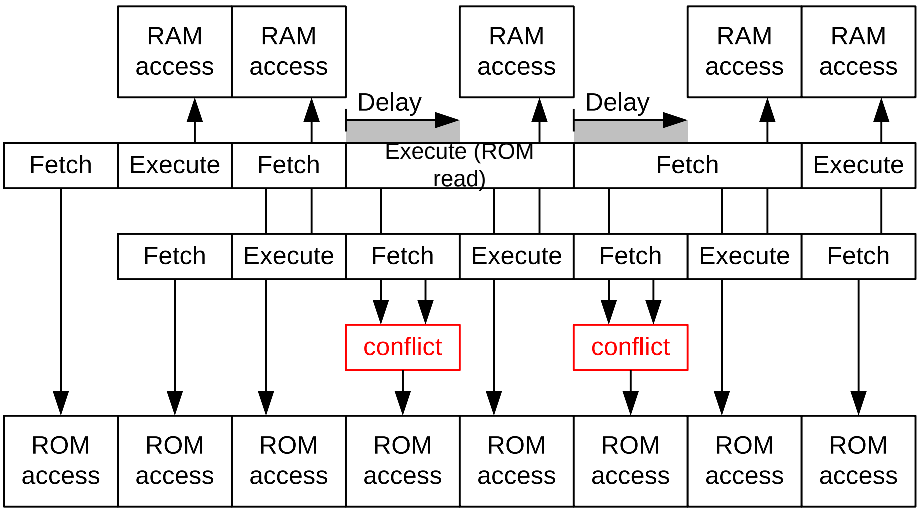


Figure 3 - CPU interleaving

3.4 MLX16-8

The 16 bit CPU is an Mlx16-8. This core is an evolution of the Mlx16 to increase GCC code generation efficiency. The change is limited to a few added instructions. A detailed description can be found in the Mlx16-8 datasheet. For readers familiar with the Mlx16, the list of instructions added is:

- CALLF : Call Far (anywhere within 64K)
- FSB : Find first bit set (in a word)
- MOVSB [X++], [Y++] : Copy array of bytes
- MOVSW [X++], [Y++] : Copy array of words
- Push #Word : Push a constant word into the stack
- SFB : Set first bit (in a word)

Moreover a new address mode has been added to allow direct access to any location. It is similar to dp: Addressing mode but allows any address within 64K at expense of an extra word of op-code.

4. Address Space

Mlx4 and Mlx16 share a common ROM and RAM. From the 2 CPUs a unified 16 bit bus is created (Von Neumann architecture). This bus is hooked to the ROM, the RAM, the EEPROM and the Mlx16-8 peripherals. Two arbiters are in charge of creating a unique memory address and corresponding access signals for ROM and RAM.

4.1 Memory Mapping

The unified 16 bit bus accesses devices as shown on Table 5.

Mlx16-8

Memory space					Allowed: Fetch	Write	System
E030	-	FFFF	Not used				
E000	-	E02F	Mlx16 System Ports	48 Bytes			
C020	-	DFFF	Not used				
C000	-	C01F	Mlx16 User ports	32 Bytes			
B000	-	BFFF	Not used				
A200	-	AFFF	Not used				
A000	-	A1FF	RAM (2)	RAM: 512 Bytes		(2)	
80C0	-	9FFF	Not used				
8014	-	80BF	EEPROM (1)	EEPROM: 172 Bytes			
8000	-	8013	EEPROM Melexis Area (1)	EEPROM: 20 Bytes			
4000	-	7FFF	Not used				
2000	-	3FFF	ROM	ROM: 8kBytes, Mlx16 code			
1000	-	1FFF	ROM	ROM: 4kBytes, Mlx4 or Mlx16 code			
0000	-	0FFF	ROM	ROM: 4kBytes, Minimum Mlx4 code			

(1): Fetch enabled in this area for patch codes
(2): See RAM sharing for Mlx4-Mlx16 distribution and protection

Table 5 - Unified memory mapping

There are some restrictions for accessing certain areas depending on the type of access:

- Mlx4 can fetch anywhere from 0x0000 to 0x1FFF (12 bits word address)
- Mlx16 can fetch from:
  - ROM: Normal case
  - EEPROM: For patched code
  - RAM: For test purposes
- Mlx4 and Mlx16 can read any RAM location (limited to 256 bytes for Mlx4)

The predefined pages of the Mlx16-8 are encoded as shown on Table 5. Some have fixed values (in grey) while others have value that depends of the ROM size. Table 6 gives examples for most common ROM sizes.

	ROM	
Name	**16K**	**Note**
Fp0:	3F00	Last ROM page (used by interrupt controller)
Fp1:	3E00	Could be used for C runtime
Fp2:	3D00	Could be used for C runtime
Fp3:	3C00	Could be used for C runtime
Fp4:	3B00	Could be used for C runtime
Fp5:	A100	In (large) RAM for fast patches (copied from EEPROM)
Fp6:	A000	In RAM Dp: for test routines
Fp7:	8000	In EEPROM to allow single instruction patch start
Dp:	A000	Mlx16 private RAM
Io:	C000	Standard Ports
Ep:	8000	EEPROM (First page)

Legend:

(grey)	Fixed address for any ROM size
(white)	Address depending on the ROM size

Table 6 - MLX16 pre-defined pages

4.2 RAM Sharing

A RAM size of 512 bytes is available for the MLX80104/5. This area is used by both CPUs.

While Mlx4 sees its private and shared RAM areas as 2 consecutive spaces, Mlx16 sees the private area of Mlx4 at the top of its RAM address space and the shared area at its bottom. This arrangement has the following advantages:

- Shared area is in Mlx16 Dp: address space, so Mlx16 has a fast access to it.
- The Mlx16-8 private area is in a single piece which makes GCC more efficient.

4.3 ROM/OTP Sharing

The MLX80104/5 has integrated 16Kbyte ROM or OTP. This area is used from both CPUs. The LIN Task + LIN API use 5kbytes while the rest (11kbytes) is available for the application running on the MLX16

Each CPU has is own separate program code in the ROM/OTP area but there is no specific mechanism to isolate them. The linker program merges the two programs and verifies that there is no overlapping, but if at execution time an error causes one CPU to jump into the code of the other one, it will of course execute unpredictable instructions and this situation will be detected either by watchdog overflow or protection error.

4.4 EEPROM

With the EEPROM it is possible to store non-volatile information. The EEPROM block is a 96 x 16bit Electrically Erasable Programmable Read Only Memory (EEPROM) with single power supply, single-error correction (SEC) and double-error detection (DED). An internal charge pump generates high voltage needed for the Erase/Write operations.

The EEPROM is Mlx16 private. The required EEPROM data for the Mlx4 execution is placed in RAM by the Mlx16 before it releases Mlx4 reset.
The EEPROM is organized in words (16 bits). Reading byte-wise is possible, but writing is only possible word-wise.

4.4.1. Static/dynamic Characteristics

Parameter	Remark	min	Typ	Max	Unit
Number of erase/write cycles	T_{amb} = 25°C	100 000			
	T_{amb} = 125°C	10 000			
Data retention time	T_{amb} = 85°C	10			Years
Erase/Write time	T_{amb} = -40…125°C	4		8	ms

4.4.2. Reserved EEPROM Segments

Segment name	Segment range (word addresses)	Description
Melexis area	0x8000 – 0x8013	Melexis calibration data
Patch0 start address	0x8014	start address and enable bit for firmware patch 0
Patch1 start address	0x8016	start address and enable bit for firmware patch 1
User area	0x8018 – 0x809E	User data
Patch0 area	0x80A0 – 0x80AE	Patch0
Patch1 area	0x80B0 – 0x80BE	Patch1

The using of firmware patches is optional but recommended. In case no firmware patch is used, these areas can be used for user data.

4.4.3. Write Timing

The EEPROM requires a 5ms delay for write and erase operations. This is generated from a 250 KHz internal clock. A write or erase access to the EEPROM starts a 5ms delay period that can be monitored by either polling port bit EE_BUSY or waiting for the interrupt EE_IT.

Note:
While the EEPROM is being written, both CPUs are still running. An attempt to read or write to EEPROM by Mlx16 while it is busy generates an exception interrupt.

4.4.4. Read timing

The read access time of the EEPROM is 4 clock periods. This delay is created using the master clock.

4.4.5. Read

A read is done “on the fly” by adding wait states in the instruction.

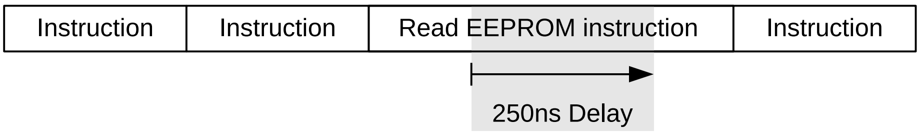


Figure 4 - EEPROM read

4.4.6. Write/Erase

The MLx16 supports 2 operations: Read and Write, while EEPROM requires 3 operations: Read, Write, and Erase. EEPROM Write and Erase are both accomplished by an Mlx16 write instruction.
As write and erase delays are long, the Mlx16 does not delay its instruction till completion. A specific hardware buffers address and data and the CPU continues its execution while the write/erase is ongoing.
The CPU has 2 options to know when the write/erase delay is terminated. It can either poll bit EE_BUSY (0 when not busy, 1 when busy) for a 0 value, or it can enable interrupt EE_IT that will be triggered when EE_BUSY goes from 1 to 0.

In order to minimize the risk of erroneous write/erase of the EEPROM, those accesses are only possible in system mode, e.g. application should call a secure system function to erase or write.

Since some applications require the EEPROM should never be written there is an extra protection for the EEPROM. The system port CONTROL has a bit EN_EEPROM_WE (0 at reset) that must be set to enable write and erase, or else the operation is cancelled and a protection interrupt is generated.

EEPROM Control register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE001	**EEPROM**	EE_BUSY	Reserved	Reserved	Reserved	Reserved	Reserved	EE_CTL[1]	EE_CTL[0]

EE_BUSY Will be always high in case there is a write process running
EE_CTL[1:0] Controls the EEPROM read and write mode
- 00 Write
- 01 Erase
- 10 Block write, write access to any EEPROM address will overwrite the complete EEPROM
- 11 Block erase, write access to any EEPROM address will reset the complete EEPROM to 1

System Control register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE000	**CONTROL**	Reserved	EEPROM_ WE	OUTC_WE	OUTB_WE	OUTA_WE	Reserved	HALT	M4_PORB

EEPROM_WE Write enable bit EERPOM
- 1 = EEPROM content can be changed
- 0 = EEPROM content can **not** be changed

OUTC_WE Write enable bit
- 1 = ANA_OUTC can be changed
- 0 = ANA_OUTC can **not** be changed

OUTB_WE Write enable bit
- 1 = ANA_OUTB can be changed
- 0 = ANA_OUTB can **not** be changed

OUTA_WE Write enable bit
- 1 = ANA_OUTA can be changed
- 0 = ANA_OUTA can **not** be changed

HALT Writing to the bit will halt the MLX16
M4_PORB Mlx4 Reset: Writing to the bit resets the MLX4

System Various register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE000	**VARIOUS**	EE_DED	EE_SEC	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

EE_DED EEPROM double-error detection
1 = EEPROM double-error detected
0 = EEPROM double-error **not** detected

EE_SEC EEPROM single-error correction
1 = EEPROM single-error detected and corrected
0 = EEPROM single-error **not** detected

4.5 OTP (MLX80105 only)

The MLX80105 has integrated 16Kbyte OTP. This area is used by both CPUs. The LIN Task + LIN API use 5kbytes while the rest (11kbytes) is available for the application running on the MLX16

Each CPU has is own separate program code in the OTP area but there is no specific mechanism to isolate them. The linker program merges the two programs and verifies that there is no overlapping, but if at execution time an error causes one CPU to jump into the code of the other one, it will of course execute unpredictable instructions and this situation will be detected either by watchdog overflow or protection error.

From the functional point of view the MLX80104 (ROM) behaves the same as the MLX80105 (OTP).

5. IO Registers

5.1 General

There are 2 port spaces for the Mlx16:

- System protected ports (starting at address 0xE000), Mlx16 bit USER must be cleared.
- User ports (starting at address 0xC000), not protected, Mlx16 bit USER must be set.

The Mulan port map has an open window of 16 bytes of custom user ports and of 12 bytes of custom system ports (not included in Mulan). Reading to non existing custom ports will have no effect and reading from non existent custom ports will always return 0.

5.2 System Protected ports

Table 7 shows the available system ports. All of these ports are system protected, meaning they are only accessible with bit USER=0. All of these registers are located outside of the IO-Segment.

Name	Address	Access Mode	Description	Page
MLX	0xE02F	Byte	MLX Reserved	
SEL_XTAL	0xE02E	Word/Byte	Selection of internal/external Oscillator	43
MLX	0xE02D	Byte	MLX Reserved	
STATUS	0xE02C	Word/Byte	Wakeup Source and central pull up/down input comparator	27
SW_IN_H	0xE02B	Byte	SW8..9 Input comparator	28
SW_IN_L	0xE02A	Word/Byte	SW0..7 Input comparator	28
IO_IN	0xE029	Byte	IO0..8 Input comparator	29
IO_AWD	0xE028	Word/Byte	Watchdog Acknowledge	44
IO_IRQ	0xE027	Byte	Interrupt source of IO generated interrupts	29
IO_EN	0xE026	Word/Byte	Enable IO pins	29
IO_INT_ENF	0xE025	Byte	Enable IO interrupt on falling edges	29
IO_INT_ENR	0xE024	Word/Byte	Enable IO interrupt on rising edges	29
MLX	0xE023	Byte	MLX Reserved	
MLX	0xE022	Word/Byte	MLX Reserved	
ANA_OUTC_H	0xE021	Byte	ADC reference calibration	68
ANA_OUTC_L	0xE020	Word/Byte	RC Oscillator trimming, enable external system clock source	68
ANA_OUTB_H	0xE01F	Byte	Current references and bandgap trimming, slew rate LIN transceiver	68
ANA_OUTB_L	0xE01E	Word/Byte	Switch current source trimming, VDDD and VDDA trimming	68
ANA_OUTA_H	0xE01D	Byte	Setting EEPROM write delay, timer controlled wake up enable	68
ANA_OUTA_L	0xE01C	Word/Byte	Power down enable LIN transceiver	68
PATCH3_A_H	0xE01B	Byte	4th Patch start address high byte, patch enable	70
PATCH3_A_L	0xE01A	Word/Byte	4th Patch start address low byte	70
PATCH2_A_H	0xE019	Byte	3rd Patch start address high byte, patch enable	70
PATCH2_A_L	0xE018	Word/Byte	3rd Patch start address low byte	70
PATCH1_A_H	0xE017	Byte	2nd Patch start address high byte, patch enable	70
PATCH1_A_L	0xE016	Word/Byte	2nd Patch start address low byte	70
PATCH0_A_H	0xE015	Byte	1st Patch start address high byte, patch enable	70
PATCH0_A_L	0xE014	Word/Byte	1st Patch start address low byte	70

Name	Address	Access Mode	Description	Page
PATCH3_I_H	0xE013	Byte	4th Patch jump instruction high byte	70
PATCH3_I_L	0xE012	Word/Byte	4th Patch jump instruction low byte	70
PATCH2_I_H	0xE011	Byte	3rd Patch jump instruction high byte	70
PATCH2_I_L	0xE010	Word/Byte	3rd Patch jump instruction low byte	70
PATCH1_I_H	0xE00F	Byte	2nd Patch jump instruction high byte	70
PATCH1_I_L	0xE00E	Word/Byte	2nd Patch jump instruction low byte	70
PATCH0_I_H	0xE00D	Byte	1st Patch jump instruction high byte	70
PATCH0_I_L	0xE00C	Word/Byte	1st Patch jump instruction low byte	70
MLX	0xE00B	Byte	MLX reserved	
MLX	0xE00A	Word/Byte	MLX reserved	
PEND_H	0xE009	Byte	Pending Interrupts high byte	53
PEND_L	0xE008	Word/Byte	Pending Interrupts low byte	53
MASK_H	0xE007	Byte	Interrupt mask high byte	53
MASK_L	0xE006	Word/Byte	Interrupt mask low byte	53
PRIO_H	0xE005	Byte	Interrupt priority high byte	53
PRIO_L	0xE004	Word/Byte	Interrupt Priority low byte	53
SHRAMH	0xE003	Byte	Upper limit for the RAM not accessible by MLX16	
SHRAML	0xE002	Word/Byte	Lower limit for the RAM not accessible by MLX16	
EEPROM	0xE001	Byte	EEPROM control register	19
CONTROL	0xE000	Byte	System control register	19

Table 7 - System Protected Ports Overview

5.3 Standard ports

Table 8 shows the available system ports. All of these ports are system protected, meaning they are only accessible with bit USER=1. All of these registers are located outside of the IO-Segment.

Name	Address	Access Mode	Description	Page
MLX	0xC01F	Byte	MLX reserved	
MLX	0xC01E	Word/Byte	MLX reserved	
SW_CONFIG	0xC01D	Byte	Current configuration central current source, IREF enable	27
S3H	0xC01C	Word/Byte	IO pin open drain enable (S3)	29
S2H	0xC01B	Byte	IO pin central current source pull down enable (S2)	27
S1H	0xC01A	Word/Byte	IO pin central current source pull up enable (S1)	27
S3L_H	0xC019	Byte	SW8..9 pin open drain enable (S3)	28
S3L_L	0xC018	Word/Byte	SW0..7 pin open drain enable (S3)	28
S2L_H	0xC017	Byte	SW8..9 pin central current source pull down enable (S2)	27
S2L_L	0xC016	Word/Byte	SW0..7 pin central current source pull down enable (S2)	27
S1L_H	0xC015	Byte	SW8..9 pin central current source pull up enable (S1)	27
S1L_L	0xC014	Word/Byte	SW0..7 pin central current source pull up enable (S1)	27
PWM_DATA_READ	0xC013	Byte	PWM duty cycle value (read only)	
PWM_DATA_WRITE	0xC012	Word/Byte	PWM duty cycle write register	
PWM_AD	0xC011	Byte	PWM channel selection	57
PWM_CTL	0xC010	Word/Byte	PWM configuration register	58
MLX	0xC00F	Byte	MLX reserved	
MLX	0xC00E	Word/Byte	MLX reserved	
MLX	0xC00D	Byte	MLX reserved	
MLX	0xC00C	Word/Byte	MLX reserved	
ADC_IN_H	0xC00B	Byte	ADC result high byte	50
ADC_IN_L	0xC00A	Word/Byte	ADC result low byte	50
ADC_CTL_H	0xC009	Byte	ADC reference voltage and channel selection	50
ADC_CTL_L	0xC008	Word/Byte	ADC configuration and status	50
TIMER_H	0xC007	Byte	Timer register high byte, Timer enable	60
TIMER_L	0xC006	Word/Byte	Timer register low byte	60
XIN	0xC005	Byte	Thermal error	66
WTG	0xC004	Word/Byte	Digital Watchdog tag register	47
WDCTRL	0xC003	Byte	Digital watchdog control register	
WDT	0xC002	Word/Byte	Digital Watchdog timeout register	
VER	0xC001	Byte	Hardware revision	
VARIOUS	0xC000	Word/Byte/Bit	System status	

Table 8 - Standard Ports Overview

6. IO Ports

The MLX80104/5 contains two types of ports. All of them are proof to battery voltage.
In case of ECU loss of battery (LOB) and a short of the wiring harness to an external supply line the MLX80104/5 will be reverse powered. Please refer to chapter "Operating under Disturbance".

6.1 Common Features of Pin SWx and IOx

The ports *SW0..9* as well as the ports *IO0..7* allow a very flexible control of up to 18 single switches or a switch matrix or any combination of both, supplied by an internal current source of typically >7mA. The switch control is sequential and periodical, so that only one port will be supplied at the same time.
If switches are placed outside and connected via a wiring harness to the ECU the MLX80104/5 allows full diagnosis of short circuits or broken line.
All ports provide a programmable wake up function and a 10mA open drain low side switch (matrix row connection to GND).
If ports are not used for switch detection, they can be configured passive (tristate behaviour) or as general purpose 10mA open drain output with port monitor. The input thresholds are compatible to 3.3V/5V supply systems. The accuracy of the input threshold allows a monitoring of external voltages without ADC. It allows connection of external supplied encoders, halls or similar.
Furthermore this architecture supports driving of logic output signals for other ECU components via an external pull up resistor as well as the driving of high side or low side loads by providing base current for an external pnp transistor.

6.1.1. Pin structure

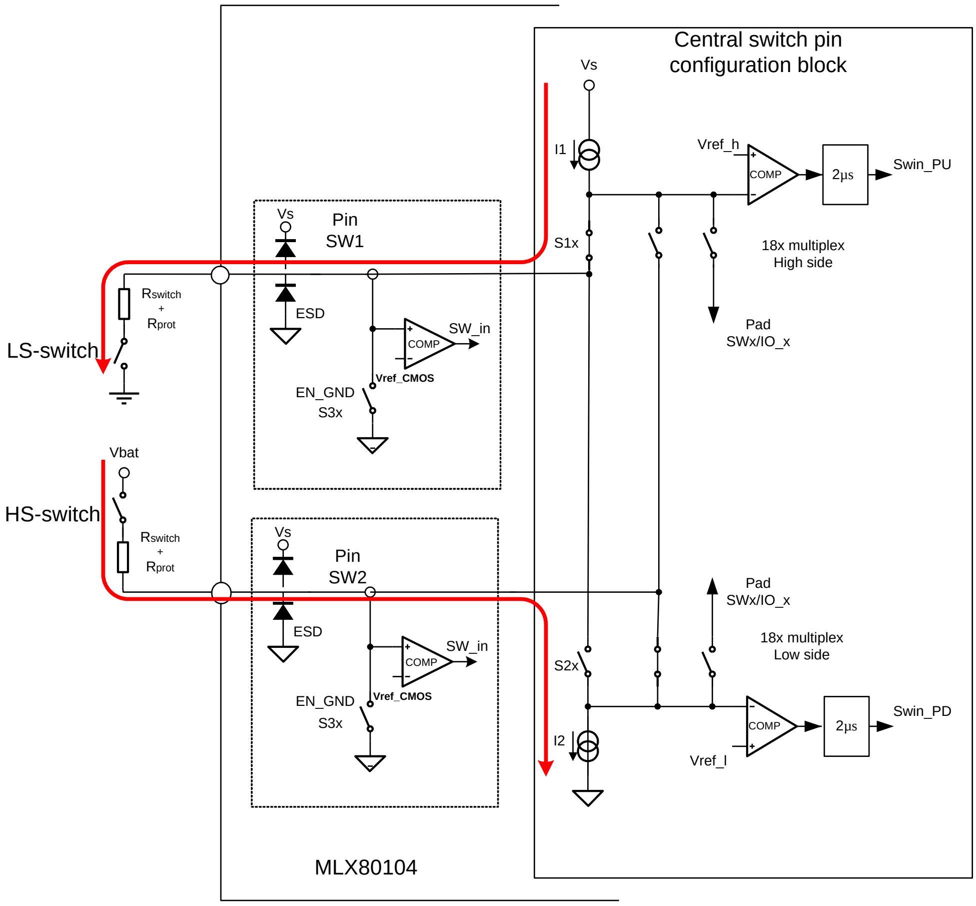


Figure 5 - Common pin Structure SWx and IOx

Figure 5 illustrates the basic structure and control of the ports for switch detection.

The default configuration of all ports after power on or wake up is tristate. After the initialisation procedure the ports will be configured by the MCU. The pull up or pull down current is provided by two central current sources I1 and I2. The currents for switch control have to be applied sequentially by the multiplex switches S1x or S2x. If a low impedance path to Ground is required (open drain buffer or matrix mode row connection), the local switch S3x has to be used.
Because of the multiplex principle only two comparators are required to detect the port input voltage levels. For RF interference as well as suppression of automotive disturbances the comparator path contains a debounce filter of typically 2µs.

The multiplex switches S1, S2 as well as the local open drain buffer S3 are controlled by the registers S3H and S3L.

6.1.2. Configuration Register Central Current Source

Status Register pull up/down input comparator – System protected port

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE02C	**STATUS**	-	-	WAKEUP_ ERROR	INTERNAL_ WAKEUP	LOCAL_ WAKEUP	BUS_ WAKEUP	SWIN_PU	SWIN_PD

WAKEUP_ERROR	Will be set if during change to sleep mode a switch state change is detected
INTERNAL_WAKEUP	Wakeup event generated from the internal timer
LOCAL_WAKEUP	Wakeup event generated from a wakeup configured SWx or IOx pin
BUS_WAKEUP	Wakeup event generated from the LIN bus
SWIN_PD	Input comparator of central current source pull down
SWIN_PU	Input comparator of central current source pull up

Central current source configuration

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC01D	**SW_CONFIG**	-	-	-	-	IREF_EN	DIAG_S2	DIAG_S1	-

IREF_EN	Switch IREF PIN on/off (0=off)
DIAG_S2	Configure central pull down current source to 10..20% of nominal value for switch diagnosis
DIAG_S1	Configure central pull up current source to 10..20% of nominal value for switch diagnosis

Central current source enable register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC01B	**S2H**	IO7_S2	IO6_S2	IO5_S2	IO4_S2	IO3_S2	IO2_S2	IO1_S2	IO0_S2
0xC01A	**S1H**	IO7_S1	IO6_S1	IO5_S1	IO4_S1	IO3_S1	IO2_S1	IO1_S1	IO0_S1
0xC017	**S2L_H**	-	-	-	-	-	-	SW9_S2	SW8_S2
0xC016	**S2L_L**	SW7_S2	SW6_S2	SW5_S2	SW4_S2	SW3_S2	SW2_S2	SW1_S2	SW0_S2
0xC015	**S1L_H**	-	-	-	-	-	-	SW9_S1	SW8_S1
0xC014	**S1L_L**	SW7_S1	SW6_S1	SW5_S1	SW4_S1	SW3_S1	SW2_S1	SW1_S1	SW0_S1

IOx_S2	Enable central pull down current source for IOx (S2) – See Figure 5
IOx_S1	Enable central pull up current source for IOx (S2) – See Figure 5
SWx_S2	Enable central pull down current source for SWx (S2) – See Figure 5
SWx_S1	Enable central pull up current source for SWx (S2) – See Figure 5

6.1.3. Configuration Register SWx

Open drain output configuration register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC019	**S3L_H**	-	-	-	-	-	-	SW9_S3	SW8_S3
0xC018	**S3L_L**	SW7_S3	SW6_S3	SW5_S3	SW4_S3	SW3_S3	SW2_S3	SW1_S3	SW0_S3

SWx_S3 Enables open drain transistor at SWx pin (S3) – See Figure 5

Input comparator register – System protected ports

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE02B	**SW_IN_H**	-	-	-	-	-	-	SW_IN9	SW_IN8
0xE02A	**SW_IN_L**	SW_IN7	SW_IN6	SW_IN5	SW_IN4	SW_IN3	SW_IN2	SW_IN1	SW_IN0

SW_INx Input comparator of pin SWx

6.1.4. Configuration Register IOx

Open drain output configuration register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC01C	**S3H**	IO7_S3	IO6_S3	IO5_S3	IO4_S3	IO3_S3	IO2_S3	IO1_S3	IO0_S3

IOx_S3 Enables open drain transistor at IOx pin (S3) – See Figure 5

Input comparator register – System protected ports

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE029	**IO_IN**	IO7_IN	IO6_IN	IO5_IN	IO4_IN	IO3_IN	IO2_IN	IO1_IN	IO0_IN
0xE026	**IO_EN**	IO7_EN	IO6_EN	IO5_EN	IO4_EN	IO3_EN	IO2_EN	IO1_EN	IO0_EN

IOx_IN Input comparator of pin IOx
IOx_EN Enables IOx input comparator

Interrupt register – System protected ports

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE027	**IO_IRQ**	IO7_IRQ	IO6_IRQ	IO5_IRQ	IO4_IRQ	IO3_IRQ	IO2_IRQ	IO1_IRQ	IO0_IRQ
0xE025	**IO_INT_ENF**	IO7_INTF	IO6_INTF	IO5_INTF	IO4_INTF	IO3_INTF	IO2_INTF	IO1_INTF	IO0_INTF
0xE024	**IO_INT_ENR**	IO7_INTR	IO6_INTR	IO5_INTR	IO4_INTR	IO3_INTR	IO2_INTR	IO1_INTR	IO0_INTR

IOx_IRQ Interrupt source of external interrupt
IOx_INTF Enables falling edge interrupt on IOx
IOx_INTR Enables rising edge interrupt on IOx

6.1.5. Switch current generation

The switch level detection is limited by the following criteria:

- Battery voltage range of 5…27V
- GND or VBAT shift < 0.1*Vs max.
- Applied current >7mA
- For switch matrix mode the voltage drop via the internal GND switch (S3) has to be lower than or equal to the maximum GND shift voltage for a low side input switch
- Contact resistance of the switch up to 1KΩ
- Internal voltage drops (On - resistance of multiplex switches, impedance of the current source, supply wiring resistance)
- Failure diagnosis for switches placed outside

In order to meet these requirements, the switch current has to be a function of the battery voltage and must be limited for battery voltages higher than 14V:

Figure 6 - Voltage dependency of the switch current

For normal battery operation voltages of 13..14V, a minimum current of >7mA can be guaranteed.
In case of higher battery voltages the current will be limited to <10mA.

6.1.6. The switch detection thresholds

LS – switch

	Vbat 14V	Vbat 7V
Injection current (calibrated)	8mA	3.5mA
GND shift(0.1*Vbat)	1.4V	0.7V
Drop switch (1kΩ)	8V	3.5V
Drop S1(300Ω)	2.4V	1.05V
Drop current source I1	1V	0.5V
Supply voltage Vs	13V	6V

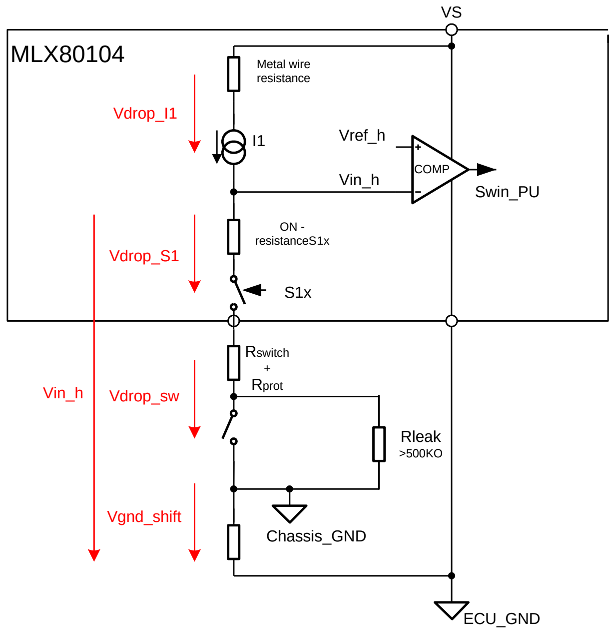


Figure 7 - Voltage drops external LS switch

Switch closed: (maximum input low voltage)

(1) Vin_h = Vgnd_shift + Vdrop_sw + Vdrop_S1
(2) Vin_h < VS – Vdrop_I1 < Vref_h

Switch open: (minimum input high voltage)

(3) Vs > Vin_h = I1 * Rleak > Vref_h

These conditions will be met by Vref_h = 0.9*VS

Switch matrix

	Vbat 14V	Vbat 7V
Injection current (calibrated)	8mA	3.5mA
Drop S3(175Ω)	1.4V	0.6V
Drop switch (1kΩ)	8V	3.5V
Drop S1(300Ω)	2.4V	1.05V
Drop current source I1	1V	0.5V
Supply voltage Vs	13V	6V

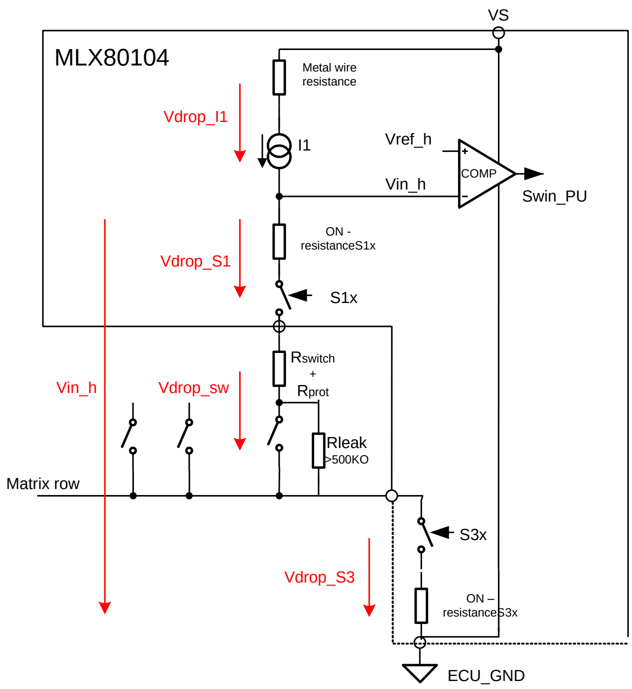


Figure 8 - Voltage drops switch matrix

Switch closed: (maximum input low voltage)

(1) Vin_h = Vdrop_S3 + Vdrop_sw + Vdrop_S1
(2) Vin_h < VS – Vdrop_I1 < Vref_h

Switch open: (minimum input high voltage)

(3) Vs > Vin_h = I1 * Rleak > Vref_h

These conditions will be met by Vref_h = 0.9*VS

HS – switch

	Vbat 14V	Vbat 7V
Injection current (calibrated)	8mA	3.5mA
Vbat shift(0.1*Vbat)	1.4V	0.7V
Drop switch (1kΩ)	8V	3.5V
Drop S2(300Ω)	2.4V	1.05V
Drop current source I2	1V	0.5V
Supply voltage Vs	13V	6V

Switch closed: (minimum input high voltage)

(1) Vbat-Vin_I = Vdrop_S2 + Vdrop_sw + Vbat_shift
(2) Vbat-Vin_I < Vdrop_I2 > Vref_I

Switch open: (maximum input low voltage)

(3) 0< Vbat-Vin_I = Vbat –(I2 * Rleak) < Vref_I

These conditions will be met by Vref_I = 0.1*VS

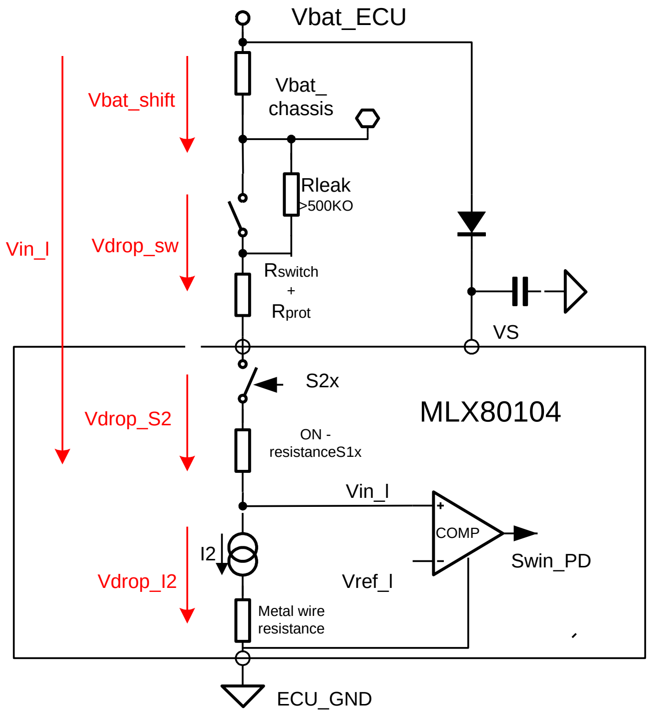


Figure 9 - Voltage drops external HS switch

Parameters of input switches

Closed switch threshold resistance (including optional protection resistor)	Rin_max	< 1175Ω
Closed switch threshold resistance (including optional protection resistor and maximum battery or GND shift)	Rin_max_ext	< 1000Ω
Protection resistor for external switches	Rprot	>100 Ω
Protection capacitor for external switches	Cprot	0…10nF

6.1.7. Switch diagnosis

If switches are connected via a wiring harness outside the ECU some failure states has to be considered:

- Short circuit to battery
- Short circuit to GND
- Short circuit to other switches
- Break of wires in the harness

For diagnosis the current sources I1 as well as I2 can be configured to 10..20% of the normal current value. Assuming the same worst case conditions as used for the switch detection level calculation, the diagnosis current allows the detection of up to 7.5kΩ resistance in the switch path.

Low side switch

Table 9 - Logic table for detection of LS input switches

Error Condition	Closed Switch	Open Switch	Broken Wire	Short to battery	Short to GND	Short to 2nd switch	SWx_S1 IOx_S1	SWx_S2 IOx_S2	DIAG_S1	DIAG_S2
SWIN_PU	1	0	0	0	1	1/0	1	0	0	0
SWIN_PD	0	0	0	0	0	0	1	0	0	0

As shown in the Table 9, a closed switch cannot be differentiated from a short vs. GND by the logic level of SWIN_PU, but if the value is stable after a certain number of cycles, a faulty closed or shorted switch can be identified.
A short to battery can be detected by using the complementary diagnosis current 10..20% * I2:

Table 10 - Logic table for diagnosis of LS input switches short vs. battery

Error Condition	Closed Switch	Open Switch	Broken Wire	Short to battery	Short to GND	Short to 2nd switch	SWx_S1 IOx_S1	SWx_S2 IOx_S2	DIAG_S1	DIAG_S2
SWIN_PU	0	0	0	0	0	0	0	1	0	1
SWIN_PD	0	0	0	1	0	1/0	0	1	0	1

If a switch Sx is shorted to another switch Sy, a diagnosis is possible by applying the injection current I1 to the first switch and a sequential scan of the other switches Sy with the diagnosis current 10..20% * I2:

Table 11 - Logic table for diagnosis of all input switches short vs. other switches by I1

Error Condition	No short	Short to 2nd Switch	+ Short to GND	+ Short to Vbat	Switch x SWx_S1/ IOx_S1	Switch x SWx_S2/ IOx_S2	Switch y SWy_S1/ IOy_S1	Switch y SWy_S2/ IOy_S2	DIAG_S1	DIAG_S2
SWIN_PU	0	0	1	0	0	1	1	0	0	1
SWIN_PD	0	1	0	1	0	1	1	0	0	1

This diagnosis additionally allows the detection of double fault conditions (short to other switch pin & short to battery or GND). For separation of double fault condition with short vs. battery the diagnosis scan has to be repeated by the opposite current configuration applying the injection current I2 to the first switch and a sequential scan of the other switches Sy with the diagnosis current 10..20% * I1:

Table 12 - Logic table for diagnosis of all input switches short vs. other switches by I2

Error Condition	No short	Short to 2nd Switch	+ Short to GND	+ Short to Vbat	Switch x SWx_S1/ IOx_S1	Switch x SWx_S2/ IOx_S2	Switch y SWy_S1/ IOy_S1	Switch y SWy_S2/ IOy_S2	DIAG_S1	DIAG_S2
SWIN_PU	0	1	1	0	0	1	1	0	1	0
SWIN_PD	0	0	0	1	0	1	1	0	1	0

The last possible fault condition of the wiring harness is a break(s) of wire(s).This fault cannot be detected by using the scan methods as described in the above tables.
By adding a resistor of 7.5kΩ±1% in parallel to the switch, an open switch can be differentiated from a switch break. For diagnosis the scan result has to be compared to a 2nd scan with the diagnosis injection current 10..20% * I1:

Table 13 - Logic table for break detection of LS input switches

Error Condition	Closed	Open	Break	Short to Vbat	Short to GND	Short to 2nd switch	SWx_S1/ IOx_S1	SWx_S2/ IOx_S2	DIAG_S1	DIAG_S2
SWIN_PU	1	1	0	0	1	1/0	1	0	1	0
SWIN_PD	0	0	0	0	0	0	1	0	1	0

High side switch

For the diagnosis of the HS – input switches the complementary configuration has to be applied:

Table 14 - Logic table for detection of HS input switches

Error Condition	Closed	Open	Break	Short to Vbat	Short to GND	Short to 2nd switch	SWx_S1/ IOx_S1	SWx_S2/ IOx_S2	DIAG_S1	DIAG_S2
SWIN_PD	1	0	0	1	0	1/0	0	0	0	0
SWIN_PU	0	0	0	0	0	0	0	0	0	0

As shown in the Table 14, a closed switch cannot be differentiated from a short to battery by the logic level of SWIN_PD, but if the value is stable after a certain number of cycles, a faulty closed or shorted switch can be identified. A short to GND can be distinguished from an open switch by using the complementary diagnosis current 10..20% * I1:

Table 15 - Logic table for diagnosis of HS input switches short vs. GND

Error Condition	Closed	Open	Break	Short to Vbat	Short to GND	Short to 2nd switch	SWx_S1/ IOx_S1	SWx_S2/ IOx_S2	DIAG_S1	DIAG_S2
SWIN_PD	0	0	0	0	0	0	1	0	1	0
SWIN_PU	0	0	0	0	1	1/0	1	0	1	0

By adding a resistor of 7.5kΩ±1% in parallel to the switch, an open switch can be distinguished from a broken wire. For diagnosis the scan result has to be compared to a 2nd scan with the diagnosis injection current 10..20% * I2:

Table 16 - Logic table for break detection of HS input switches

Error Condition	Closed	Open	Break	Short to Vbat	Short to GND	Short to 2nd switch	SWx_S1/ IOx_S1	SWx_S2/ IOx_S2	DIAG_S1	DIAG_S2
SWIN_PD	1	1	0	0	1	1/0	0	1	0	1
SWIN_PU	0	0	0	0	0	0	0	1	0	1

The short circuits vs. other switch input pins are covered by the method described in Table 14 and Table 15.

6.1.8. Switch Configuration in sleep mode

In case of a valid go to sleep condition, the following procedure must be initiated:

- All ports requesting a wake up capability will be connected in parallel by the closed switches S1x or S2x to the shared sleep comparators and the shared pull up/down resistors.

- Any permanently closed pushbutton or switch as well as ports with short circuits to battery or GND have to be *excluded* from the wake up capability, because a permanent current would be applied in sleep mode and no wake up edge detection would be possible (OR interconnection). This makes switch diagnosis mandatory before GO TO SLEEP

- Switches with parallel resistor for break diagnosis have to be *excluded* from the wake up capability because of a permanent current flow in sleep mode and an undefined shift of the wake up threshold.

- After the GO TO SLEEP command any local wake up condition will be suppressed by a sleep counter in order to insure stable conditions at any port and prevent an invalid wake up.
  The status of S1x, S2x as well as S3x (matrix rows) will be stored with the rising edge of the GO TO SLEEP command.

- In case of a changed switch status after the GO TO SLEEP timeout period the system will wake up immediately and a 'wake up error flag' will be set.

- A local wake up will be detected after a change of a switch position(s) for longer than the specified wake up filter time, the local wake up flag will be set.

- This described procedure allows a change into power saving modes even in case of failures

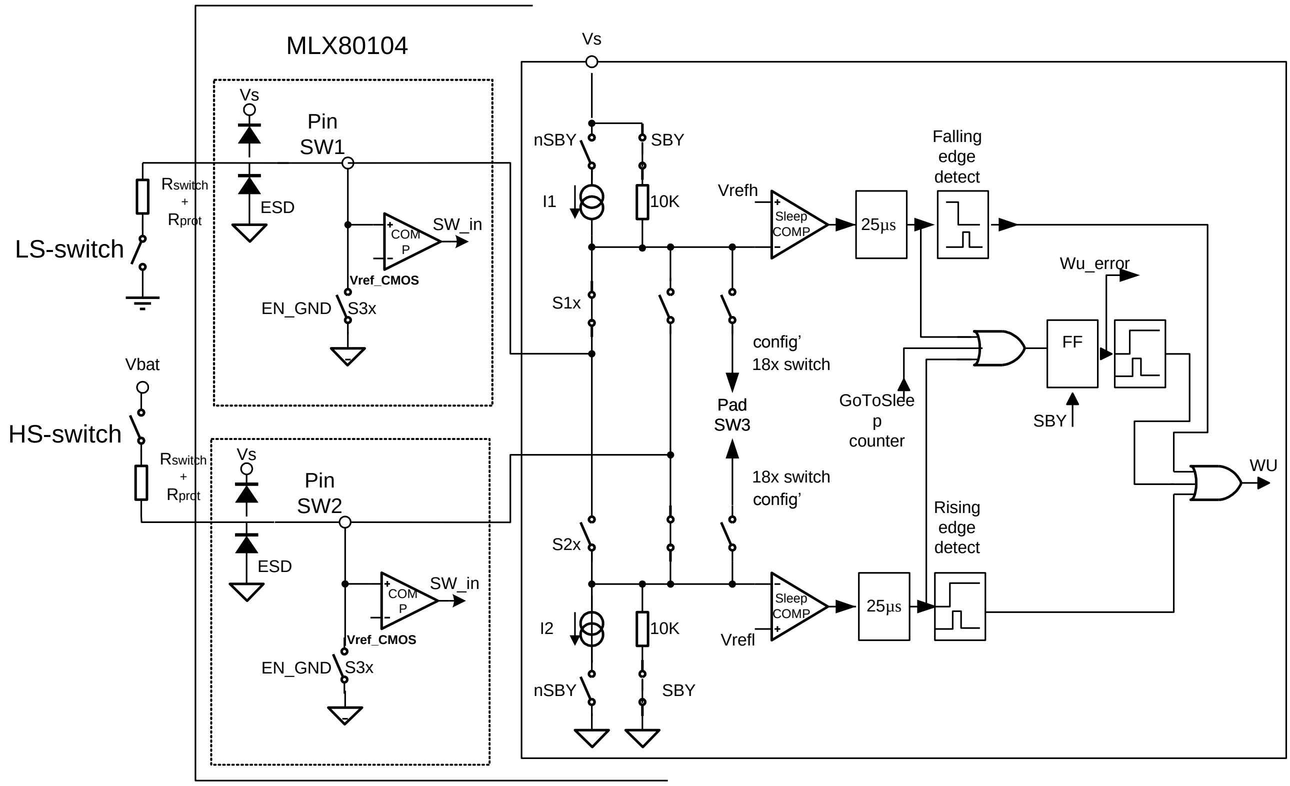


Figure 10 - Wake up detection for switch inputs

As shown in Table 17, the following sleep mode configurations are possible:

Table 17 - Sleep mode configuration overview (switch detection)

Mode	S1x	S2x	S3x	Comment
No wake up required	0	0	0	Port tristate
Wake up for LS switch	1	0	0	Internal wake up current source to Vs
Wake up fur HS switch	0	1	0	Internal wake up current source to GND
Wake up matrix columns	1	0	0	Internal wake up current source to Vs
Wake up matrix rows	0	0	1	Path to GND

6.2 Additional Operation Modes SWx Ports

Open drain output mode

The SWx pins can also be used as normal open drain outputs. This mode can be switched on via the configuration register bits. In this mode the central current source (S1x and S3x) should not be applied to the open drain configured pin.

Because of the high voltage capability of the pin the current capability can be easy extended via an external pnp-transistor.

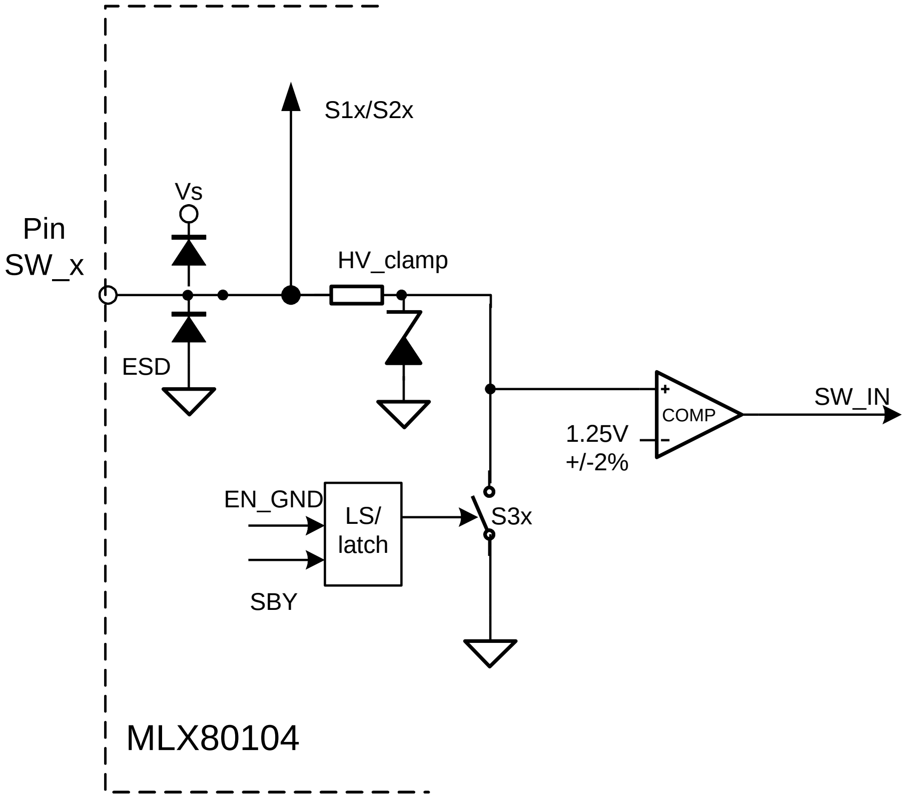


Figure 11 - Structure of SWx pins

Table 18 - Active mode configuration overview SWx pins

Mode	Register SW_Sxy			Reg. SW_CONFIG		Central current source value		Input result	Remark
	SWx_S1	SWx_S2	SWx_S3	DIAG_S1	DIAG_S2	I1	I2		
Tristate	0	0	0	x	x	x	x	-	
Central pull up current	1	0	0	0	X	100%	X	SWIN_PU	Low side switch or matrix columns
Central pull down current	0	1	0	x	0	x	100%	SWIN_PD	High side switch
Matrix row connection	0	0	1	x	x	x	x	SWIN_PU	
Diagnosis 1	1/0	1/0	0	1	0	10..20%	100%	SWIN_PU/ SWIN_PD	Switch Diagnosis
Diagnosis 2	1/0	1/0	0	0	1	100%	10..20%	SWIN_PU/ SWIN_PD	Switch Diagnosis
Digital Input	0	0	0	x	x	x	x	SW_Inx	
Open drain output	0	0	1/0	x	x	x	x	SW_Inx	

6.3 Additional Operation Modes IOx Ports

Open drain output mode

The IOx pin can also be used as normal open drain outputs. This mode can be switched on via the configuration register bits. In this mode the central current source (S1x and S3x) should not be applied to the open drain configured pin.
Because of the high voltage capability of the pin the current capability can be easy extended via an external pnp-transistor.

ADC input mode

Every IOx pin can also be used as analogue input signal for the integrated 10-bit ADC. Via the ADC_CTL register the IOx pins can be selected to be used as ADC channel. See chapter 9 Analogue to digital converter for detailed description.

Interrupt capable input

In case external events should generate an interrupt the IOx pins can also be configured as an interrupt source. The interrupt sensitivity can be configured either for the falling or for the rising or for both edges. See chapter 10 Interrupts for a detailed description.

PWM Output

The eight available PWM channels can be applied to the corresponding IOx pin via the register PWM_AD. For output of the PWM channels the pin must be configured in open drain configuration. See chapter 11 PWM Unit for a detailed description.

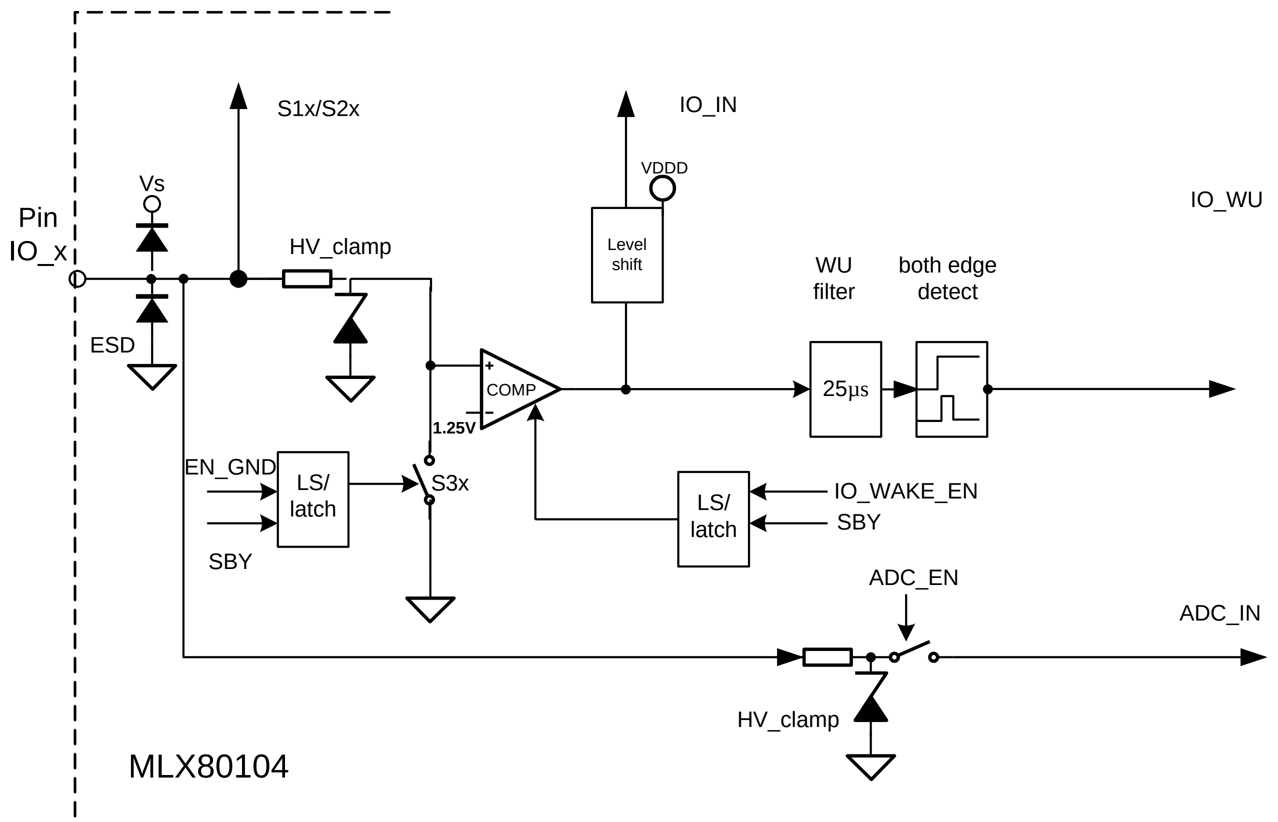


Figure 12 - Structure of IOx pins

Table 19 - Active mode configuration overview IOx pins

Mode	IOx_S1 [1]	IOx_S2 [1]	IOx_S3 [2]	IOx_EN [3]	IOx_IRQ [4]	ADCMUXx [5]	PWMx_y [6]	DIAG_S1 [7]	DIAG_S2 [7]	Input result	Remark
Tristate	0	0	0	0	x	0	0	x	x	-	
Central pull up current	1	0	0	0	x	0	0	x	x	SWIN_PU	Low side switch or matrix columns
Central pull down current	0	1	0	0	x	0	0	x	x	SWIN_PD	High side switch
Matrix row connection	0	0	1	0	x	0	0	x	x	SWIN_PU	
Diagnosis 1	1/0	1/0	0	0	x	0	0	1	0	SWIN_PU/ SWIN_PD	Switch diagnosis
Diagnosis 2	1/0	1/0	0	0	x	0	0	0	1	SWIN_PU/ SWIN_PD	Switch diagnosis
Digital Input	0	0	0	1	0	0	0	x	x	IO_INx	
Interrupt Input	0	0	0	1	1	0	0	x	x	IO_IRQx IO_INx	
ADC Input	0	0	0	0	x	1	0	x	x	ADC result	
Open drain output	0	0	1	1/0	x	0	0	x	x	IO_INx	
Open drain PWM Output	0	0	1	0	x	0	1	x	x	-	

[1] Central current source enable register
[2] Open drain output configuration register IOx
[3] Input comparator register IOx
[4] Interrupt register IOx
[5] ADC channel selection register
[6] PWM channel selection register
[7] Central current source configuration register

6.4 The IREF pin

This pin provides a calibrated pull up current from the VS supply. This output current can be used for generation of an external reference or supply voltage by using an external bipolar transistor.

An Application Note "External supply regulator using the IREF pin" is available at Softdist.

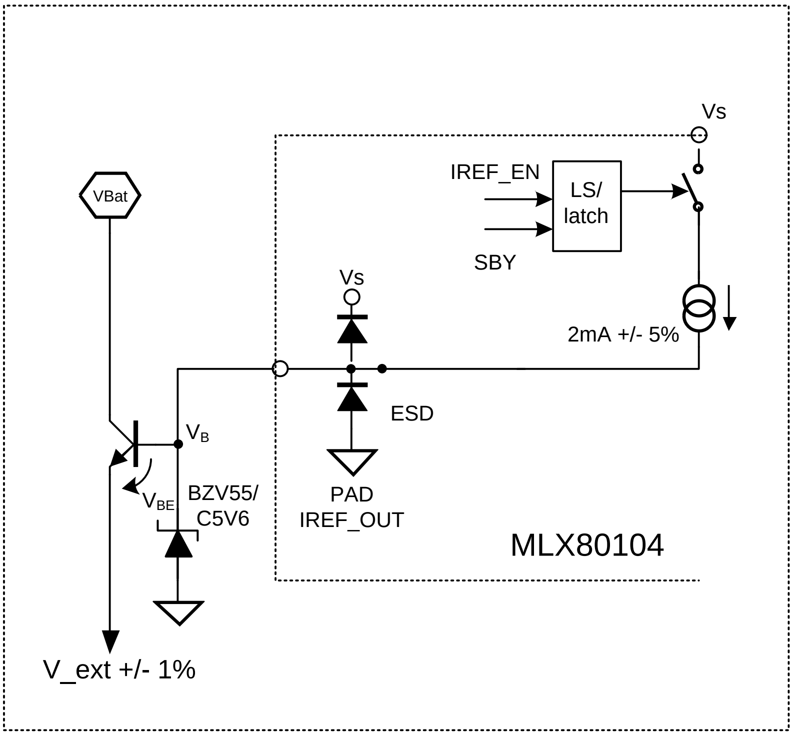


Figure 13 - Sample circuitry for IREF pin

For increasing the accuracy of the V_ext voltage at higher loads a zener diode can be placed at the base of the transistor. V_ext = V_B - V_{BE}

Via the central current source diagnose register the IREF current can be switched on/off.

The voltage at this pin can be monitored via the internal ADC channel IREF

Central current source configuration register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC01E	SW_CONFIG	-	-	-	-	IREF_EN	DIAG_S2	DIAG_S1	-

IREF_EN Switch IREF PIN on/ff (0=off)
DIAG_S2 Configure central pull down current source to 10..20% of nominal value for switch diagnosis
DIAG_S1 Configure central pull up current source to 10..20% of nominal value for switch diagnosis

7. Clock System

7.1 RC-Oscillator

The main oscillator is a 12MHz RC oscillator, which will be trimmed under software control according to the stored calibration value in the EEPROM. The frequency can be trimmed from 8MHz up to 14MHz.
After Reset the RC oscillator is calibrated with the default reset value 0x00. The RC oscillator will be calibrated during production process to 12MHz ±5%. The calibration value will be stored in the EEPROM and the software initialisation routine must set this value in the system configuration register (See 16.2 Initialising the System) after start up.

7.2 Crystal Oscillator

In case an external 12MHz resonator or crystal is connected, it is possible to select this oscillator as system clock by setting the XTAL_ON bit in the external clock source register. The loading capacitors are not a part of the IC and must be added externally.

The start-up of the IC will always be done with the internal RC Oscillator. The XTAL oscillator can be switched on and off via the SEL_XTAL register. The settling time has to be taken into account, before under software control the XTAL oscillator will be selected as system clock for the IC.

External clock source register – system protected register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE02E	**SEL_XTAL**	-	-	-	-	-	-	-	XTAL_ON

XTAL_ON	Selection of external clock source
0 = Use internal RC oscillator (reset value)
1 = Use external clock source

The clock switching will be done fully synchronous and therefore the switching doesn't generate spikes or disturbances to the CPU.

The external XTAL oscillator must be connected to IO2 and IO5. In this case, the IO2 and IO5 must be configured as tristate and can't be used for any other function.

8. Watchdog System

The MLX80104/5 is equipped with two different watchdog systems. One digital programmable window watchdog and one completely independent operating analogue Watchdog are available.

8.1 Analogue Watchdog

The analogue Watchdog is intended to fulfil application requirements where a completely independent clock source from the CPU is demanded for the watchdog system. Therefore an analogue system is used for this function.
This system is based on charging/discharging an external capacity. For definition of the watchdog time an external capacitor must be connected to the pin AWD. Together with a fixed loading current source inside of the IC, the Watchdog time can be adjusted to any application needs.

The Watchdog will be started automatically after reset. Once this has been done after the power on, the Watchdog cannot be stopped anymore. The Watchdog is stopped during sleep mode and is enabled again after every return from wakeup or power on reset.

Watchdog acknowledge register – system protected register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE028	IO_AWD	-	-	-	-	-	-	AWD_ACK	-

AWD_ACK Writing “1” Acknowledge the analogue watchdog

Writing a “1” to the AWD_ACK bit loads the external capacitor to the upper threshold and restarts the unloading time. This bit will be cleared automatically after charging of the watchdog capacity is done. Software cannot read back the value.

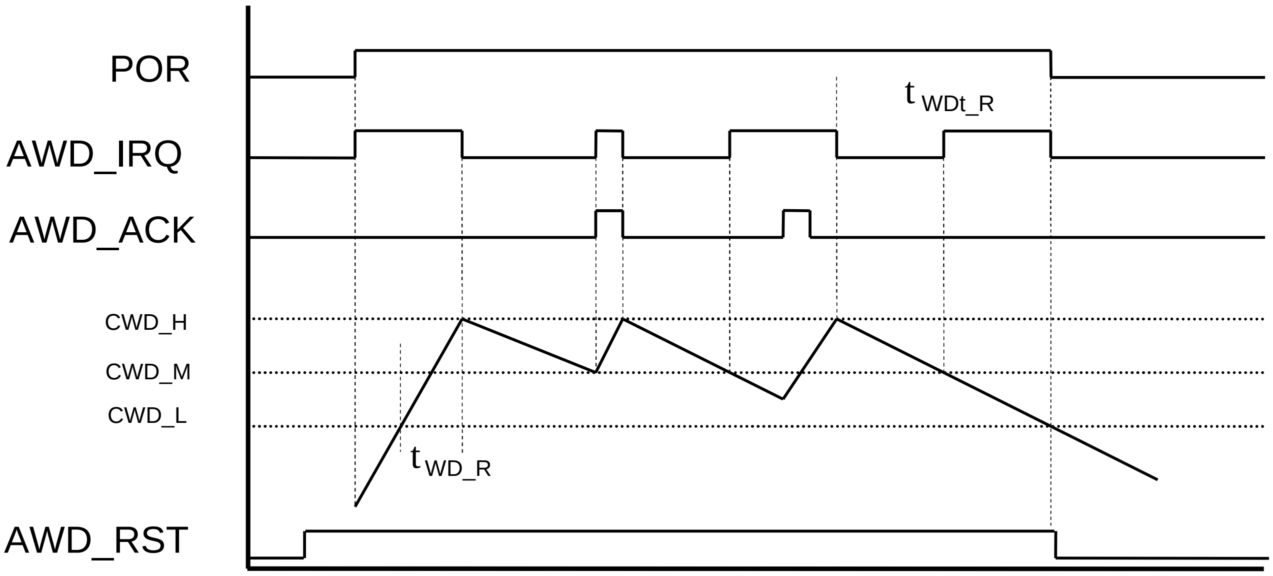


Figure 14 - Analogue watchdog behaviour

8.1.1. Using the analogue WDOG

If the Watchdog has been started by power on reset, the capacitor voltage on AWD pin ramps up until the upper voltage level is reached. After that, the current source of WDOG reverts to unload the capacitor. On half of the Watchdog time it generates precondition status information via an external watchdog interrupt request to the CPU. This request can be used to store sensitive data into non-volatile memory and to continue without restarting WDOG. It is not allowed to use this interrupt to trigger the watchdog!
The Watchdog must be acknowledged before the CWD_L voltage is reached, otherwise a system shutdown will be performed. This system shutdown ends with a POR.

8.1.2. Timing definition

The watchdog time is defined by the external capacitor connected to the AWD pin. The value of this capacitor can be calculated as follows:

t_{WDt_R} [ms] = WD[nF] and
t_{WD_R} [ms] = 0.1*WD [nF]

Example:
WD = 10nF -> t_{WDt_R} =10ms und t_{WD_R} = 1ms

The complete watchdog period will be for this example: 10ms+1ms=11ms

8.2 Digital Window Watchdog

The Mulan digital watchdog has 3 possible behaviors and is running on a 12MHz clock. It is described in the next chapters.

Important:
After reset the intelligent watchdog is disabled. Bootstrap code should enable it as needed.

Timer watchdog description

In this mode, the watchdog is a free-running up counter that can be reset by software. When it reaches a predefined timeout value, a watchdog reset is generated (RST_WD_IT). Software must therefore periodically clear this counter to avoid a CPU reset. As interrupt RST_WD_IT is also generated at power on reset, reading bit WD_BOOT of register CONTROL can be used to find out which source has generated it (WD_BOOT = 1 in case it is the watchdog).

Window watchdog description

In the window mode clearing the counter is only authorized within a time window starting at half the predefined timeout value. In case a clear is done outside the window (e.g. before half the timeout delay), a RST_WD_IT interrupt is generated (WD_BOOT = 1). At the end of the window an interrupt is generated (not a reset). That interrupt also starts a new waiting sequence which is stopped when the software clears the free-running up counter. If the software has not cleared the counter after a given time, a RST_WD_IT interrupt is generated.

Intelligent watchdog description

This watchdog operates in a completely different way. It supposes the software allocates for a given task a given provision of time and a tag. This amount of time is programmable and can be changed. The tag can represent a state of the software. Once this time is elapsed, it generates an interrupt (not a reset). The software must check if the new state of the program is coherent with the tag saved, and then reload a new couple of time and tag. The interrupt generated also starts a new waiting sequence that is cleared when the software updates the couple time and tag (i.e. when the interrupt is serviced). If the software has not updated the couple time and tag after a given time, a RST_WD_IT interrupt is generated.

8.3 Watchdog Register

Watchdog Tag Register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC004	**WD_TAG**	WD_TAG[7:0]							

WD_TAG[7:0] Tag value to be used for intelligent Watchdog mode

Watchdog Control Register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC003	**WDCTRL**	ERR	WND	MODE1	MODE0	-	-	DIV1	DIV0

ERR Watchdog access error (read only, clear on read)
WND Window Watchdog Value (read only)
MODE[1:0] Definition of Watchdog behaviour
00 Disabled
01 Timer Watchdog
10 Window Watchdoog
11 Intelligent Watchdog
DIV[1:0] Watchdoog clock divider, definition of watchdog clock (OSC=187kHz)
00 OSC/8
01 OSC/32
10 OSC/128
11 OSC/512

Watchdog Timer Register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC002	**WDT**	WDT[7:0]							

WDT[7:0] Watchdog timeout value, function depends on selected mode

9. Analogue to digital converter

9.1 General Description

The ADC10 is a 10-bit analogue-to-digital converter, which utilizes successive approximation technique with an internal sample and hold circuit.

The pins IO0 … IO7 can be used as ADC input. In addition the voltage on pin IREF and VS can be monitored via ADC. Please have a look to section 9.2 for information about the input divider.

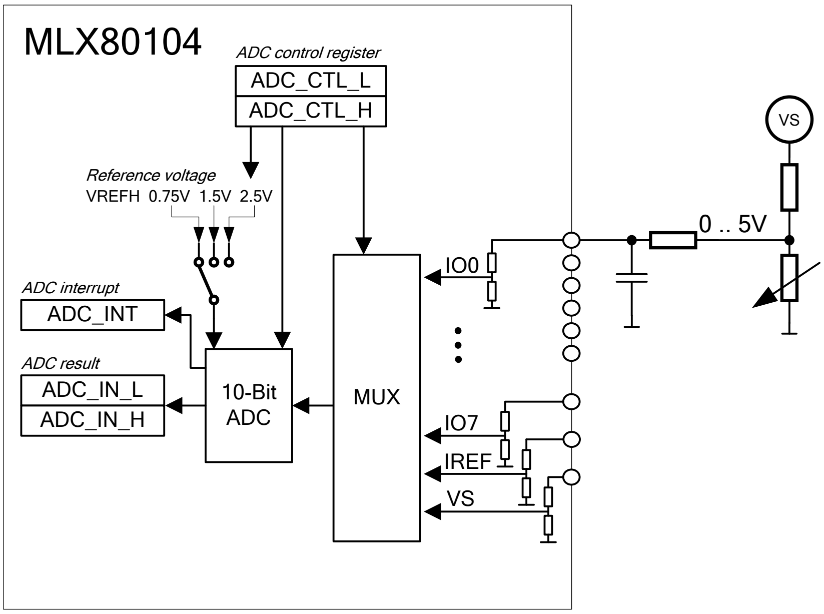


Figure 15 - ADC components

The reference voltage VREFH is based on the internal bandgap reference and is applied to the DAC after power on. In accordance to the linear input voltage range of the analogue input pins the default value of VREFH is 2.5V. To improve the maximum resolution of the measurement, the reference voltage can be adapted to VREFH=1.5V as well as 750mV. The maximum theoretical resolution (1LSB) can be calculated by

$$\text{VREFHmin} / 1024 = 0.75\text{V} / 1024 = 732\mu\text{V}.$$

9.2 Input divider

The following table illustrates the input divider on the pins, the possible maximal input voltage and resolution for the different ADC reference voltages.

Pin	Divider	Ref 0.75V		Ref 1.5V		Ref 2.5V	
		Max input voltage	Resolution	Max input voltage	Resolution	Max input voltage	Resolution
IO0..IO7	2	1.5V	732µV	3V	1.46mV	5V	2.44mV
IREF	4	3V	2.93mV	6V	5.86mV	10V	9.77mV
VS	14	10.5V	10.25mV	21V	20.51mV	35V	34.18mV

Table 20 - ADC Input divider

9.3 Accuracy of the reference

The maximum reference voltage VREFH is generated by an amplified bandgap voltage. This voltage is divided by a resistor divider with a dividing error better than 1% to generate 1.5V or 750mV as reference voltage. The value of the reference voltage can be selected by the ADC_CTL register.
The best accuracy can be calculated by:

VREFHmin +/- (MinStepsize / divider factor) = 750mV +/- 1mV

This value contains the gain and offset failure of the amplifier chain and the deviation of the resistor network. The overall deviation of the output voltage is defined by the accuracy at room temperature, the temperature gradients of the bandgap reference and the offset voltage of the amplifier (approximately +/- 1.5% from –40…150°C.) This results in a total deviation of

$$VREFH_{min} \pm (minStepsize + (1.5\% \cdot VREFH_{max})) / \text{divider factor} = 750mV \pm 16mV$$

The absolute error of the measured input voltage additionally depends on the distance of the maximum input voltage to VREFHmax.

Example:

VREFH = 750mV
V_{in_max} = 100mV (e.g. shunt measurement)

Maximum absolute error: $V_{in\_err\_max} = ((VREFH / V_{in\_max}) \times VREFH_{Tol\_max}) \pm 1LSB = \pm 2.5mV$

9.4 ADC Register

ADC result register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC00B	ADC_IN_H	-	-	-	-	-	-	ADC_R [9..8]	
0xC00A	ADC_IN_L	ADC_R [7..0]							

ADC_R Result of ADC conversion

ADC selection register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC009	ADC_CTL_H	VREF			-	ADCMUX			

VREF ADC reference voltage selection
000b off 010b 1.5V
001b 2.5V 100b 750V

ADCMUX ADC channel selection
0000b off
0001b IO0, divided by 2, 3µs sampling time
0010b IO1, divided by 2, 3µs sampling time
0011b IO2, divided by 2, 3µs sampling time
0100b IO3, divided by 2, 3µs sampling time
0101b IO4, divided by 2, 3µs sampling time
0110b IO5, divided by 2, 3µs sampling time
0111b IO6, divided by 2, 3µs sampling time
1000b IO7, divided by 2, 3µs sampling time
1001b Vs, divided by 14, 10µs sampling time, 500mV error, Switched off during standby
1010b IREF, voltage at IREF pin, divided by 4, 3µs sampling time

ADC configuration register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC008	ADC_CTL_L	BUSY	-	-	-	-	-	FAST	START

START If set it starts the ADC conversion
FAST Selection of conversion clock
0 slow clock - conversion time 10µs
1 fast clock – conversion time 5µs
BUSY ADC conversion in progress

10. Interrupts

Table 21 - shows all available interrupts in the MLX80104/5.

Column "Pos" represents the interrupt input position in the interrupt controller.
Column "Abs" represents the absolute priority of the input.
Column "Rel" represents the relative priority for inputs having an identical absolute priority.
Column "type" defines which instruction will be issued by the interrupt controller in case of interrupt.

	Priority					Ports		
Description	**Pos**	**Abs**	**Rel**	**Type**	**Notes**	**PRIO**	**MASK**	**PEND**
Reset + Watchdogs Reset	0	0	0	Jump	1,3,4			
Stack error	1	0	1	Jump	1,3,4			
Protection error	2	0	2	Call	**2**,3,4			
Invalid address	3	0	3	Call	**2**,3,4			
Program error	4	0	4	Call	**2**,3,4			
Exchange request	5	1	0	Call	3,5		MASK[0]	PEND[0]
Task reset	6	1	1	Call	3		MASK[1]	PEND[1]
Watchdog attention	7	1	2	Call			MASK[2]	PEND[2]
Mutex	8	2	0	Call			MASK[3]	PEND[3]
Signal, Handshake, Event, [Mutex]	9	5	0	Call			MASK[4]	PEND[4]
Timer	10	3-6	0	Call		PRIO[1:0]	MASK[5]	PEND[5]
ADC end of conversion	11	3-6	1	Call		PRIO[3:2]	MASK[6]	PEND[6]
End of EEPROM Write/Erase	12	3-6	2	Call		PRIO[5:4]	MASK[7]	PEND[7]
Pin change interrupt IOx	13	3-6	3	Call		PRIO[7:6]	MASK[8]	PEND[8]
External Watchdog interrupt	14	3-6	4	Call		PRIO[9:8]	MASK[9]	PEND[9]
Software interrupt	15	7	0	Call			MASK[10]	PEND[10]

Notes:
1: Abort current instruction
2: Abort current instruction ►Return is **NOT** possible
3: No disable possible
4: Priority 0 can only be reached in system mode
5: For conformance test

Table 21 - Interrupt inputs

Reminder:

The highest priority is 0 and the lowest is 7.
The absolute priority is compared to Mlx16 priority to trigger an interrupt
The relative priority is used by interrupt controller to decide between identical absolute priority interrupts fired at the same time: Lowest is issued first.

Note:

The level 0 of priority is not reachable in user mode. When Mlx16-8 sets priority to 0 in user mode, it is interpreted as priority 1 by the interrupt controller.

10.1 Interrupt vectors

Table 22 - Interrupt vectors shows the interrupt vectors table as well as the type of interrupt generated (call or jump). They all use Far Page 0 (e.g. top of the ROM). See example of Fp0 in Table 6.

	Priority				Interrupt vector	
Description	**Pos**	**Abs**	**Rel**	**Type**	**Addr**	**Name**
Reset + Watchdogs Reset	0	0	0	Jump	Fp0:80	RST_WD_IT
Stack error	1	0	1	Jump	Fp0:88	STACK_IT
Protection error	2	0	2	Call	Fp0:90	PROT_ERR_IT
Invalid address	3	0	3	Call	Fp0:98	INV_AD_IT
Program error	4	0	4	Call	Fp0:A0	PROG_ERR_IT
Exchange request	5	1	0	Call	Fp0:A8	EXCHANGE_IT
Task reset	6	1	1	Call	Fp0:B0	TASK_RST_IT
Watchdog attention	7	1	2	Call	Fp0:B8	WD_ATT_IT
Mutex	8	2	0	Call	Fp0:C0	M4_MUTEX_IT
Signal, Handshake, Event, [Mutex]	9	5	0	Call	Fp0:C8	M4_SHE_IT
Timer	10	3-6	0	Call	Fp0:D0	TIMER_IT
ADC end of conversion	11	3-6	1	Call	Fp0:D8	ADC_IT
End of EEPROM Write/Erase	12	3-6	2	Call	Fp0:E0	EE_IT
Pin change interrupt	13	3-6	3	Call	Fp0:E8	EXT0_IT
External watchdog interrupt	14	3-6	4	Call	Fp0:F0	EXT1_IT
Software interrupt	15	7	0	Call	Fp0:F8	SOFT_IT

Table 22 - Interrupt vectors

10.2 Priority port

The port PRIO defines the priority level of 4 interrupt inputs. It is divided in 4 be fields of 2 bits. The correspondence between each field value is shown on Table 23.

Priority field	Absolute Priority
00	3
01	4
10	5
11	6

Table 23 - PRIO port encoding

10.3 Interrupt mask and pending ports

A mask bit at 0 (value at reset) masks an interrupt input, while a mask bit at 1 makes it visible to the Mlx16. Note that with a mask at 0 it is still possible to check if the interrupt input is set by reading the corresponding pending bit.

The interrupt pending bit is set when the interrupt occurs, the Mlx16 cannot write into this port to simulate an interrupt. Writing in this port is used for clearing the pending bit, which discards the corresponding interrupt. As writing a 1 in any pending bit clears it while writing a 0 does nothing, you can clear one or more interrupt bits in one shot, by example writing 0x0001 in PEND port clear the interrupt 5, while writing 0x7FF clear all interrupts from 5 to 15.

Pending interrupt register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE009	**PEND_H**	-	-	-	-	-	SOFT_IT	EXT1_IT	EXT0_IT
0xE008	**PEND_L**	EE_IT	ADC_IT	TIMER_IT	M4_SHE_IT	M4_MUTEX_IT	WD_ATT_IT	TASK_RST_IT	EXCHANGE_IT

For abbreviation please see Table 22.

Interrupt mask register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE007	**MASK_H**	-	-	-	-	-	SOFT_IT	EXT1_IT	EXT0_IT
0xE006	**MASK_L**	EE_IT	ADC_IT	TIMER_IT	M4_SHE_IT	M4_MUTEX_IT	WD_ATT_IT	TASK_RST_IT	EXCHANGE_IT

For abbreviation please see Table 22.

Interrupt priority register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE005	**PRIO_H**	-	-	-	-	-	-	EXT1[1]	EXT1[0]
0xE004	**PRIO_L**	EXT0[1]	EXT0[0]	EE[1]	EE[0]	ADC[1]	ADC[0]	TMR[1]	TMR[0]

Further information can be found in Table 21.

EXT1[1:0]	Priority of *external watchdog* interrupt
EXT0[7:0]	Priority of *pin change* interrupt
EE[1:0]	Priority of *end of EEPROM Write/Erase* interrupt
ADC[1:0]	Priority of *ADC end of conversion* interrupt
TMR[1:0]	Priority of *Timer* interrupt

10.4 High level system interrupts

10.4.1. Reset interrupt and watchdogs

This interrupt is generated at power on reset or if the intelligent watchdog asks for a reset. Take care that the priority is not reset in the Mlx16, so this interrupt routine must start with instruction “MOV UPR, #0”.

10.4.2. Stack error

A stack error occurs when the Mlx16 uses the stack pointer to access an invalid or an unauthorized area. No protection error or invalid address interrupt is generated. Obviously this interrupt uses a jump and does not push the program counter into the stack.

10.4.3. Exception error

There are 3 interrupts due to software errors on the Mlx16: a protection error, an invalid address or a program error. These interrupts are at level 0, therefore you **cannot** return to the interrupted program. The program counter value pushed on the stack can **only** be used for debugging purpose. The device reaction after this failure condition must be done in the ISR and depends on the application requirements. It is possible to release a RESET, switch to sleep mode or program and endless loop to keep stable behaviour of the device.

10.4.4. Protection error

A protection error interrupt happens when the Mlx16 attempts an unauthorized access or to clear the user bit (Mlx16 M register). Here is an exhaustive list of possible causes:

- Write in user mode in the EEPROM.
- Access to EEPROM while it is busy (EE_BUSY=1).
- Write in port EEPROM while it is busy (EE_BUSY=1).
- Write in system mode in EEPROM while EN_EEPROM_WE is 0
- ADC conversion request while ADC is busy (ADC_BUSY=1)
- Write in ANA_OUTx ports while corresponding OUTx_WE bit of port CONTROL is 0.
- Write in the Mlx4 RAM private area.
- Write in user mode into a system port.
- Access error in the Intelligent Watchdog
- Clear the user bit (try to enter system mode) not after a jump or call far page.

10.4.5. Invalid address

An invalid address interrupt occurs when the Mlx16 does an invalid memory access. Here is an exhaustive list of possible causes:

- Read, write or fetch a word at an odd address
- Read, write or fetch into an unused area
- Write a byte or a bit in EEPROM
- Write a bit in a digital port supporting only word or byte.
- Fetch into port area

10.4.6. Program error

A program error occurs when the Mlx16 tries to execute an invalid Mlx16 instruction. Typically, it means that Mlx16 has an invalid value in its program counter (PC).

10.5 Debugger interrupt

This interrupt is intended to be used together with the Emulator.

10.6 Pin change Interrupt

This interrupt will be used to react on change pin IOx status. The edge sensitivity can be programmed in the interrupt register (See 6.1.4 Configuration Register IOx). For the interrupt generation, the IOx will be debounced with 3us. After the debouncing the interrupt will be generated and the interrupt request is stored for every channel in the IRQ register.

10.7 External Watchdog interrupt

This interrupt is requested if the analogue watchdog has reached half of the Watchdog time period. See chapter 8 Watchdog System for details.

10.8 Software interrupt

It is possible to trigger a low priority interrupt by software setting bit SWI of port SWI to 1 the port bit is automatically reset after one clock period, so it will always be re-read as a 0.

11. PWM Unit

11.1 General

There are 8 PWM channels available. They share a common 8 bits free running counter with an input clock being either a 750kHz clock or a 12MHz divided by a programmable divider from 1 to 64. The duty cycle for each PWM channel can be set separately via PWM data register. The available PWM channels can be output to an IOx pin in low side configuration. The selection must be done via the PWM_AD register.

To calculate the correct initialisation value for the PWM control register Equation 1 to Equation 4 are valid. Additionally, in Table 24 you will find all possible PWM frequencies and the corresponding parameters for the PWM control register.

Every IOx pin has its own PWM duty cycle register. To address this register 1st the channel must be selected via PWM channel register (0xC011). After this selection the duty cycle can be written to the PWM duty cycle register (0xC012). After this procedure, the programmed cycle will be output on IOx pin if the pin is configured as open drain output and the PWM block is enabled (Bit PWM_EN in the PWM control register 0xC010).

Because the PWM is running with the CPU frequency, the accuracy is better than ±5% of the nominal PWM frequency.

11.2 Block Diagram

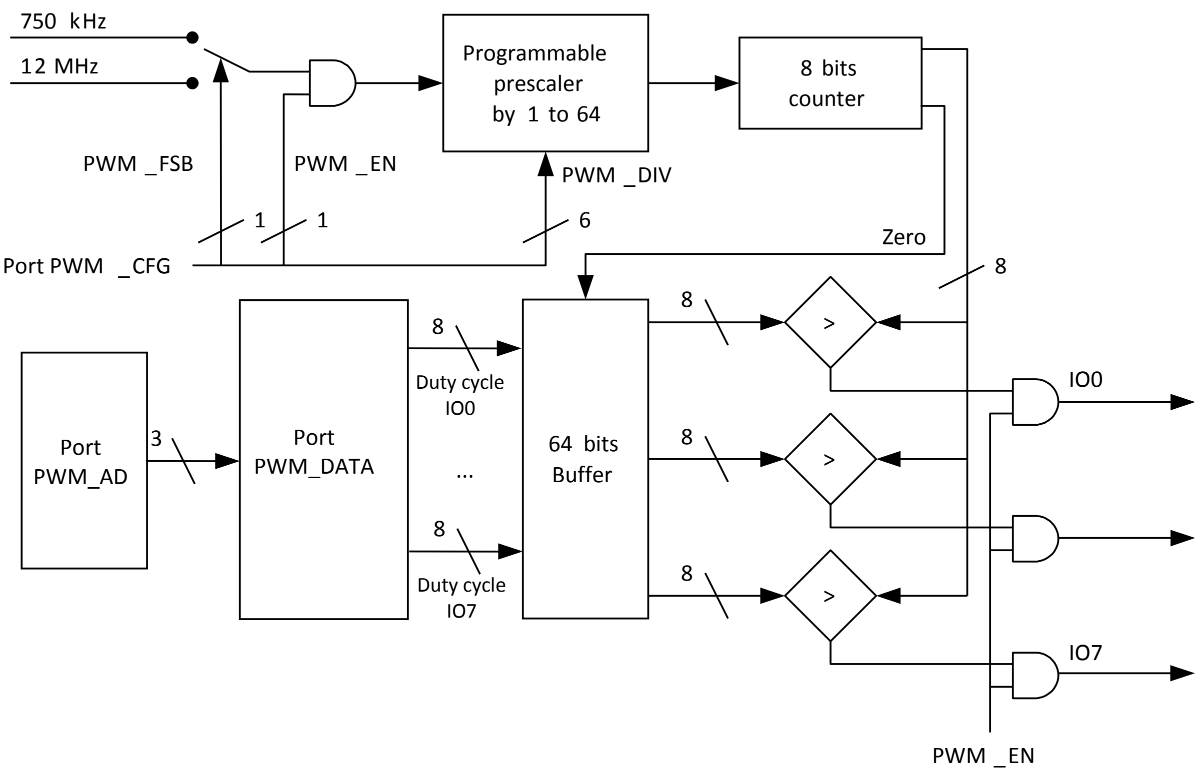


Figure 16 - PWM unit

11.3 PWM frequency calculation

Depending on the needed PWM frequency you have to choose the right equation. In case the frequency is in the range of 45Hz to 2.9kHz, Equation 3 is valid. And in case the frequency is in the range of 0.72kHz to 46kHz, Equation 4 is the right one.

$$F_{PWM}[kHz] = \frac{750kHz}{(PWM\_DIV + 1) \cdot 256}$$

Equation 1 - PWM frequency for PWM_FSB=0

$$F_{PWM}[MHz] = \frac{12MHz}{(PWM\_DIV + 1) \cdot 256}$$

Equation 2 - PWM frequency for PWM_FSB=1

$$PWM\_DIV = \frac{750kHz}{(F_{PWM}[kHz] \cdot 256)} - 1$$

Equation 3 - Parameter PWM_DIV for frequencies in the range of 45.1 .. 2929.7Hz (PWM_FSB=0)

$$PWM\_DIV = \frac{12MHz}{(F_{PWM}[MHz] \cdot 256)} - 1$$

Equation 4 - Parameter PWM_DIV for frequencies in the range of 721.2 .. 46875Hz (PWM_FSB=1)

11.4 PWM Control Register

PWM channel selection

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC011	PWM_AD	-	-	-	-		PWMSEL		

PWMSEL	000b	Address duty cycle register for IO0
	001b	Address duty cycle register for IO1
	010b	Address duty cycle register for IO2
	011b	Address duty cycle register for IO3
	100b	Address duty cycle register for IO4
	101b	Address duty cycle register for IO5
	110b	Address duty cycle register for IO6
	111b	Address duty cycle register for IO7

Duty cycle register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC012	PWM_DATA_WRITE	PWM_DATA_WRITE							
0xC013	PWM_DATA_READ	PWM_DATA_READ							

PWM_DATA_WRITE	8-bit duty cycle value for selected PWM channel (for writing new duty cycle value)
PWM_DATA_READ	For reading the current duty cycle

PWM control register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC010	**PWM_CTL**	PWM_EN	PWM_FSB	PWM_DIV					

PWM_EN Enable/Disable PWM generation
1 = Enable 0 = Disable
PWM_FSB Selection between input clock of 750kHz or 12MHz
0 = 750kHz 1 = 12MHz
PWM_DIV Programmable pre-divider 1 to 64

11.5 Available PWM Frequencies

Following PWM frequencies are configurable via the PWM Control Register PWM_CTL on page 58.

PWM Frequency in Hz	PWM_CTL [5:0]	FSB	DIV	PWM Frequency in Hz	PWM_CTL [5:0]	FSB	DIV	PWM Frequency in Hz	PWM_CTL [5:0]	FSB	DIV
45.8	0x3F	0	63	139.5	0x14	0	20	1171.9	0x28	1	39
46.5	0x3E	0	62	146.5	0x13	0	19	1201.9	0x27	1	38
47.3	0x3D	0	61	154.2	0x12	0	18	1233.6	0x26	1	37
48.0	0x3C	0	60	162.8	0x11	0	17	1266.9	0x25	1	36
48.8	0x3B	0	59	172.3	0x10	0	16	1302.1	0x24	1	35
49.7	0x3A	0	58	183.1	0x0F	0	15	1339.3	0x23	1	34
50.5	0x39	0	57	195.3	0x0E	0	14	1378.7	0x22	1	33
51.4	0x38	0	56	209.3	0x0D	0	13	1420.5	0x21	1	32
52.3	0x37	0	55	225.4	0x0C	0	12	1464.8	0x01	0	1
53.3	0x36	0	54	244.1	0x0B	0	11	1464.8	0x20	1	31
54.3	0x35	0	53	266.3	0x0A	0	10	1512.1	0x1F	1	30
55.3	0x34	0	52	293.0	0x09	0	9	1562.5	0x1E	1	29
56.3	0x33	0	51	325.5	0x08	0	8	1616.4	0x1D	1	28
57.4	0x32	0	50	366.2	0x07	0	7	1674.1	0x1C	1	27
58.6	0x31	0	49	418.5	0x06	0	6	1736.1	0x1B	1	26
59.8	0x30	0	48	488.3	0x05	0	5	1802.9	0x1A	1	25
61.0	0x2F	0	47	585.9	0x04	0	4	1875.0	0x19	1	24
62.3	0x2E	0	46	732.4	0x03	0	3	1953.1	0x18	1	23
63.7	0x2D	0	45	732.4	0x40	1	63	2038.0	0x17	1	22
65.1	0x2C	0	44	744.0	0x3F	1	62	2130.7	0x16	1	21
66.6	0x2B	0	43	756.0	0x3E	1	61	2232.1	0x15	1	20
68.1	0x2A	0	42	768.4	0x3D	1	60	2343.8	0x14	1	19
69.8	0x29	0	41	781.3	0x3C	1	59	2467.1	0x13	1	18
71.5	0x28	0	40	794.5	0x3B	1	58	2604.2	0x12	1	17
73.2	0x27	0	39	808.2	0x3A	1	57	2757.4	0x11	1	16
75.1	0x26	0	38	822.4	0x39	1	56	2929.7	0x00	0	0
77.1	0x25	0	37	837.1	0x38	1	55	2929.7	0x10	1	15
79.2	0x24	0	36	852.3	0x37	1	54	3125.0	0x0F	1	14
81.4	0x23	0	35	868.1	0x36	1	53	3348.2	0x0E	1	13
83.7	0x22	0	34	884.4	0x35	1	52	3605.8	0x0D	1	12
86.2	0x21	0	33	901.4	0x34	1	51	3906.3	0x0C	1	11
88.8	0x20	0	32	919.1	0x33	1	50	4261.4	0x0B	1	10
91.6	0x1F	0	31	937.5	0x32	1	49	4687.5	0x0A	1	9
94.5	0x1E	0	30	956.6	0x31	1	48	5208.3	0x09	1	8
97.7	0x1D	0	29	976.6	0x02	0	2	5859.4	0x08	1	7
101.0	0x1C	0	28	976.6	0x30	1	47	6696.4	0x07	1	6
104.6	0x1B	0	27	997.3	0x2F	1	46	7812.5	0x06	1	5
108.5	0x1A	0	26	1019.0	0x2E	1	45	9375.0	0x05	1	4
112.7	0x19	0	25	1041.7	0x2D	1	44	11718.8	0x04	1	3
117.2	0x18	0	24	1065.3	0x2C	1	43	15625.0	0x03	1	2
122.1	0x17	0	23	1090.1	0x2B	1	42	23437.5	0x02	1	1
127.4	0x16	0	22	1116.1	0x2A	1	41	46875.0	0x01	1	0
133.2	0x15	0	21	1143.3	0x29	1	40				

Table 24 - Configurable PWM Frequencies

12. Timer

The timing generation principle is shown on Figure 17.

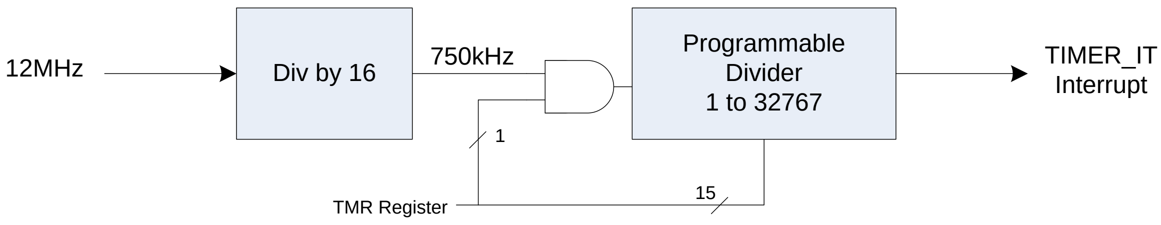


Figure 17 - Block Diagram of Timer

A 15 bits free running counter clocked by 750kHz is available to generate TIMER_IT interrupt at a rate varying from 1.33µs (TIMER [14:0] = 0) to 43.689ms (TIMER [14:0] = 32767). The timer is made of a down counting loadable binary counter. It is enabled by TMR_EN (bit 15) of TMR register. Once enabled each time it reaches 0x0000; it is reloaded by the value of TMR register TMR [14:0] and generates a TIMER_IT interrupt. Reading register TMR reads the current value of the counter when TMR_EN = 1 or an unknown value when TMR_EN = 0.

Because the timer is running with the CPU frequency, the accuracy is better than ±5% of the nominal value.

Timer Register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC007	**TIMER_H**	TMR_EN	TMR [14:8]						
0xC006	**TIMER_L**	TMR[7:0]							

TMR_EN Enable/Disable Timer
1 = Enable 0 = Disable
TMR 15-bit Timer value

12.1 Timer Calculation

The TMR value for the TIMER register can be calculated with Equation 5, where Timer_Period is the time between the timer interrupts in µs.

$$TMR[14:0] = \frac{Timer\_Period[\mu s] \cdot 12MHz}{16}$$

Equation 5 - Calculation of the TMR parameter

13. LIN Interface

13.1 The Concept

The LIN protocol is implemented on a MULAN core on the MLX4 part. The complete MLX16 part is free for the application. With this dual core architecture the bus communication is decoupled from the application. The complete LIN driver running on the MLX4 is part of the software development system and will be supported by Melexis. The communication between both CPUs is done via an API. This API uses the common RAM area for data exchange. The application task (running on MLX16) transmits all necessary LIN configuration data via the API to the LIN task (running on MLX4) during the initialization process. Further information can be found in the document "MelexCM LIN Firmware API - Programmer's Reference Manual".

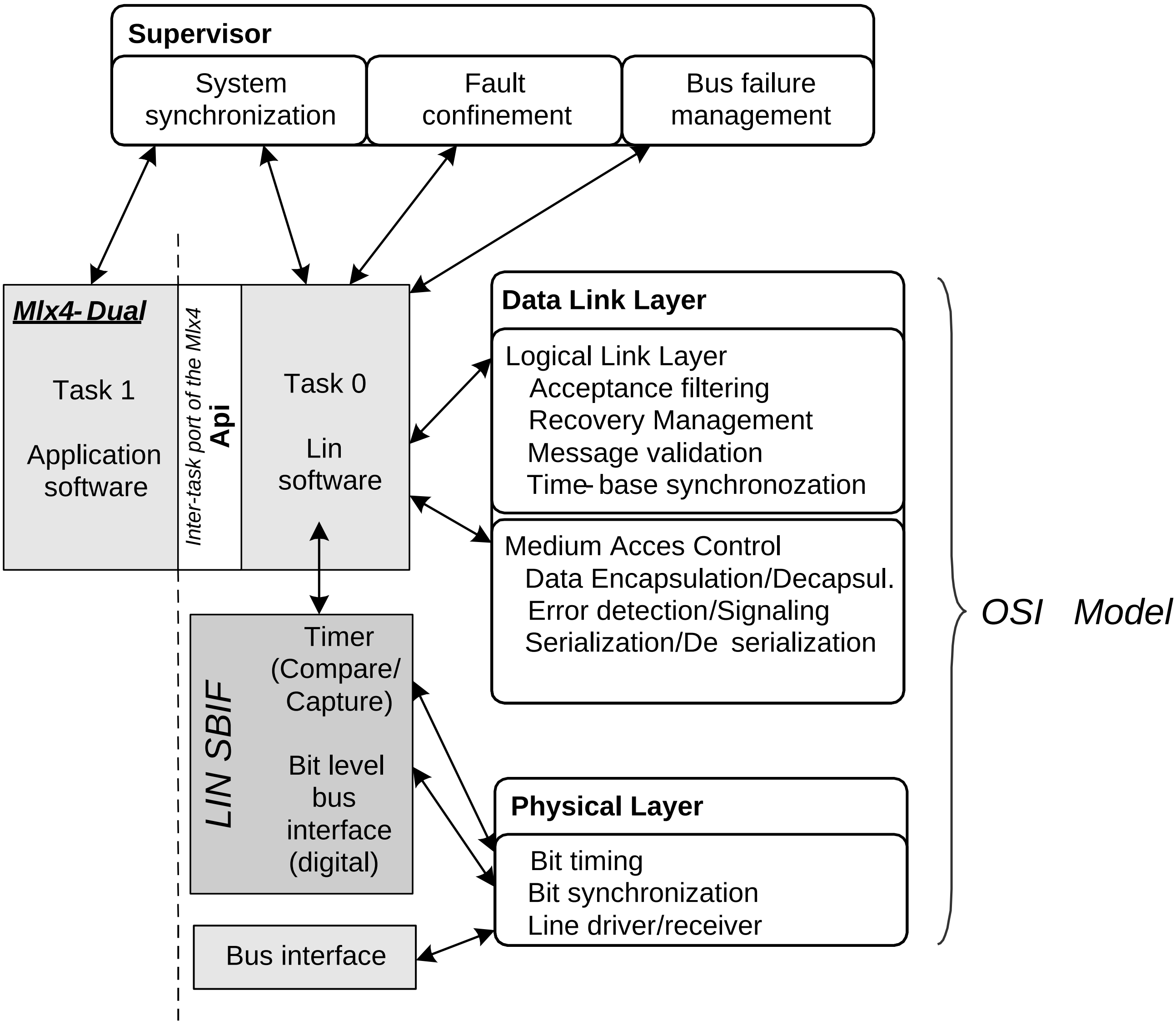


Figure 18 - LIN OSI-Reference model

13.2 LIN Physical Layer

The MLX80104/5 contains an integrated physical layer for applications of low speed vehicle serial data network communication using the Local Interconnect Network (LIN) protocol. The device is designed in accordance to the physical layer definition of the LIN Protocol Specification Package 2.x and the SAE J2602 standard. The corresponding baudrate and slew rate can be set via API commands.
The sleep mode capability allows a shutdown of the whole application. The included wake-up function detects incoming dominant bus messages and wakes up the IC.
Because of the good symmetry parameter of the transceiver the communication with RC based synchronization accuracy is possible under all worst case conditions in Vbat - or Ground shift, even in case of recessive bus voltages down to 5V.

RxD debounce

The RxD debouncing circuit and the integrated low pass filter in the receiver path prevent RxD spikes in case of RF interferences and schaffner pulses to guarantee a correct sampling of the master request.

TxD timeout

A special feature is the TxD timeout. In case of a faulty blocked TxD (MLX or LIN controller crash) the Bus output is switched off automatically after the specified TxD timeout reaction time to prevent a dominant bus. The transmission is continued by next TxD L to H transition without delay.

Undervoltage lockout

An undervoltage lockout comparator detects an unspecified decrease of the regulated supply voltage VAUX. This measurement covers both, unspecified overload on VAUX and unspecified decrease of VS. It's an additional factor of safety against undefined bus behaviour. To prevent a transmission interrupt due to Schaffner or RF modulation a debounce filter is used for spike suppression.

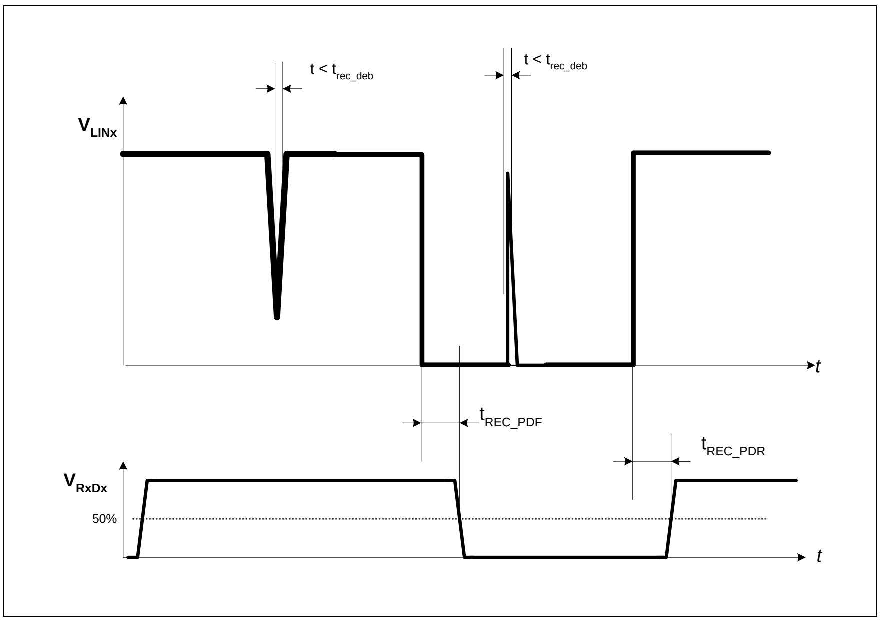


Figure 19 - Receiver debouncing & propagation delay

Duty cycle calculation LIN 2.x

With the timing parameters shown in the picture below two duty cycles , based on $t_{rec(min)}$ and $t_{rec(max)}$ can be calculated as follows : t_{Bit} =50µs **D1 =** $t_{rec(min)}$ / (2 x t_{Bit})

D2 = $t_{rec(max)}$ / (2 x t_{Bit})

Table 25 - Duty cycle measurement and calculation in accordance to LIN physical layer specification 2.x for baud rates up to 20Kbps

Duty cycle calculation J2602:

With the timing parameters shown in the table below two duty cycles , based on $t_{rec(min)}$ and $t_{rec(max)}$ can be calculated as follows : t_{Bit} =96µs **D3 =** $t_{rec(min)}$ / (2 x t_{Bit})

D4 = $t_{rec(max)}$ / (2 x t_{Bit})

Table 26 - Duty cycle measurement and calculation in accordance to LIN physical layer specification 2.x for baud rates of 10.4Kbps or below

14. Sleep Mode and Wake up System

14.1 Entering Sleep Mode by API

A valid MLX80104/5 sleep command is used to switch into the most power saving mode under software control. In this mode all unnecessary function blocks are switched off to save the maximum possible current, keeping only some minimum parts alive, which will watch events or conditions for possible wakeup requests.

To enter Sleep Mode the following sequence has to be performed: Application software first takes care of saving any needed data into non-volatile memory, because Sleep Mode will force the system to switch off power supplies. Any register content of the CPU, the content of volatile memories, etc. will be lost.
Finally a HALTED command (set “EN_HALTED” bit) has to be performed, which gives a signal to enter the sleep mode. Make sure that MLX4 is already halted otherwise the system cannot finish the power down procedure. This request starts the system shutdown process. This has to be the last action from the CPU. After sending this request the CPU has to stay in an infinite loop, waiting for system shutdown. This shutdown will be performed, even if incoming wakeup conditions should occur – which will be ignored as long as the system is not in sleep mode. This ensures that the system first shuts down and clears all CPU registers completely, to secure a defined restart into Power On state.

<u>By receiving a HALTED Signal from the CPU the following sequence is performed from the MLX80104/5 itself:</u>

- Analogue Watchdog is disabled
- All registers not required in sleep mode are cleared and contain their reset values.
- All registers containing configuration needed in sleep mode (i.e. enable bits for Wake Up sources etc.) keep their values
- The internal auxiliary supply is switched on to supply the wake-up comparators as well as the wake-up enable register

Any trimming value gets lost and must be restored within the software initialisation routine after wake-up.
The digital supply as well as the analogue supply is switched off.

In Sleep Mode all IOs will be switched to tri-state (high-impedance).

14.2 Wake Up System

There are three possible ways to wake-up the MLX80104/5:

14.2.1. LIN Bus

The LIN standby receiver detects any changing edge on the bus exceeding the wake up debouncing time of minimum 50us. The integrated filter prevents a wake up via EMC interferences.

14.2.2. Local Wake-up

The second way to wake up the slave node is a local wake up condition. The input comparators detect any changing edge exceeding the wake up thresholds and the local wake up debouncing time of minimum 20us.
Every wake up detection set a wake up flag, the bandgap reference and the voltage regulators are switched on and the power on procedure starts. The information about a local wake up is stored in the status register.

14.2.3. Internal Wake-up

The third way to wake-up is the configurable internal wake timer. After a configured time the MLX80104/5 is switched on. This mode is foreseen for observing applications with a very slow current consumption in user mode.

If local wake up capabilities are used, the leakage currents of the connected switches will increase the current consumption of the whole slave node.

15. Thermal Shutdown

A thermal overload of the MLX80104/5 may occur due to an increased power dissipation and high ambient temperature. Causes for the unspecific power dissipation may be:

- Short LIN to Vbat/Vs
- Shorted load at IO Pins
- IO loads too high

In case the chip temperature exceeds the specified limit, the THERMAL bit in the XIN register (see below) will be set to 1. This bit can be used for triggering the software to find the reason of the thermal problem. This can be done by disable SWx/IOx pins to check if the external circuitry causes the problem.

Thermal Error Bit

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC005	**XIN**	-	-	-	-	-	-	-	THERMAL

THERMAL Thermal error bit
0 = **no** thermal error
1 = Thermal error

16. System behaviour

16.1 Reset behaviour

After connecting power to the VS pin the system will start operation. The on-chip supplies start after the defined minimum voltage level is reached on the VS pin. The system is in the RESET state as long as the supply voltage is below its minimum voltage level.

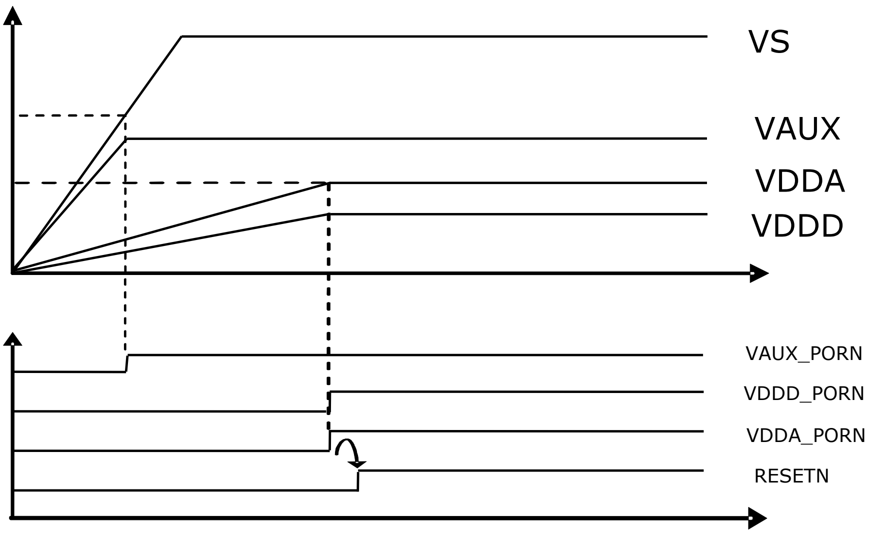


Figure 20 - Reset behaviour

The reset signal keeps the complete IC in reset state if the supply voltage is below the specified value. After reaching the minimum voltage level of the supply, the reset signal becomes inactive and the initialisation sequence is started. The RC-Oscillator is switched on with the lowest frequency and the CPU starts the initialisation.

16.2 Initialising the System

For correct system start-up some registers in the IO part must be restored after every RESET or WAKEUP by writing the values from reserved EEPROM addresses. These trim values have been stored during chip test. Overwriting these EEPROM memory addresses is prohibited otherwise the data for application needs is lost and the correct IC behaviour cannot be guaranteed in the specified range.

Start-up steps:

1. Trim the bandgap to the expected value (3bit),
2. Trim the RC to the expected frequency (7bit),
3. Trim the internal biasing to the expected current,
4. Trim the ADC reference to the expected voltage for every input range (7bit),
5. Trim the switch current (4bit),
6. Set the EEPROM delay time (4bit).

System configuration register

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE021	**ANA_OUTC_H**	reserved	ADC-REF *						
0xE020	**ANA_OUTC_L**	EN_XTAL	RC_CALI *						
0xE01F	**ANA_OUTB_H**	CU_TRIM *				reserved	BG_TRIM *		
0xE01E	**ANA_OUTB_L**	reserved				SW_TRIM *			
0xE01D	**ANA_OUTA_H**	EE_DELAY *				reserved			
0xE01C	**ANA_OUTA_L**	reserved						INT_WAKE	

EE_DELAY Set the EEPROM programming time
INT_WAKE Control of internal timer controlled wake up
- 00 off
- 01 wake up after 0.5s
- 02 wake up after 1s
- 03 wake up after 2s

BG_TRIM Adjust bandgap
CU_TRIM Adjust current references
SW_TRIM Adjust switch current source
ADC_REF Adjust reference voltage of ADC VREFH
RC-CALI RC-Oscillator calibration
EN_XTAL Enable use of external Quartz or Resonator as clock source for the MCU
- 0 internal RC-Clock is used
- 1 Switch from RC to external

Attention: All values marked with "*" are trimming values for analogue IC parameter. Those values must be kept after initialisation of the IC! Otherwise the IC will not operate correctly.

17. ROM Patches

In order to rapidly correct minor bugs in ROM a specific hardware has been added to replace up to four ROM spaces by EEPROM code. The principle is shown on Figure 21.

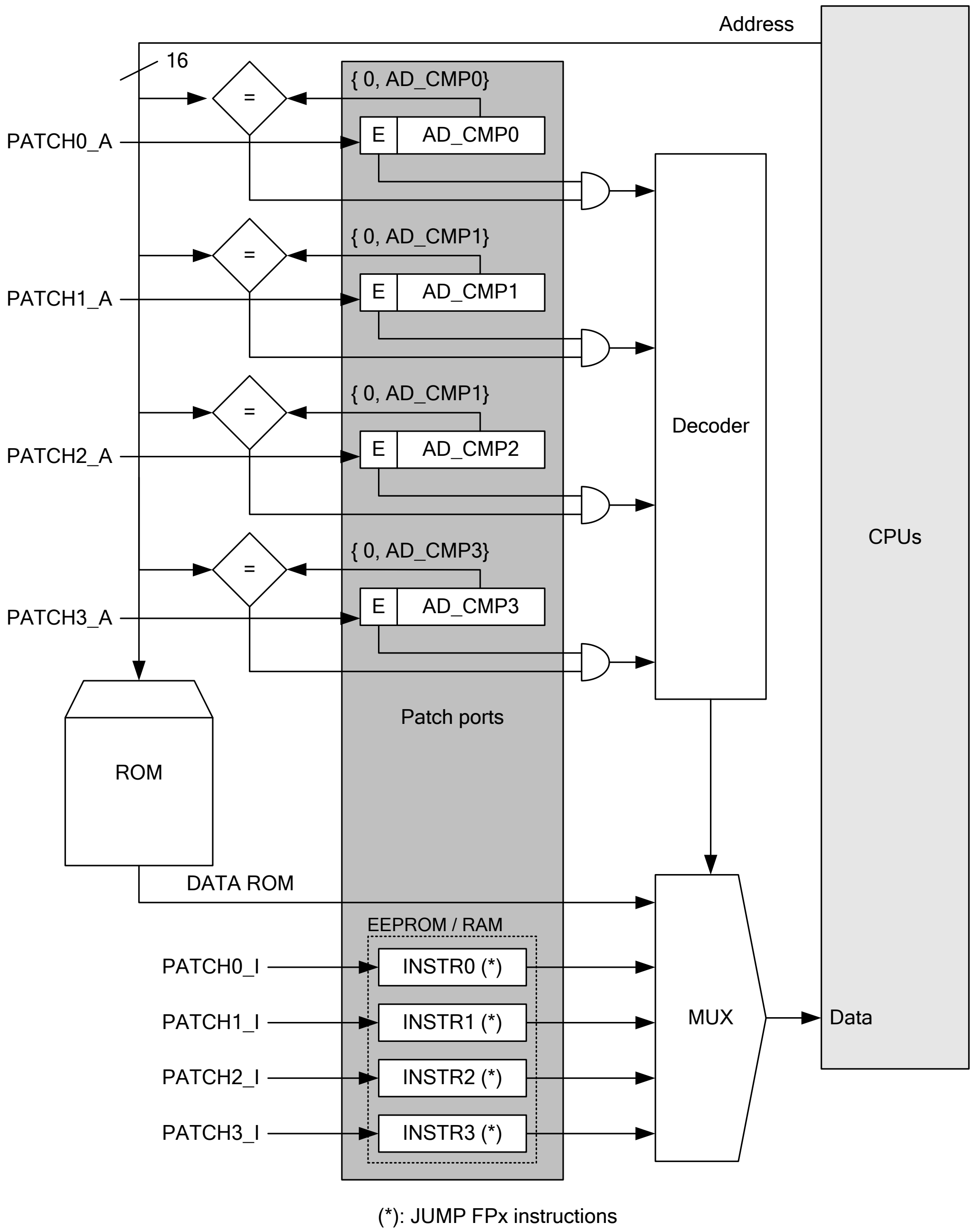


Figure 21 - Patch hardware

17.1 Principle of operation

There are 4 possible patch start addresses PATCHx_A (x=0..3) available. In case the program counter (PC) of the CPU points to an address, which is equal to one of the PATCHx_A ports (and the patch is enabled) the PC will be redirected to the address defined by the PATCHx_I port.
The patch instruction can be located in the EEPROM or the RAM.

17.2 Patch start address

Initially the patches are disabled (Bit E=0). The Mlx16 ROM startup code must be written in a way that an EEPROM byte decides if patches must be applied. If yes, patch ports must be loaded. This operation must be done prior to any other to allow patch of any code.

PATCHi_A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	E	AD_CMP0[14:0]														
At reset	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Port PATCHx_A (x = 0 to 3) must be loaded with the address where the patch should start.

Note: This address is only 15 bits, but ROM is less than 32Kbytes.

17.3 Patch jump instruction

PATCHx_I must be loaded with a special instruction (a jump into far page) and the address into the far page. Figure 22 shows a how to execute the patch in EEPROM while Figure 23 shows a how to execute the patch from RAM (it supposes RAM has been loaded before).

PATCHx_I	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	0	0	0	0	0	1	1	1	FPAD[4:0]				
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Fp7 (bits 7–5)

Resulting patch start address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	FPAD[4:0]					0	0	0

Fp7 value (Defined on Table 6) (bits 15–8)

Figure 22 - Patch code in EEPROM

PATCHx_I	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	1	0	0	0	0	0	0	1	0	1	FPAD[4:0]				
At reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Fp5 (bits 7–5)

Resulting patch start address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	0	0	0	1	FPAD[4:0]					0	0	0

Fp5 value (Defined on Table 6) (bits 15–8)

Figure 23 - Patch code in RAM

Notes:

- A patch can only start on an 8 bytes boundary.
- The last instruction of the patch must be a far jump back to the first correct ROM instruction.

Important:
The access time to EEPROM is longer than for ROM; therefore the execution time of the patched code will be a bit slower than the same code in executed from ROM.

Abnormal cases where two patches are at the same address but have different instruction is solved by giving priority to the lowest patch id. See examples below.

Examples:
If PATCH0_A = PATCH1_A, PATCH0_I is used
If PATCH0_A = PATCH3_A, PATCH0_I is used
If PATCH1_A = PATCH2_A = PATCH3_A, PATCH1_I is used

18. Application Hints

Further information regarding the use of the IO and SW pins can be found in the Application note "Standard input/output pin configurations".

18.1 Application Examples

The SWx are used for connection to a switch matrix as well as for single switches to GND or VS
The IOx pins can be used for different purposes:

1. Single switch input connected to GND or VS incl. switch diagnostics
2. Rotating encoder input
3. General purpose digital input
4. Open drain high voltage capable output
5. ADC Input

The pin IREF, via an external bipolar transistor, is used to generate a 5V voltage to supply external pull up resistors.

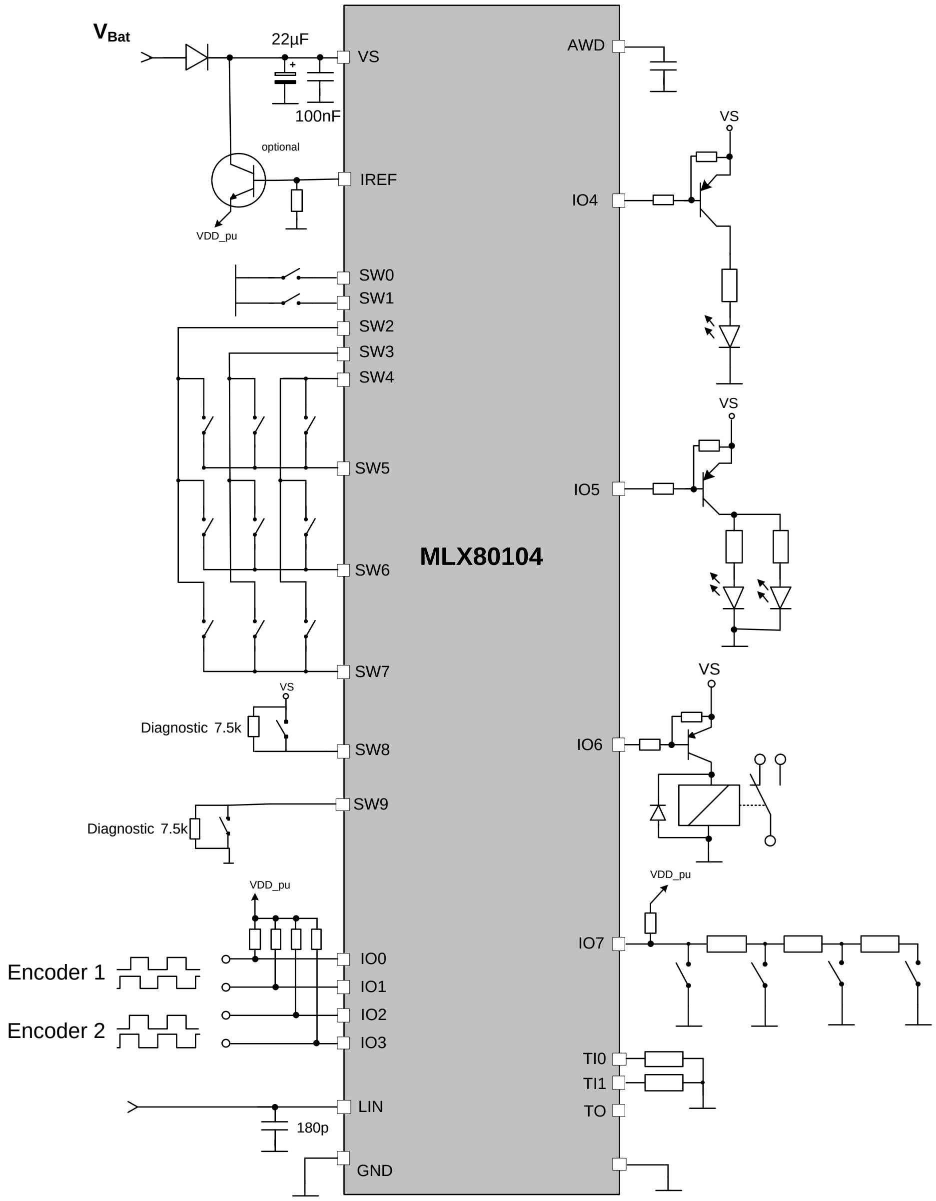


Figure 24 - Application schematic sample

18.1.1. Switch Matrix Hints

If more than two switches are closed at the same time, it can happen that reading the switches gives a wrong result. A "ghost" switch is detected, that means it will read out a certain switch is pressed, but this switch is not really pressed (See Figure 25). To avoid this effect, diodes can be used for decoupling the switches. The diodes prevent the fault current by a closed switch in another row.

Note: This wiring with diodes is only necessary if it is possible to press more than three switches at the same time.

Example: In a matrix without diodes (left example) the open switch 2b ("ghost" switch from left example) is recognized as closed. The closed switches 1b, 1c and 2c setup a wrong current path. This wrong path is prevented in the protected wiring (right example) by the diode 1c.

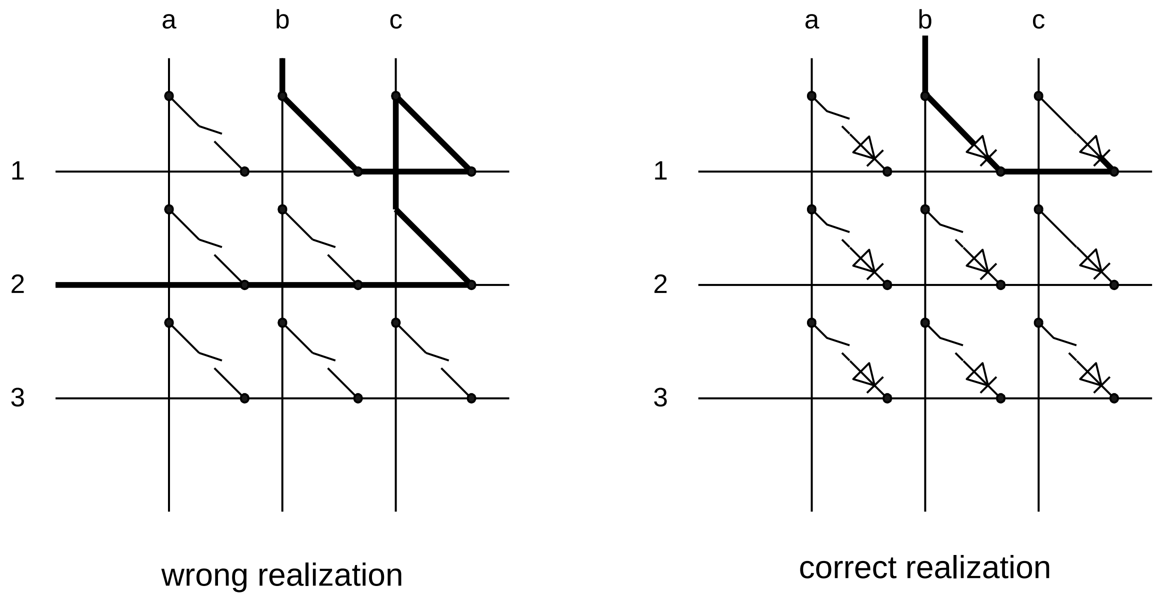


Figure 25 - Reading the switch matrix

19. Software Development

For software development a software development environment consisting of

- Compiler
- Linker
- Debugger
- User library
- LIN2.x / J2602 API

and a hardware development kit consisting of

- Evaluation board
- Emulator
- Application board

are available at Melexis. The kit description can be found in [4].

19.1 UniROM (80104 only)

Beside the software development at customer side a ready-to-use firmware, so called uniROM, is available. The uniROM firmware offers a ready to use application software which removes the need for new software development for new LIN applications. This Software can be configured to the need of different applications. Further information can be found in [1].

The main features are:

- LIN protocol specification according to LIN 2.x and J2602
- 19.2kBaud and 10.4kBaud transmission speed
- Up to 5 LIN configurable LIN frames:
  - Configurable data byte length
  - Configurable LIN identifier
  - Configurable communication direction (slave to master, master to slave)
  - Configurable data byte content on byte level
- Event triggered frame
- Go to sleep command
- Node configuration services
  - Assign NAD
  - Assign frame ID range
  - Assign frame ID (according LIN2.0)
  - Read by identifier
  - J2602 target reset
  - J2602 broadcast reset

- Error detection (Communication error (according LIN2.x), EEPROM error, Thermal overload error, under voltage error, over voltage error etc.)
- EEPROM user area for production data
- Hardware CRC to protect EEPROM data
- Internal 12MHz RC-oscillator. For higher accuracy an external resonator can be applied. But this is only necessary for slave to slave communication)
- Window watchdog and additional independent analog watchdog
- 18 configurable high voltage I/O pins which are ground shift tolerant and can be used as following:
  - Up to 18 switch inputs (low side or low side can be configured for each pin separately)) incl. broken line detection
  - Switch matrix inputs (5x5, 5x4, 4x4, 4x3, 3x3, 3x2) incl. broken line detection
  - Up to 18 configurable open drain outputs
  - Up to eight 10bit ADC inputs
  - Up to 8 PWM outputs with common frequency between 45Hz … 46,9kHz and different duty cycles for each output
  - Support of SMART Fets with current sense
  - Up to two rotary encoders supported
- Configurable debouncing times for switches
- Internal supply voltage measurement
- Configurable Wake up sources (LIN, switches, ADC)
- Software SPI and I^2C-interface supported for controlling IO extension
- Constant current source output IREF (2mA) for building an external help supply

20. Programming Interface

The MLX80104/05 programming interface consists of the pins:

- Pin 6 - TO => output
- Pin 8 - TI0 => input 0
- Pin 7 - TI1 => input 1

TO is an open drain output. In case a third party programmer is used, an external pull-up resistor of 500Ohm against 3.3V to this pin is necessary. In case the Melexis Mini E-Mlx emulator with Melexis interface adapter or the PTC-04 is used, no extra pull-up resistor is needed.

Additionally it is necessary to connect the MLX80104/05 with the supply voltage Vs and to stop the analog watchdog by connecting AWD (Pin 21) with GND.

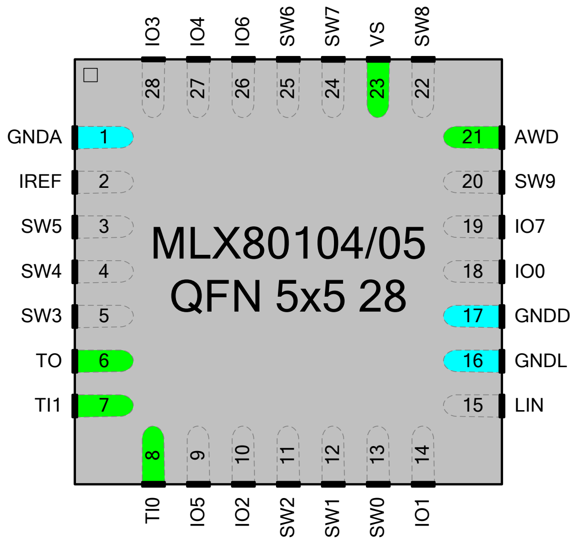


Figure 26 - Pin out MLX80104/05 – Top view

20.1 Characteristics for the interface pins

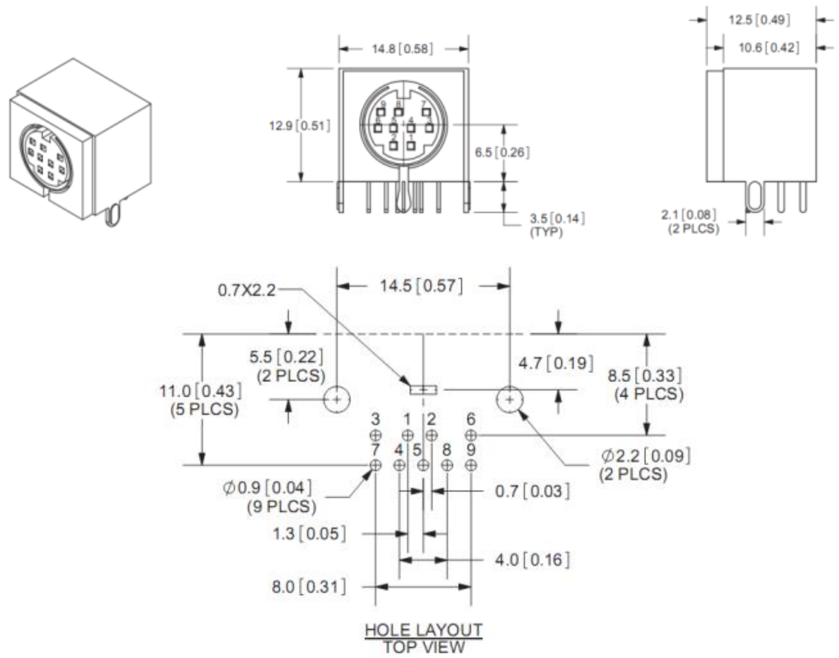
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pin VS						
Supply voltage	V_S		7		18	V
Supply voltage during OTP programming	V_S		7.8		8.2	V
Supply current, active without switch current	I_S			6	10	mA
Undervoltage lockout	V_{S_UV}		2		4.5	V
PIN AWD						
Input voltage range	V_{AWD}		0		3.4	V
Pull down current	I_{PD_AWD}			2		µA
PIN TO						
Input voltage range	V_{TO}		0		3.4	V
Pull up resistor (only necessary in case third party programmer is used)	R_{TO_PULLUP}			500		Ω
Input frequency	F_{TI}	max output load 20pF			20	MHz
PIN TI0,TI1						
Input voltage range	V_{TI}		0		3.4	V
Input threshold rising edge	V_{TI_RISE}			1.7		V
Input threshold falling edge	V_{TI_FALL}			1.5		V
Input frequency	F_{TI}				20	MHz

20.2 Melexis Mini E-Mlx emulator

To use the MLX80104/05 programming interface directly with the Melexis Mini E-Mlx connector it is necessary to put external components (see Figure 27) and a 9 pin mini circular connector with shield on the PCB. The connector could be a MD-90SM from CUI INC. This part can be ordered for instance from Digi-Key (CP-2290-ND).

The Melexis emulator does not provide the supply voltage for the MLX80104/05. Because of this the module has to be powered by an external power supply.

To disable the analog watchdog during programming and debugging it is necessary to connect pin 21 AWD to GND via a Jumper JP1.



Pin No	Name	Function
1	TI0	Test input 0
2	GND	Ground
3	VS	VS output
4	TI1	Test input 1
5	LIN/MUST	Open (not used)
6	V0	Open (not used)
7	V2	3.3V input
8	TO	Test output
9	V1	Open (not used)
Shield	GND	Ground

Table 27 - Pin description 9 pin mini circular connector

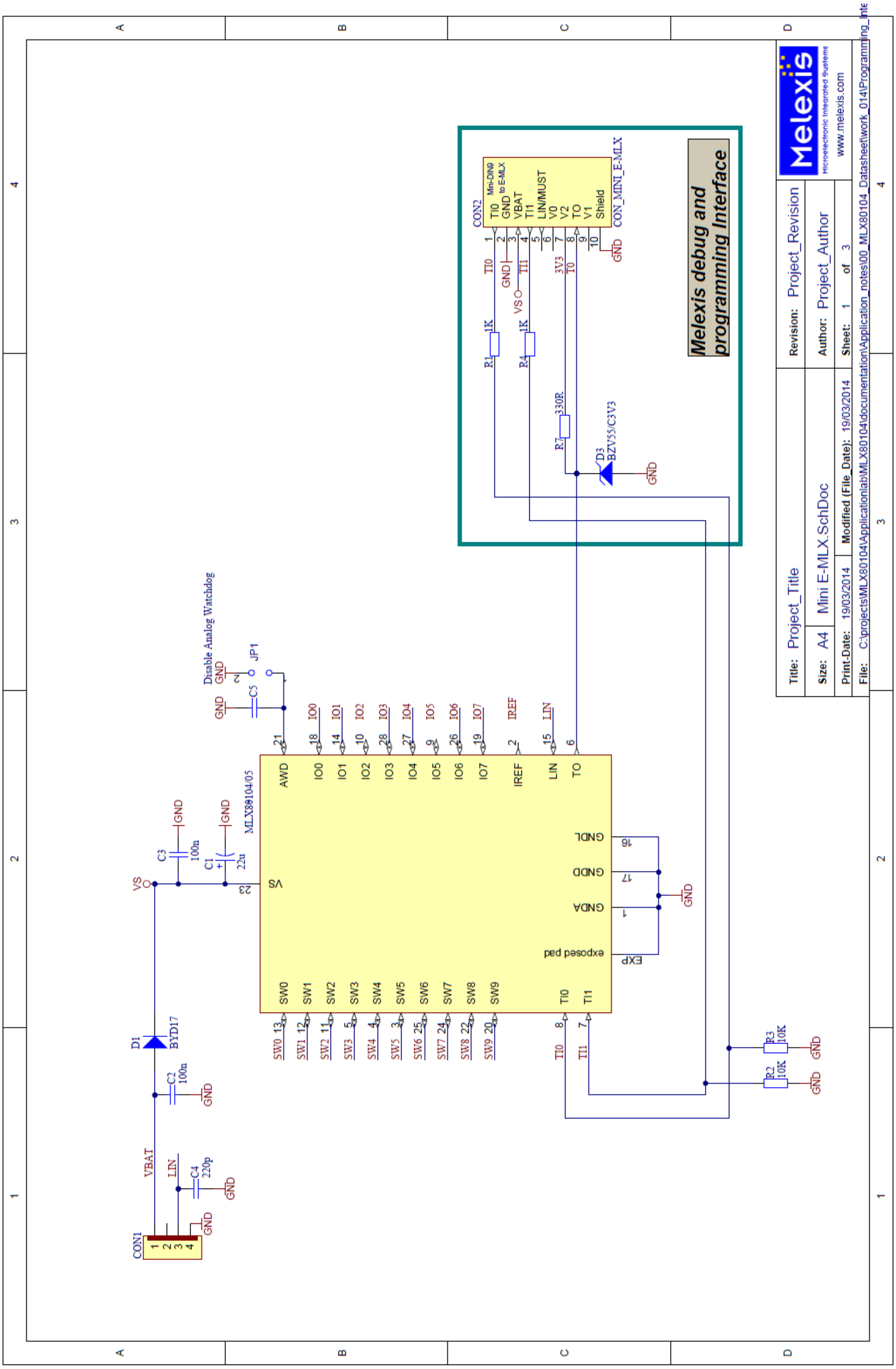


Figure 27 - MLX80104/05 programming interface with the Melexis Mini E-Mlx emulator

20.3 Melexis Mini E-Mlx emulator and Melexis interface adapter

In case there is not enough space to put all necessary components on the PCB as described in chapter 20.1 it is possible to use the Melexis interface adapter. This connector includes the 9 pin mini circular connector as well as all necessary components.

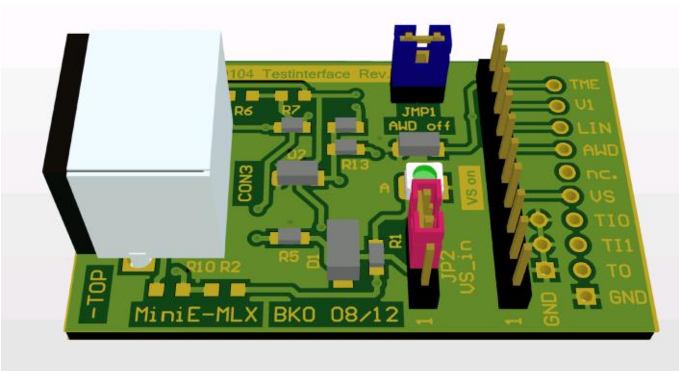


Figure 28 - Melexis MLX80104/05 programming interface adapter

The interface adapter provides an 10 pin header on top side as well as an 10 pin female header on the bottom side to connect the adapter to the MLX80104/05 module.

The Melexis emulator does not provide the supply voltage for the MLX80104/05. Because of this the module has to be powered by an external power supply.

Pin No	Name	Function
1	GND	Ground
2	TO	Test output
3	TI1	Test input 1
4	TI0	Test input 0
5	VS	VS input
6	n.c.	not used
7	AWD	Analog watchdog
8	LIN/MUST	not used
9	V1	not used
10	TM_ENABLE	not used

Table 28 - Pin description 10 pin header connector

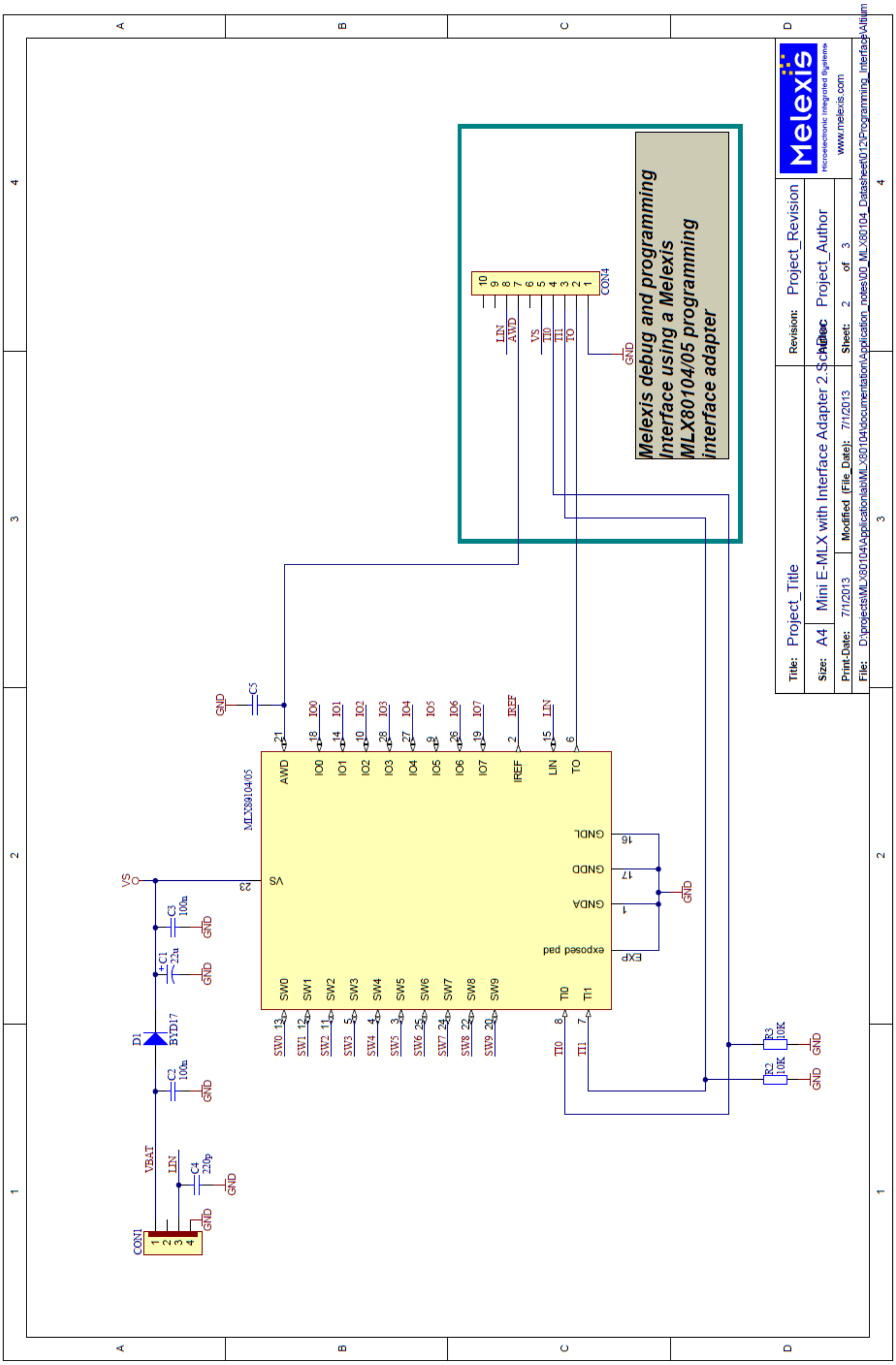


Figure 29 - MLX80104/05 programming interface with the Melexis Mini E-Mlx emulator and Melexis interface adapter

20.4 Melexis Programmer PTC-04

The PTC-04 can be used for programming OTP & EEPROM via Melexis Test Interface. 3 test pins must be accessible by the PTC-04 programmer. These pins are TO (Test Interface output), TI0 and TI1 (both Test Interface inputs are used for data and clock).
Additionally, the analog Watchdog pin AWD must be connected to GND to disable it. Otherwise, the IC will be reset via the analog Watchdog which makes it impossible to execute any operation via the Melexis Test Interface.
A more detailed schematic can be found in Figure 31.

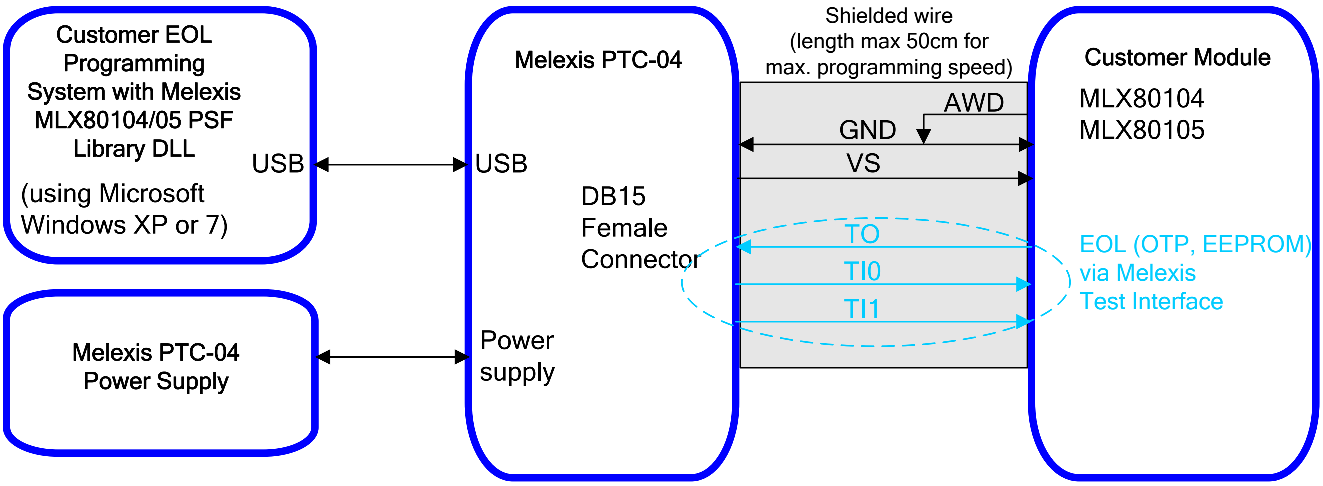


Figure 30 - Connection diagram between PTC-04 and MLX80104/5

There is no additional power supply for the MLX80104/5 necessary. It will be powered via the PTC-04.

Melexis suggests to keep the cable length between the PTC-04 and the MLX80105 as short as possible to allow a maximum programming speed (in the range of 0.5m maximum). Shielded wires must be used.

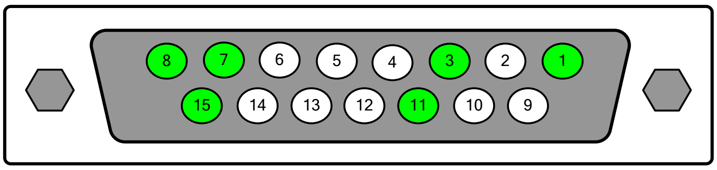
The most critical connections regarding the used cable and the cable length are TO, TI0 and TI1.

In case the cable length is longer than 0.5m the customer has to be secure that the shape of the signals for TO (at the PTC-04), TI0 and TI1 (at the MLX80104/05) are still correct. Otherwise the test interface speed has to be reduced by using the Melexis PSF DLL function SetSetting().

20.4.1. PTC04 DB 15 Female Connector

All unused pins of the connector have to be left open.

PTC05 DB15 Female Connector



Pins	Name	Description
1	***VBAT***	***Power Supply (output)***
2	N.C.	Not connected
3	***DGND***	***Digital Ground***
4	MUST	Analog test pin
5	TXD0	USART Transmit Data
6	VOUT_PPS2	VOUT_PPS2
7	***MUST0 / TI0***	***Digital test pin TI0***
8	***MICE / TO***	***Digital test pin TO***
9	***LIN_OUT***	***LIN BUS***
10	+5V_DIG_CON	+5V DC Supply
11	***DGND***	***Digital Ground***
12	RXD0	USART Receive Data
13	XCK0	USART Clock
14	N.C.	Not connected
15	***MUST1 / TI1***	***Digital test pin TI1***

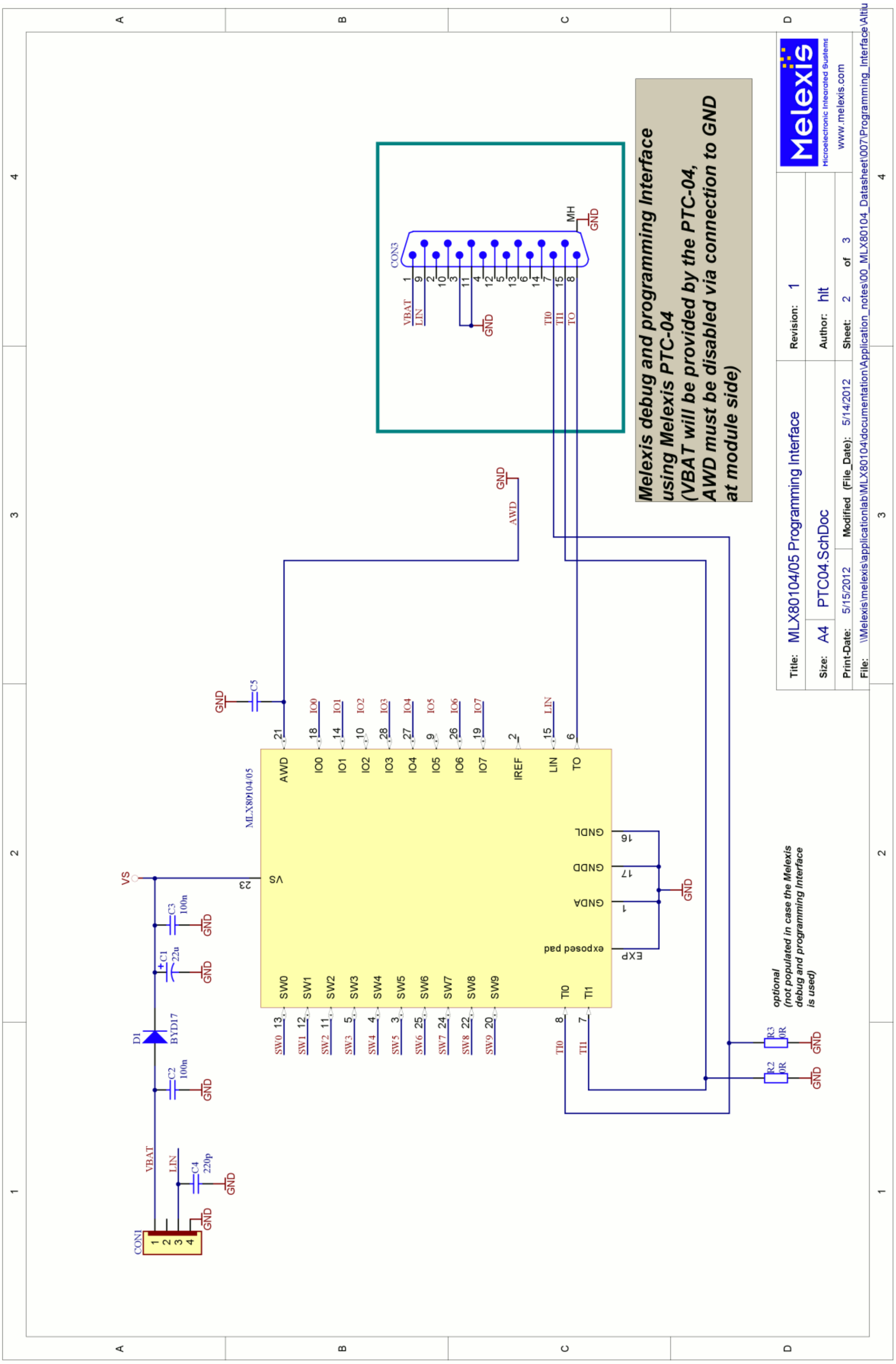


Figure 31 - MLX80104/05 programming interface with the Melexis PTC-04

20.5 Third party programmer

In case a third party programmer tool is used, the MLX80104/05 based module has to provide at least following connections.

MLX80104/05 Pin No	Name	Function
1,17,16	GND	Ground
6	TO	Test output
7	TI1	Test input 1
8	TI0	Test input 0
21	AWD	Analog watchdog

Table 29 - Connections for third party programmer

21. Operating under Disturbance

21.1 Loss of battery

If the MLX80104/5 is disconnected from the battery, the bus pin is in high Impedance State. There is no impact to the bus traffic and to the ECU itself.
The IC will be reverse powered if switches are placed outside and via wiring harness a short circuit to battery or a faulty blocked switch is connected to the MLX80104/5.To prevent undefined failure currents the ports for connections to external switches or loads have to be protected by a serial resistor of at least 100Ω.

21.2 Loss of Ground

In case of an interrupted ECU ground connection there is no influence to the bus line.

21.3 Short circuit to battery

The LIN transmitter output current is limited to the specified value in case of short circuit to battery in order to protect the MLX80104/5 itself.

21.4 Short circuit to ground

If the bus line is shorted to negative shifted ground levels, there is no current flow from the ECU ground to the bus and no distortion of the bus traffic.
If the controller detects a short circuit of the bus to ground (RxD timeout) the transceiver can be set into sleep mode. The internal slave termination resistor is switched off and only a high impedance termination is applied to the bus. The failure current of the whole system can be reduced by at least ten times to prevent a fast discharge of the car battery. If the failure disappears, the bus level will become recessive again and will wake up the system even if no local wake up is present or possible.

21.5 Thermal overload

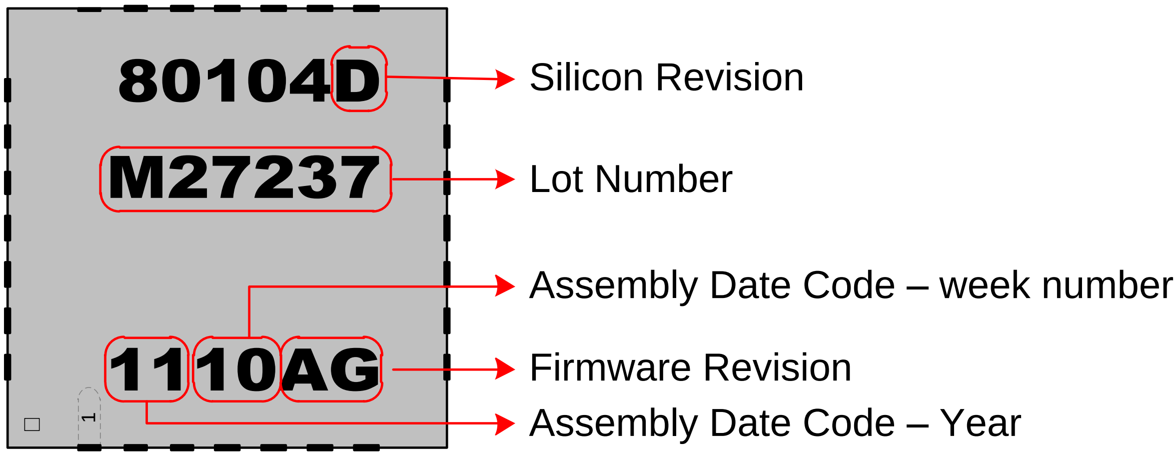
The MLX80104/5 is protected against thermal overloads. If the chip temperature exceeds the specified value, the transmitter is switched off until thermal recovery. The receiver is still working during thermal shutdown.

21.6 Undervoltage Vs

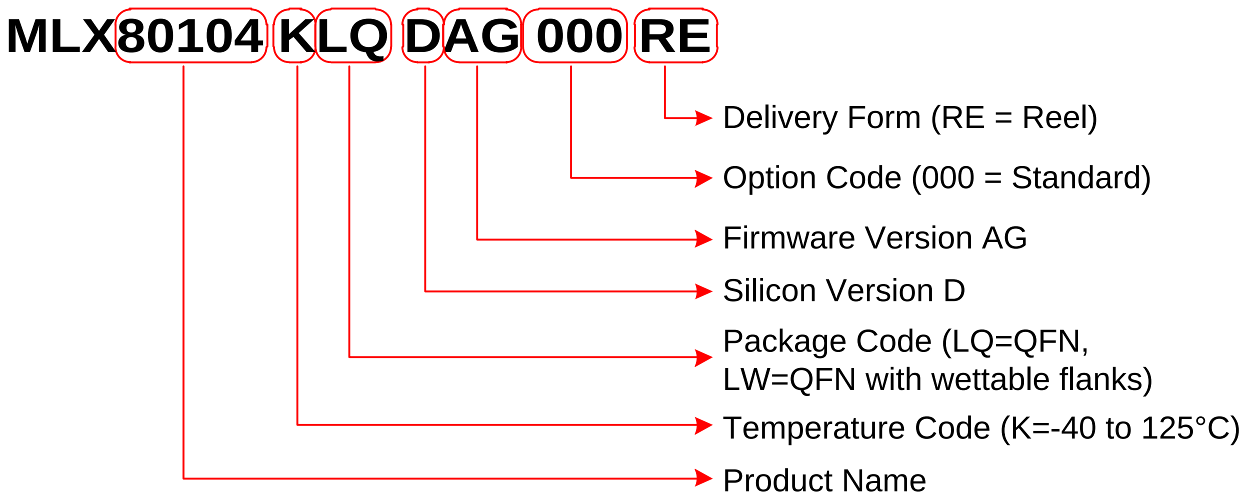
If the ECU battery supply voltage is missing or decreases under the specified value, the LIN pin functions as passive.

22. Marking/Order Code

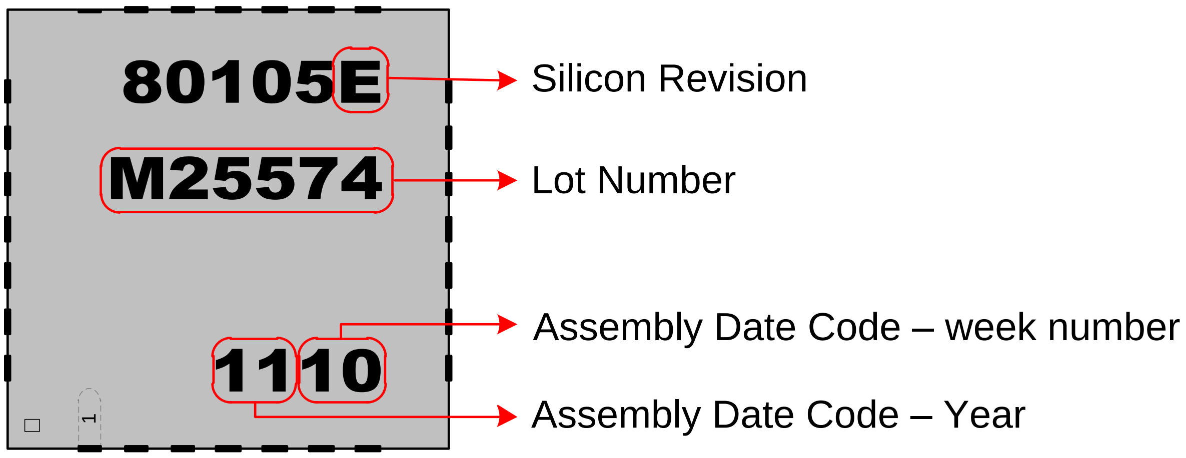
22.1 Marking MLX80104



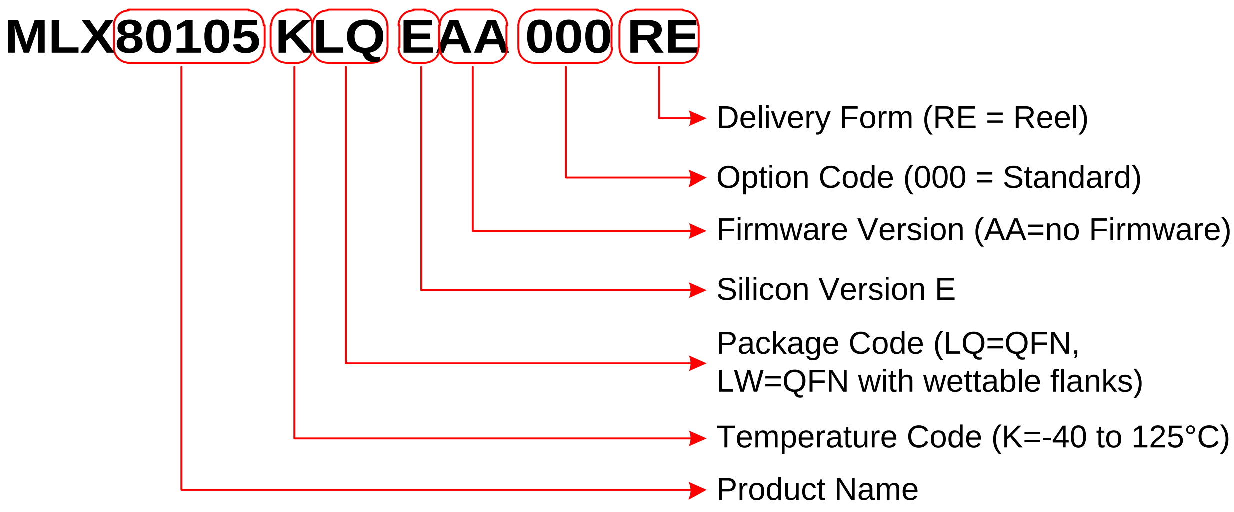
22.2 Order Code MLX80104



22.3 Marking MLX80105



22.4 Order Code MLX80105



23. Pin Description

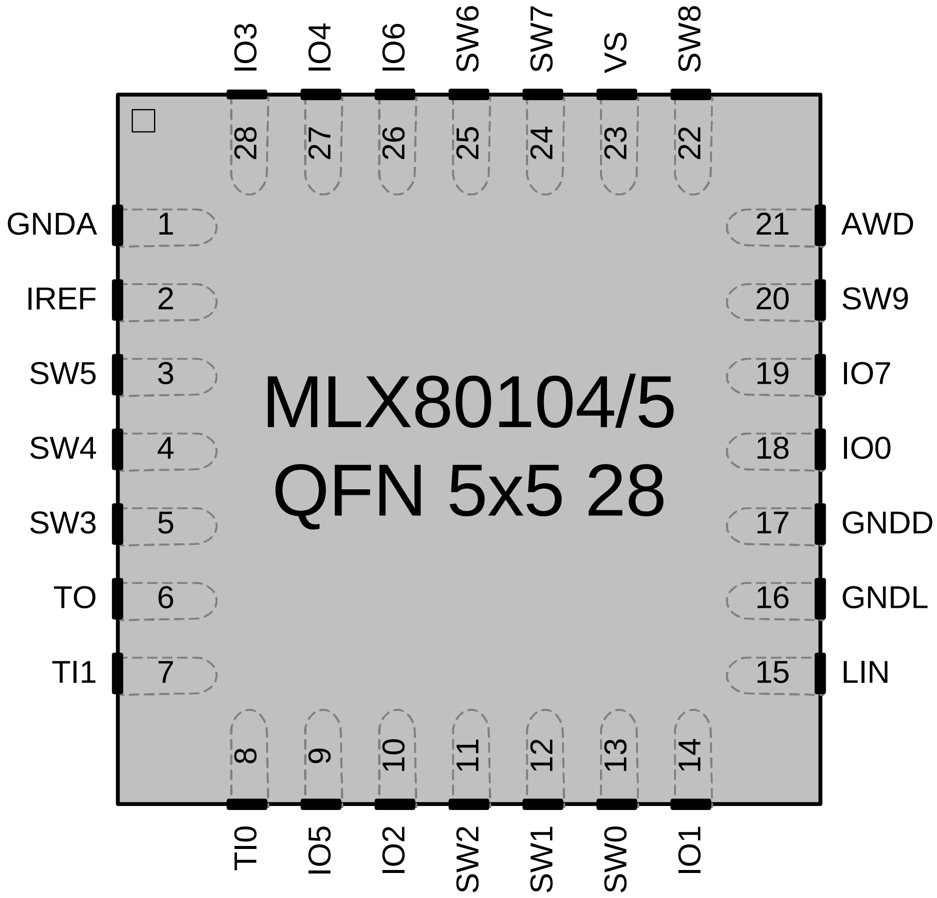


Figure 32 - Pin out MLX80104/5 – Top view

Table 1 – Pin Description MLX80104 QFN 5x5 28

Pin No	Name	Function	I/O Type
1	GNDA	Analogue ground and ADC ground	GND
2	IREF	IREF output	O
3	SW5	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
4	SW4	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
5	SW3	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
6	TO	Test output, unconnected in application mode	O
7	TI1	Test input - connect to GND in application mode	I
8	TI0	Test input - connect to GND in application mode	I
9	IO5	SWx functionality and ADC input, wake up capable, PWM output	I/O
10	IO2	SWx functionality and ADC input, wake up capable, PWM output	I/O
11	SW2	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
12	SW1	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
13	SW0	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
14	IO1	SWx functionality and ADC input, wake up capable, PWM output	I/O
15	LIN	Connection to LIN bus	IO
16	GNDL	LIN driver ground	GND
17	GNDD	Digital ground	GND
18	IO0	SWx functionality and ADC input, wake up capable, PWM output	I/O
19	IO7	SWx functionality and ADC input, wake up capable, PWM output	I/O
20	SW9	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
21	AWD	Watch dog load capacitor	I/O
22	SW8	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
23	VS	High voltage supply, battery voltage	P
24	SW7	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
25	SW6	Switch matrix I/O, single switch input, open drain output, wake up capable	I/O
26	IO6	SWx functionality and ADC input, wake up capable, PWM output	I/O
27	IO4	SWx functionality and ADC input, wake up capable, PWM output	I/O
28	IO3	SWx functionality and ADC input, wake up capable, PWM output	I/O

24. Mechanical Specification

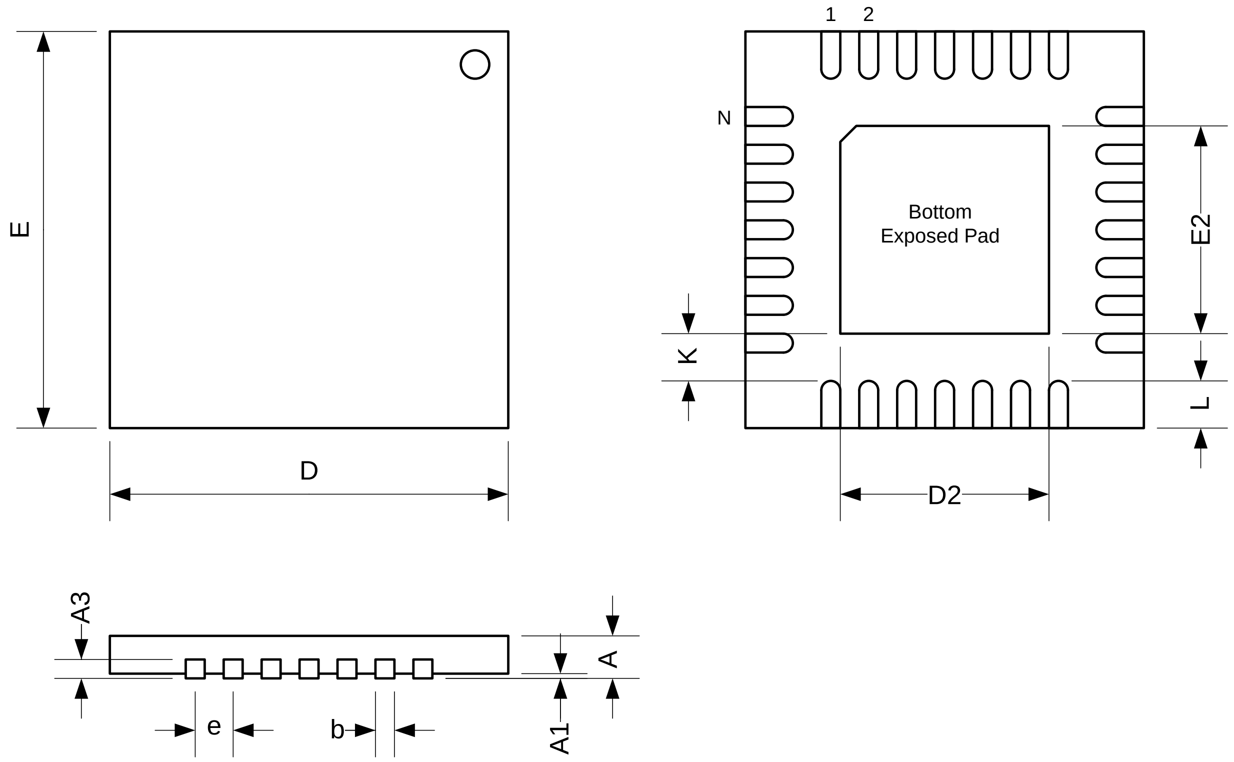


Figure 33 - QFN28 Drawing

Table 2 – QFN28 Package Dimensions

Symbol		A	A1	A3	b	D	D2	E	E2	e	K	L	N [6][3]	ND [5]	NE [5]	
QFN28	min	0.80	0	0.20	0.18	5.00	3.00	5.00	3.00	0.50	0.20	0.45	28	7	7	[1] [2]
	nom	0.90	0.02		0.25		3.10		3.10			0.55				
	max	1.00	0.05		0.30		3.25		3.25			0.65				

[1] Dimensions and tolerances conform to ASME Y14.5M-1994
[2] All dimensions are in Millimeters. All angels are in degrees
[3] N is the total number of terminals
[4] Dimension b applies to metalized terminal and is measured between 0.25 and 0.30mm from terminal tip
[5] ND and NE refer to the number of terminals on each D and E side respectively
[6] Depopulation is possible in a symmetrical fashion

25. Land Pattern Recommendations

This recommendation is provided as a guideline for board layout.

Table 3 – QFN28 Land Pattern Dimensions

Symbol	Land X1	Land Y1	Tab Land X2	Tab Land Y2	Land Space C1	Land Space C2
(in mm)	0.30	1.00	3.25	3.25	4.70	4.70

26. ESD/EMC Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

26.1 ESD/EMC Recommendations for the MLX80104/5

In order to minimize EMC influences, the PCB has to be designed according to EMC guidelines. The MLX80104/5 is an ESD sensitive device and has to be handled according to the rules in IEC61340-5-2. MLX80104/5 will apply the requirements in the application according to the specification and to ISO7637-2

26.2 Automotive Qualification Test Pulses

The following chapter is valid for a complete assembled module. That means that automotive test pulses are applied to the complete module and not to the single IC. Therefore attention must be taken, that only protected pins (protection done the IC itself or by external components) are wired to a module connector. In the recommended application diagrams, the reverse polarity diode together with the capacitors on supply pins, the protection resistors in several lines and the load dump protected IC itself will protect the module against the below listed automotive test pulses. The exact values of the capacitors for the application have to be chosen in dependence of the automotive requirements of the module.

For the LIN pin the specification “LIN Physical Layer Spec 2.x” is valid.
Supply Pin VS is protected via the reverse polarity diode and the supply capacitors. No damage will occur for defined test pulses. A deviation of characteristics is allowed during pulse 1 and 2; but the module will recover to the normal function after the pulse without any additional action. During test pulse 3a, 3b, 5 the module will work within characteristic limits.

Test pulses on supply lines

Parameter	Symbol	Us	Dim	Test Condition
Transient test pulses in accordance to ISO7637-2 (supply lines) Test pulses are defined with the 12V DC voltage shift on the supply lines. Application schematics are according application notes.				
Test pulse #1	vpulse1	-100	V	5000 pulses, t_1 = 5s, t_d = 2ms, R_i = 10Ω
Test pulse #2a	vpulse2	75	V	5000 pulses, t_1 = 0.5s, t_d = 0.05ms, R_i = 2Ω
Test pulse #3a	vpulse3a	-200	V	1h, t_1 = 0.1ms, t_4 = 10ms, t_5 = 90ms, R_i = 50Ω
Test pulse #3b	vpulse3b	200	V	1h, t_1 = 0.1ms, t_4 = 10ms, t_5 = 90ms, R_i = 50Ω
Test pulse #5b	vpulse5	45	V	10 pulses, t_d = 400ms, R_i = 0.5Ω

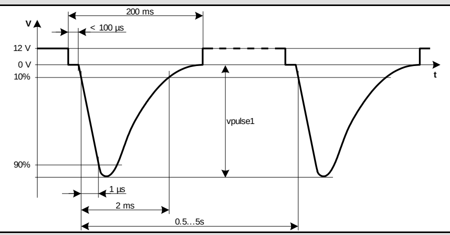
Test pulses on LIN line

Parameter	Symbol	Us	Dim	Test Condition
Transient test pulses in accordance to ISO7637-3 (signal lines) Test pulses are defined with the 12V DC voltage shift on the signal lines. Application schematics are according application notes.				
Test pulse #1 [8]	vpulse1	-100	V	5000 pulses, t_1 = 5s, t_d = 2ms, R_i = 10Ω
Test pulse #2a [9]	vpulse2	75	V	5000 pulses, t_1 = 0.5s, t_d = 0.05ms, R_i = 2Ω
Test pulse #3a	vpulse3a	-200	V	1000 bursts, t_1 = 0.1ms, t_4 = 10ms, t_5 = 90ms, R_i = 50Ω
Test pulse #3b	vpulse3b	200	V	1000 bursts, t_1 = 0.1ms, t_4 = 10ms, t_5 = 90ms, R_i = 50Ω

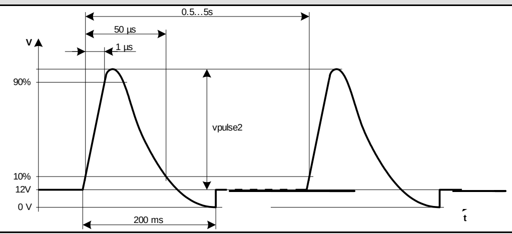
26.3 EMC Test pulse definition

EMC Test Pulse shapes

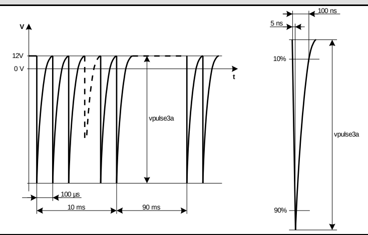
Test Pulse 1



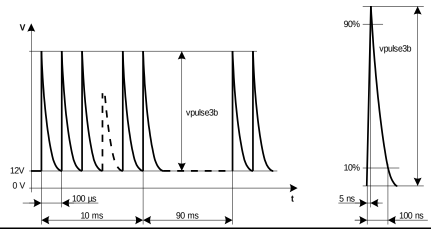
Test pulse 2



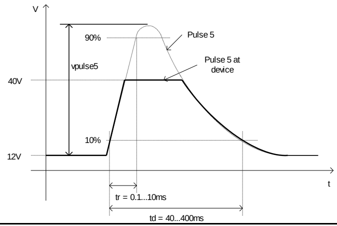
Test Pulse 3a



Test Pulse 3b



Test Pulse 5 (Load Dump)



[8] Test pulse 1 is not part of ISO 7637-3 for signal lines, this test is made additional.
[9] Test pulse 2 is not part of ISO 7637-3 for signal lines, this test is made additional.

27. References

[1]	Software Functional Specification for MLX80104 UniROM	
[2]	LIN Specification Package 2.1	November 24, 2006
[3]	GM LIN/J2602 Implementation Specification	Issue 1.4 December 19, 2006
[4]	MLX80104/08 – Software Development Kit	

28. List of Abbreviations

Dp	Direct page
Ep	EEPROM
Fp	Far page
GCC	GNU Compiler Collection

29. Revision History

Version	Changes	Remark	Date
0.1		First preliminary release	March 2008
0.11	Updated application schematic		March 2008
001	Update of block diagram of MLX80104 Increase RAM size to 512byte Update absolute maximum ratings Update static characteristics Definition of pull up/down resistance on SWx and IOx in sleep mode Chapter ADC Add additional channel IREF Chapter PWM unit Increase number of PWM channels on IOx to eight Change the access to duty cycle register Chapter mechanical specification Update package dimensions Update chapter automotive test pulses		December 2008
002	Correct test pin description in chapter Pin description Chapter Timer added Application example modified ADC chapter updated Chapter Patches added		February 2010
003	Update absolute maximum ratings		July 2010
004	Chapter PWM Unit Equation for PWM_DIV register added Frequency table added Chapter Timer Equation for Timer register added Chapter ADC Description for input divider added		September 2010
005	Chapter Programming Interface added		September 2010
006	Small layout changes done		January 2011
007	Chapter Application Examples Application Schematic modified, capacitor value at VS pin increased to fulfil the performance status A Chapter PWM unit Block Diagram PWM unit modified Chapter Automotive Qualification Test Pulses Voltage levels updated		August 2011
008	Order Information updated Marking MLX80104/5 updated Disclaimer updated Chapter Software Development added		January 2012
009	Package drawing corrected		March 2012

010	Chapter “Memory Mapping” updated Chapter “Programming Interface” New sub-chapter “Melexis programmer PTC-04” added New chapter “Land Pattern Recommendations” added Chapter “Operating Conditions” updated Chapter “Melexis Programmer PTC-04” updated		June 2012
011	Chapter “List of Abbreviations” added Chapter “EEPROM” updated		April 2013
012	Chapter “Programming Interface” updated		July 2013
013	Chapter “Order Code” updated		January 2014
014	Chapter “Order Code” updated Chapter “Melexis Mini E-Mlx emulator and Melexis interface adapter” updated Chapter “Entering Sleep Mode by API” updated		March 2014
015	Chapter “Order Code” updated Chapter “Static Characteristics” updated		May 2014
016	Chapter “Operating Conditions” updated Chapter “Switch diagnosis” updated Chapter “Order Code” updated (wettable flanks) Chapter “Reserved EEPROM Segments” added Chapter “The IREF pin” updated Parameter “LIN current during loss of Ground” updated in chapter “Static Characteristics”		April 2015
017	Chapter “Characteristics for the interface pins” Parameter “Supply voltage during OTP programming” updated	Only MLX80105 affected	June 2016

30. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

31. Disclaimer

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Or for additional information contact Melexis Direct:

Europe, Africa, Asia:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

America:
Phone: +1 248 306 5400
E-mail: sales_usa@melexis.com

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