# Le9622
## Subscriber Line Interface Circuit
## miSLIC™ Series
Preliminary Data Sheet

Document ID# 157378 Version 3 September 2017

## Features

- **Cost Optimized Dual Channel FXS Solution**
  - 53-pin 7x7mm 0.4mm Pitch QFN Package
  - Low Cost, 2-Layer PCB Reference Designs
  - Supports Multi-Channel Enterprise Applications
- **PCM/SPI Interface**
  - Programmable Interface Voltage to support 1.8V, 2.5V and 3.3V SoC Processors
- **Low Cost, Energy Efficient Dual Battery Switching Regulator Architectures**
  - Consistent with Code of Conduct on Energy Consumption of Broadband Equipment
  - *Patented* Shared Buck-Boost Automatic Battery Switch (BBABS)
    - 60Vrms ringing with 5 REN load
  - Multi-Line Inverting Boost Automatic Battery Switch (ABS)
    - 70Vrms ringing with 5 REN load
- **VoicePath SDK and VP-API-II Software available to implement FXS functions**
- **VeriVoice Professional Test Suite Software**
  - Comprehensive subscriber loop testing, including Telcordia GR-909-CORE / TIA-1063
- **VeriVoice Manufacturing Test Package - VVMT**
  - Facilitates factory testing of assembled boards
- **Worldwide Programmability**
- **Narrowband or Wideband operation**

## Applications

- **Multi-Channel Enterprise and Small Office**
- **DSL Residential Gateways and Integrated Access Devices (IADs)**
- **Cable eMTAs**
- **PON Single Family Units (SFUs)**
- **Fiber to the Premise/Home/Building (FTTx)**
- **Fixed Wireless (LTE Gateways)**

### Ordering Information

| Device OPN | Device Type | Package | Packing |
|---|---|---|---|
| Le9622RQCT | 120V SLIC | 53-pin QFN | Tape & Reel |
| Le9622RQC | 120V SLIC | 53-pin QFN | Tray |

*The Green package meets RoHS 2 Directive 2011/65/EC of the European Council to minimize the environmental impact of electrical equipment.*

## Description

The miSLIC™ Series Line Circuits together with a VoIP processor or SoC, provides an economical turn-key solution for derived voice applications. The Le9622 miSLIC 2 FXS device is a cost optimized FXS solution.

The versatile Le9622 miSLIC is controlled via a PCM/SPI interface which makes the device ideal for both 4 or 8 channel Enterprise and 2 channel Broadband Gateway applications.

Two power supply topologies are supported: Multi-Line Inverting Boost for up to 70 Vrms ringing into 5 REN and a patented Shared Buck Boost Automatic Battery Switch for up to 60 Vrms ringing into 5 REN. Manufacturing self test and subscriber line diagnostics are available features. The Le9622 features wideband clarity and complete BORSCHT functionality. All AC, DC and power parameters are programmable making the Le9622 device suitable for any short loop application requiring SLIC functionality.

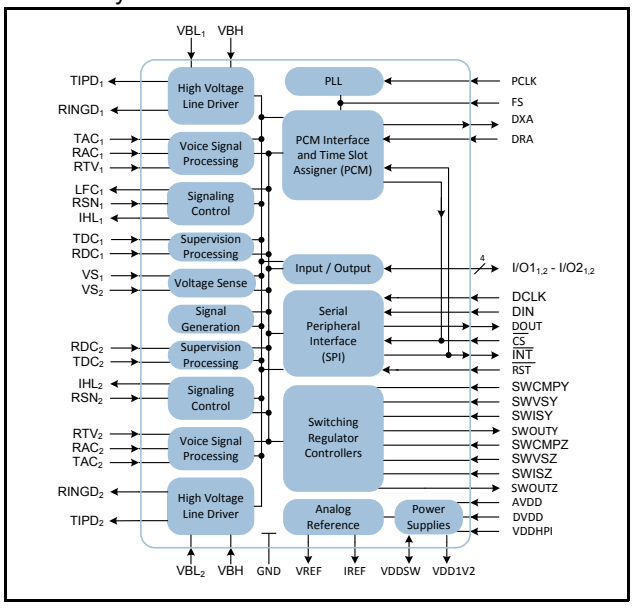



**Figure 1 - Le9622 Device Block Diagram**

# Table of Contents

# List of Figures

# List of Tables

# 1.0 Solution Overview

The sixth-generation *miSLIC* line interface solution consists of *a miSLIC* device, *VoicePath API-II (VP-API-II)* Software, and *Profiles* Data Structures. To support the *miSLIC* device, Microsemi offers comprehensive software and hardware collateral packages, including 2-layer printed circuit board reference designs.

The *VoicePath API-II (VP-API-II)* software initializes the FXS port coefficient data containing application or country-specific AC and DC parameters, ringing and other signaling characteristics, and configures the switching power supply. *VP-API-II* resides on the customer's VoIP processor or SoC and provides high level control over the telephony functions. *VP-API-II* offers a seamless migration between products utilizing its common software architecture and interfaces with the Microsemi *VeriVoice Professional Test Suite Software*.

A *Microsoft*® *Windows*® GUI (Graphical User Interface) application, *VoicePath Profile Wizard (VP Profile Wizard)*, allows the user to select the operating parameters of the FXS channels and to automatically generate the sets of data structures, called *Profiles*, that are required by the *VP-API-II* for integration with the VoIP host software.

## 1.1 Le9622 Automatic Battery Switch (ABS) Devices

The Le9622 device implements a dual-channel universal telephone line interface with a PCM and SPI interface, making it the ideal solution for 4 or 8 channel Enterprise and Small Office applications and dual port cable eMTAs, fiber PON SFUs, Integrated Access Devices, DSL Gateways, and other telephony products for worldwide markets.

Two Automatic Battery Switch (ABS) power supply topologies are supported: The lower cost Buck Boost ABS for lower cost and Microsemi's Multi-line Inverting Boost topology. The Le9622 features integrated switching controllers which generate the high voltages needed for efficiently powering and ringing analog telephones. The Le9622 performs all necessary voice telephony functions from driving a high voltage subscriber telephone line to DSP Codec functions. All AC, DC, and signaling parameters are fully programmable via the PCM and SPI interface. The Le9622 supports both Wideband and Narrowband voice.

The *VoicePath API-II (VP-API-II)* software initializes each FXS port coefficient data containing application or country specific AC and DC parameters, ringing and other signaling characteristics, and configures the switcher. *VP-API-II* resides on the customer's VoIP processor or SoC and provides high level control over the telephony functions. *VP-API-II* offers a seamless migration between products utilizing its common software architecture and interfaces with the Microsemi *VeriVoice Professional Test Suite Software*.

Figure 2 shows a high level solution diagram with a *Le9622* device, *VP-API-II* and *Profiles*.

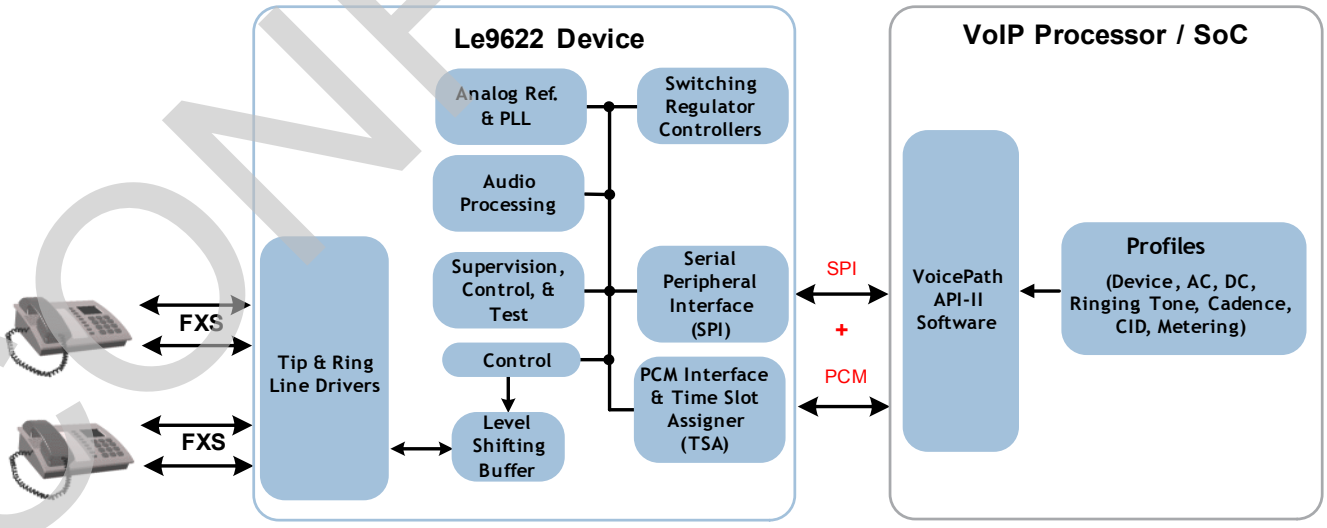



**Figure 2 - Le9622 Dual-Channel VoicePort Solution Diagram**

# 2.0 Le9622 Device Overview and Block Diagram

## 2.1 miSLIC™ Series Features

- Performs all Battery feed, Ringing, Signaling, Coding, Hybrid and Test (BORSCHT) functions
- Single chip solution provides high voltage line driving, digital signal processing, and high voltage power generation for two lines
  - Le9622 is ideal for 4 and 8 line applications
- Wideband 150 Hz – 6.8 kHz and Narrowband 200 Hz – 3.4 kHz Codec modes
  - Compliant with Cable Labs *PacketCable High Definition Voice Specification PKT-SP-HDV-104-120823*
- Exceeds *Telcordia® GR-909-CORE* transmission requirements
- Single hardware design meets worldwide requirements through software programming of:
  - Ringing waveform, frequency and amplitude
  - DC loop feed characteristics and current limit
  - Loop supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring trip filters
  - Two wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains and equalization
  - Digital I/O
  - A-law/µ-law and linear coding selection
  - Switching power supply
- Per Channel Wideband or Narrowband Select
- Supports loop-start and ground-start signaling
- On-hook transmission
- Power/service denial mode
- Smooth polarity reversal
- Supports wink function
- Metering generation with envelope shaping
  - Programmable frequency and duration
- Internal Test Termination
- Compatible with inexpensive protection networks
- Self contained ringing generation and control
  - Programmable ringing cadencing
  - Internal battery-backed balanced sinusoidal or trapezoidal
  - Integrated ring trip filter and software, manual or automatic ring trip mode
- Flexible tone generation
  - Call progress tone generation
  - DTMF tone generation
  - Universal Caller ID generation (FSK and DTMF signaling)
  - Howler tone generation with *VP-API-II* with frequency modulation capability for compliance with *BT*, *NTT*, and *Austel* special Howler tone requirements
- DTMF detection with *VP-API-II*

- Integrated switching regulator controller
  - Generates battery voltage for each line
  - Energy efficient in all states
  - Low idle power per line
  - Line feed characteristics independent of battery voltage
  - Direct FET Driver
- *VeriVoice Professional Test Suite Software*
  - Monitors two-wire interface voltages and currents for subscriber line diagnostics
  - Integrated self-test features
- *VeriVoice Manufacturing Test Package*
- Supported by *VoicePath SDK* and *VP-API-II*
- Small physical size in 7x7 mm, 0.4mm pitch 53-pin QFN
- -40°C to +85°C operation
- Programmable PCM and SPI interface voltage
  - Supports communication with host processors at 1.8 V, 2.5 V or 3.3 V
  - Allows for optimized interface to 4 or 8 channel application
  - Supports SPI Modes 0 and 3
- Low BOM cost:
  - Compatible with 2-layer PCB designs
  - Small value/size/cost switcher output and SLIC capacitors
  - No external diodes for protecting SLIC against negative surges
- Low-Power Idle Mode (LPIM)
  - Voltage based off-hook detection
- Monitors and drives Tip & Ring independently
- Built-in voice path test modes
- Simultaneous ground key / DC fault detection
- Over current monitoring and blanking
- Hook and ground key detection with hysteresis and calibrated thresholds
- On-chip timer functions
- Comprehensive device calibration capabilities
  - Short calibration time
  - No need to generate voltages to the Tip/Ring interface
  - Programmable loop current dependent overhead

## 2.2 Device Block Diagram

Figure 3 shows the major functional blocks of the Le9622 device.

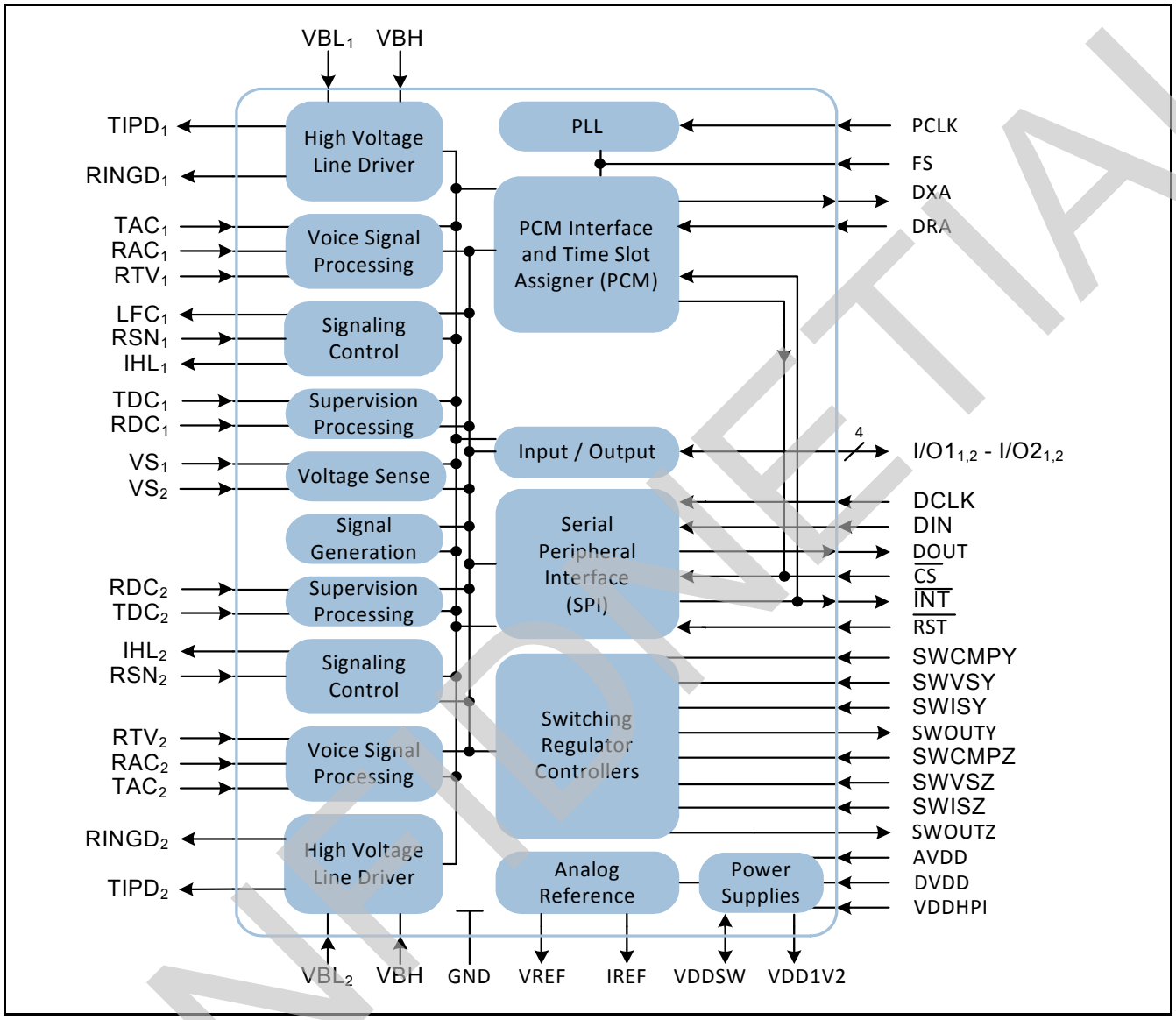



**Figure 3 - Le9622 Device Block Diagram**

# 3.0 Functional Description

## 3.1 Host Port Interface

The Le9622 device features a flexible host port interface which is hardware selectable for communicating with VoIP processors and SoCs using standard PCM and SPI interfaces.

The host port interface voltage level (VDDHPI) can be set for 1.8 V, 2.5 V, or 3.3 V for maximum system level compatibility. The host port interface supports the standard telecommunications clock rates of 1.024 MHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz and 8.192 MHz with a Frame Sync (FS) of 8 kHz.

### 3.1.1 PCM Interface and Time Slot Assigner

The PCM Interface and Time Slot Assigner (PCM block) is a synchronized serial mode of communication between the system and the Le9622 device. Voice data is transmitted/received on a serial PCM highway. This highway uses Frame Sync (FS) and PCLK as reference.

Data is transmitted out of the DXA pin and received on the DRA pin. The Le9622 device transmits/receives single 8-bit time slot (A-law/µ-law) compressed voice data or two contiguous time slot 16-bit two's complement linear voice data. The PCLK is a data clock supplied to the device that determines the rate at which the data is shifted in/out of the PCM ports. The FS pulse identifies the beginning of a transmit/receive frame and all time slots are referenced to it. For the Le9622 device, the frequency of the FS signal is 8 kHz. In Wideband mode, two evenly spaced sets of time slots are exchanged in each frame. The PCLK frequency can be a number of fixed frequencies as defined by the *VP-API-II*. Please refer to Figure 40, "Profile Wizard - Device Profile Configuration" on page 73 for an example setting of the Transmit and Receive Clock Slots, PCM Transmit Edge, and PCLK Frequency.

The *VP-API-II* allows the time slots to be offset to eliminate any clock skew in the system. The Transmit Clock Slot and Receive Clock Slot fields are each three bits wide to offset the time slot assignment by 0 to 7 PCLK periods. The Transmit and Receive Clock Slot is a global command that is applied at the device level. Thus, for each channel, two time slots must be assigned: one for transmitting voice data and the other for receiving voice data. Figure 4 shows the PCM highway time slot structure.

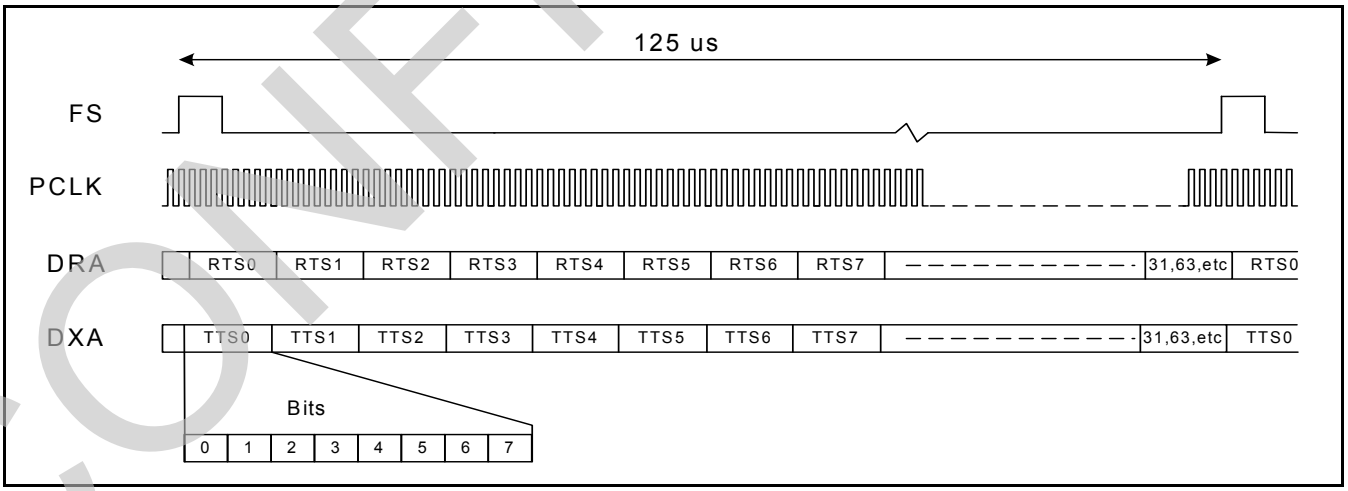



**Figure 4 - PCM Highway Structure**

#### 3.1.1.1 Transmit PCM Interface

The Transmit PCM interface receives an 8-bit compressed code (A-law/μ-law) or a 16-bit two's complement linear code from the voice signal processor (compressor). The transmit PCM interface logic (shown in Figure 5) controls the transmission of the data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The data can be transmitted on either edge of the PCLK, as selected in the *Device Profile*.

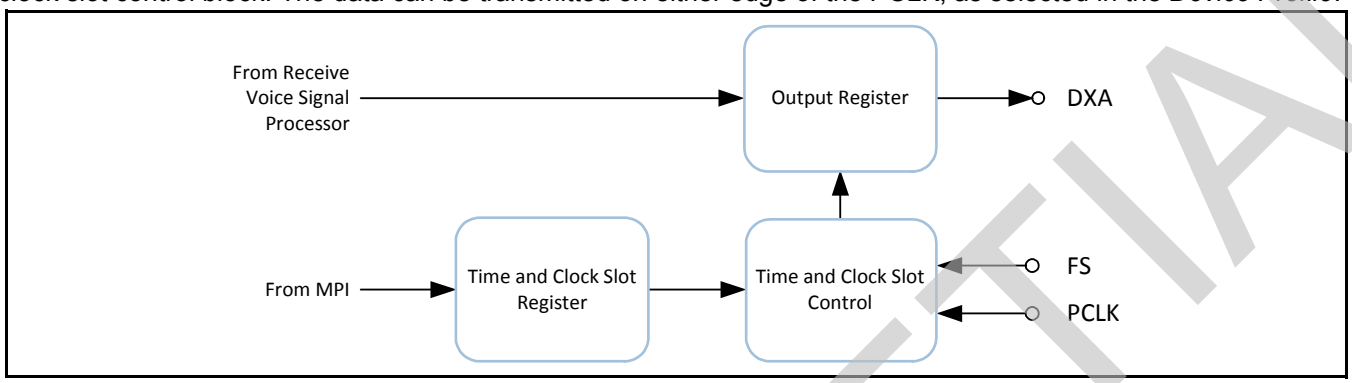



**Figure 5 - Transmit PCM Interface**

The *VP-API-II* allows the time slot of the selected channel to be programmed. The Transmit Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame, depending on the value of the PCLK frequency, the encoding scheme, and whether Narrowband or Wideband modes are selected. Refer to Table 1 below for the maximum number of available channels. Please note that linear mode requires two back to back time slots to transmit one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the number of transmit time slots as Narrowband linear mode.

| Audio Mode | Encoding | 1.024 MHz | 2.048 MHz | 4.096 MHz | 8.192 MHz |
|---|---|---|---|---|---|
| Narrowband (8 kHz sampling) | 8-bit compressed A-law/μ-law | 16 | 32 | 64 | 128 |
| | 16-bit linear | 8 | 16 | 32 | 64 |
| Wideband (16 kHz sampling) | 16-bit linear | 4 | 8 | 16 | 32 |

**Table 1 - Maximum Number of Transmit or Receive Channels**

#### 3.1.1.2 Receive PCM Interface

The receive PCM interface logic (see Figure 6) controls the reception of data bytes from the PCM highway. 8-bit compressed (A-law/μ-law) or 16-bit two's complement linear data is formatted and passed to the voice signal processor (expander).

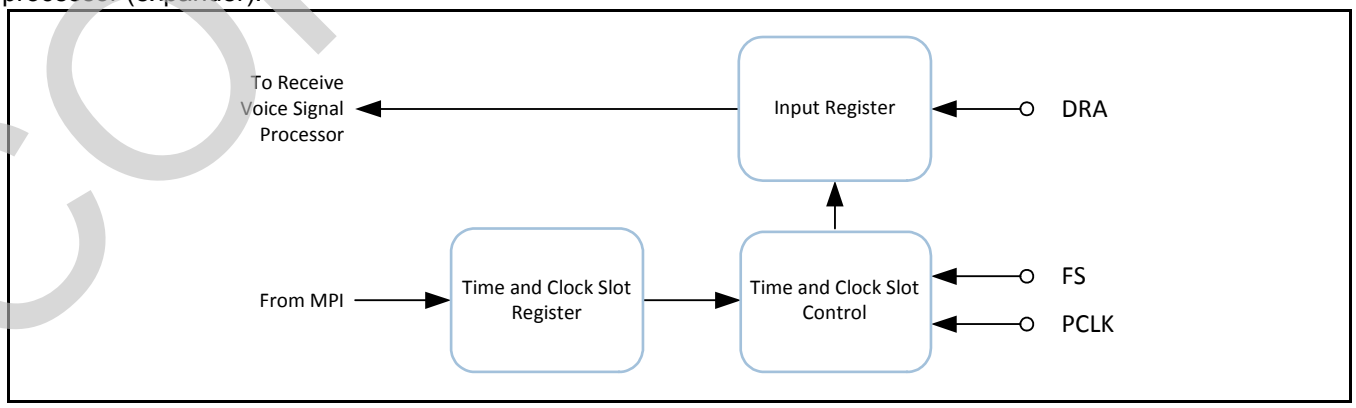



**Figure 6 - Receive PCM Interface**

The *VP-API-II* allows the time slot of the selected channel to be programmed. The Receive Time Slot Register is 7 bits wide and allows up to 128 8-bit time slots in each frame. Refer to Table 1 on page 13 for the maximum number of available channels. Please note that linear mode requires two back to back time slots to receive one voice channel. The data is transmitted in bytes with the most significant bit first. Wideband mode requires twice the numbers of receive time slots as Narrowband linear mode. Please refer to "VP-API-II Functions for Speech Coding" on page 20 for more details about setting the Codec mode and transmit and receive time slots. Figure 7 illustrates data flow on the PCM highway with data transmitted on the negative PCLK edge.

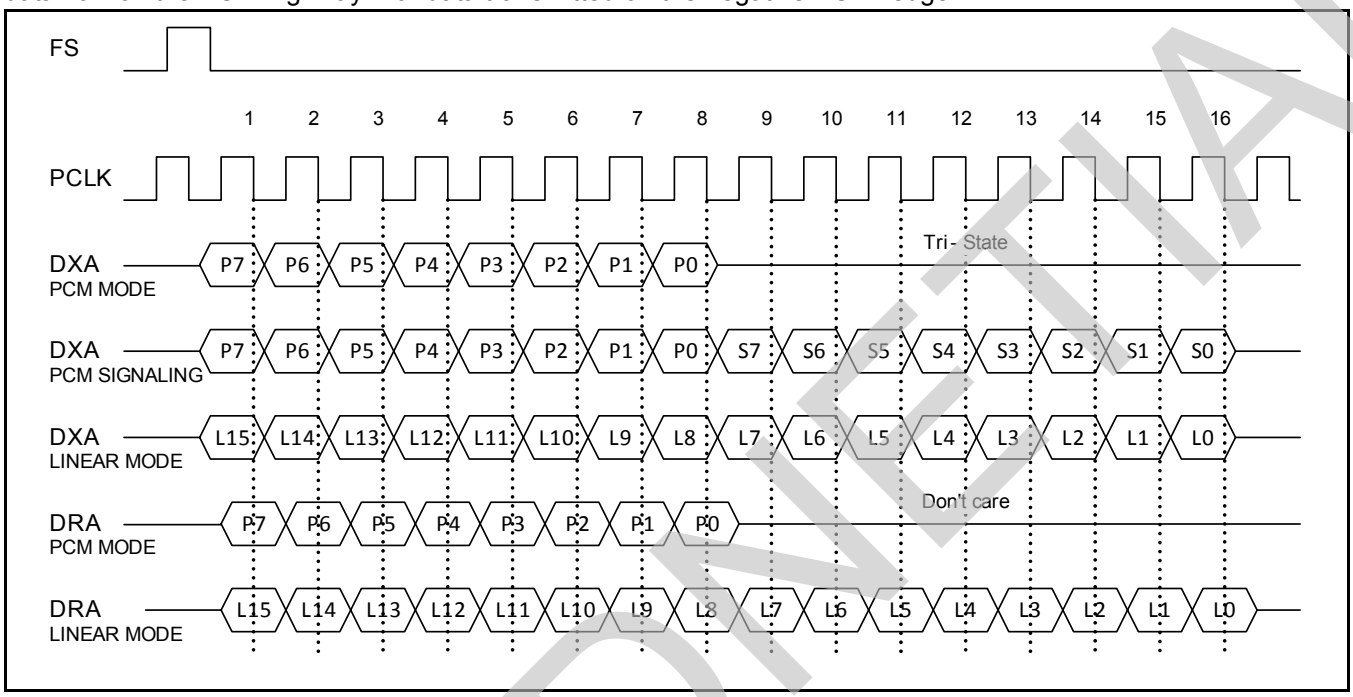



**Figure 7 - PCM Data Flow Transmit and Receive Data (Transmit Data on Negative PCLK Edge)**

### 3.1.2 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) block communicates with external VoIP processors over a flexible half-duplex synchronous serial interface. This port is always a slave to the host processor's SPI port which provides clocking, chip select and initiates transactions.

#### 3.1.2.1 SPI Signals

The SPI port physically consists of a serial data input (DIN) serial data output (DOUT), a data clock (DCLK), and a chip select ($\overline{CS}$).

| Signal Name | Type | Description |
|---|---|---|
| DCLK | Input | Serial Clock |
| $\overline{CS}$ | Input | Chip or Slave Select, active low |
| DOUT | Output | Master Input Slave Output |
| DIN | Input | Master Output Slave Input |

**Table 1 - SPI Interface Signals**

#### 3.1.2.2 Interrupt Signal

An optional interrupt signal ($\overline{INT}$) is available to alert the host processor that the device has status information. It is recommended that the $\overline{INT}$ signal be tied to an interrupt-generating pin on the host processor. If the interrupt signal is not used, the host processor will need to regularly poll the device.

### 3.1.2.3 SPI Connection Diagram

Figure 8 below shows a the standard 4-Wire SPI connection to the host processor. The optional $\overline{INT}$ signal is also shown here.

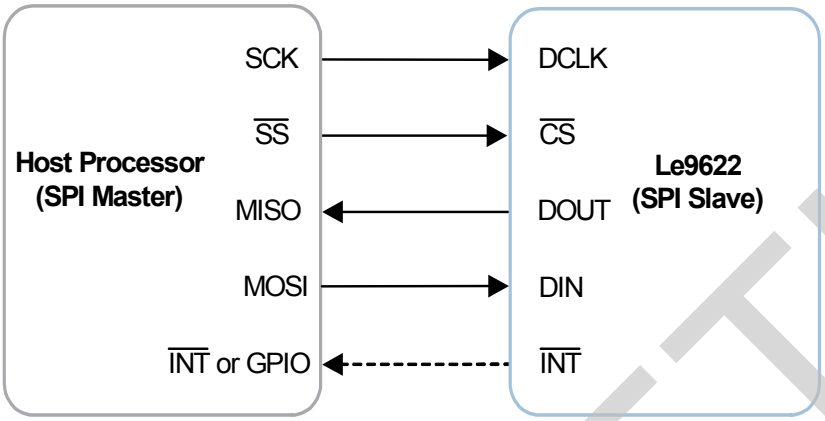



**Figure 8 - 4-Wire SPI Connection to Host Processor**

The Le9622 device also supports 2- and 3-wire variants of the SPI interface in case of limitations on the host's serial port. Contact *Microsemi CMPG Customer Applications* for more information.

### 3.1.2.4 Chip Select Settings

Three chip select settings are supported:

1. Low for each Byte or Word: $\overline{CS}$ goes inactive between bytes or words. This mode is compatible with the legacy MPI mode.
2. Command Framing: $\overline{CS}$ goes inactive on some command boundaries. Commands cannot be aborted in this mode. All required bytes are expected even if $\overline{CS}$ is de-asserted in the middle.
3. $\overline{CS}$ Hard-Wired Low: This can be used when the Le9622 device is the only slave on the SPI bus, but additional measures are required to acquire synchronization if it is ever lost.

Whenever $\overline{CS}$ goes inactive the bit state machine is reset. Also, if $\overline{CS}$ has not been active for *exactly* a multiple of 8 bit times, any byte which was partially received when $\overline{CS}$ goes inactive is ignored.

### 3.1.2.5 DCLK Polarity and Phase Settings

The SPI standards include four modes, defined by the polarity of DCLK and the phase relationship between data and DCLK. The clock polarity (CPOL) is determined by the idle state of DCLK. If the idle state is low, CPOL is 0. If the idle state is high, CPOL is 1. The clock phase (CPHA) is determined by which edge that data is valid. If the data is valid on the first edge of DCLK, CPHA is 0. If the data is valid on the second edge of DCLK, CPHA is 1.

The Le9622 device supports SPI Modes 0 (CPOL =0 and CPHA = 0) and 3 (CPOL =1 and CPHA = 1) and contains a logic block to automatically conform to the selected Mode. SPI Modes 1 (CPOL =0 and CPHA = 1) and 2 (CPOL =1 and CPHA = 0) are not supported.

Since the host processor is the master, it must place DCLK in the proper idle state before $\overline{CS}$ is asserted.

### 3.1.2.6 Length of Data Transactions

The SPI port on the Le9622 device supports 8-bit (byte-wide) transactions. 16-bit transactions are not supported.

### 3.1.2.7 SPI Interface Timing

Figure 9 below shows a typical timing interface diagram for SPI Mode 3.

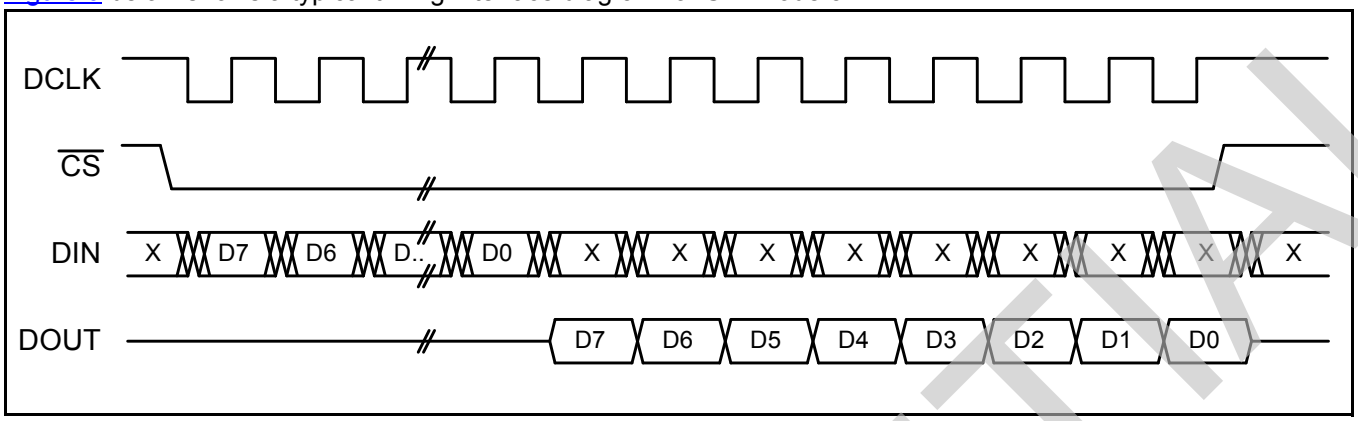



**Figure 9 - SPI Mode 3 Interface Timing**

### 3.1.2.8 MPI Interface

The Microprocessor Interface (MPI) is essentially a 4-Wire SPI Mode 3, with $\overline{CS}$ low for each byte and 8-bit data transactions. This interface has been historically used on numerous Microsemi devices.With the MPI interface, 8-bit commands can be followed with additional bytes of input data, or can be followed by the Le9622 device sending out bytes of data. All data input and output is MSB (D7) first and LSB (D0) last. All data bytes are read or written one at a time, with $\overline{CS}$ going high for at least a minimum off period before the next byte is read or written. Only a single channel should be enabled during read commands.

All commands that require additional input data to the device must have the input data as the next N words written into the device (for example, framed by the next N transitions of $\overline{CS}$). All unused bits must be programmed to 0 to ensure compatibility with future parts. All commands that are followed by output data will cause the device to output data for the next N transitions of $\overline{CS}$ going low. The Le9622 device will not accept any commands until all the data has been shifted in or out. The output values of unused bits are not specified.

Figure 10 shows an example MPI mode interface timing, with DOUT changing on the negative edge of DCLK. DIN is sampled on the rising edge of DCLK.

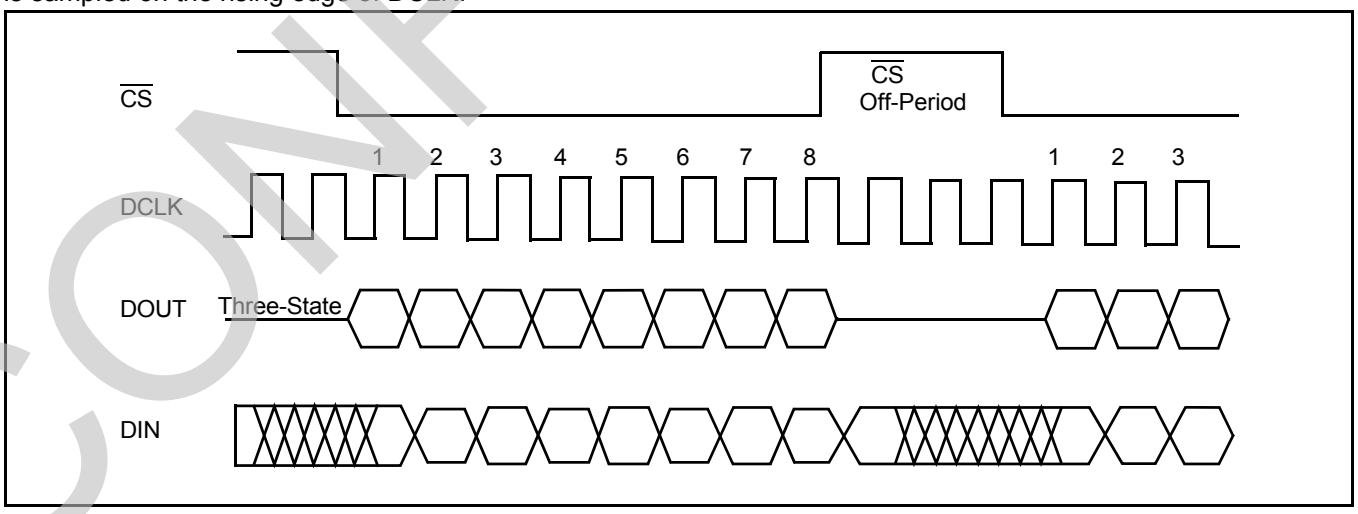



**Figure 10 - MPI Interface Timing**

An MPI cycle is defined by transitions of $\overline{CS}$ and DCLK. If the $\overline{CS}$ lines are held in the high state between accesses, the DCLK may run continuously with no change to the internal control data. Using this method, the same DCLK can be run to a number of Le9622 devices and the individual $\overline{CS}$ lines will select the appropriate device to access.

Between command sequences, DCLK can stay in a static state indefinitely with no loss of internal control information regardless of any transitions on the $\overline{CS}$ lines. Between bytes of a multi byte read or write command sequence, DCLK can also stay in a static high state indefinitely. If the host controller has a single bidirectional serial data pin, the DOUT pin of the Le9622 device can be connected to its DIN pin.

If a low period of $\overline{CS}$ contains less than 8 positive DCLK transitions, it is ignored. If it contains 8 or more positive transitions, the first 8 transitions will be interpreted as the first byte and the next 8 transitions will be treated as the second byte, etc. This allows the chip select input to be tied low permanently if desired.

## 3.2 Input / Output Block

The Le9622 device features two dedicated and two optional general purpose input / output (I/O) pins. $I/O1_1$ and $I/O1_2$ can be configured by the user as inputs, outputs, or as high current LED or relay drivers. $I/O2_1$ and $I/O2_2$ may be configured as general purpose digital inputs or outputs or as voltage sense pins (VS1 and VS2). When configured as inputs, $I/O2_1$ and $I/O2_2$ are capable of generating interrupts.

## 3.3 Voltage Sense

The voltage sense block allows the measurement of analog voltages at the pins VS1 and VS2, when they are configured as analog inputs. This makes it possible to monitor VSW and VBH or VBL in real time and make switcher optimizations based on their levels and to measure power consumption. An external 1.0MΩ, 1% resistor needs to be connected between each of these pins and the voltages to be measured.

### 3.4 Voice Signal Processor

This block, shown in Figure 11, performs digital signal processing for the transmission and reception of voice. It includes *G.711* compression/decompression, impedance matching, filtering, gain scaling, DTMF generation and general purpose tone generators for each channel. Additionally Caller ID (FSK and DTMF) and metering generation are provided.

This block performs the Codec and filter functions associated with the four wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band limit the voice signals.

The user-programmable filters perform the following functions:

- Sets the receive and transmit gain
- Performs the transhybrid balancing function
- Permits adjustment of the two wire termination impedance
- Provides frequency attenuation adjustment (equalization) of the receive and transmit paths

Country and standards specific *Profiles* are available from Microsemi with pre-computed digital filter coefficients. The PCM codes can be either 16-bit linear two's-complement or 8-bit companded A-law or µ-law.

The Le9622 device is architected in such a way as to reduce the real time demands on the host processor. An integrated cadencer/sequencer controls ringing and call progress tone generation. This feature can also generate timed interrupts and substantially reduces the user's need to implement time critical functions.

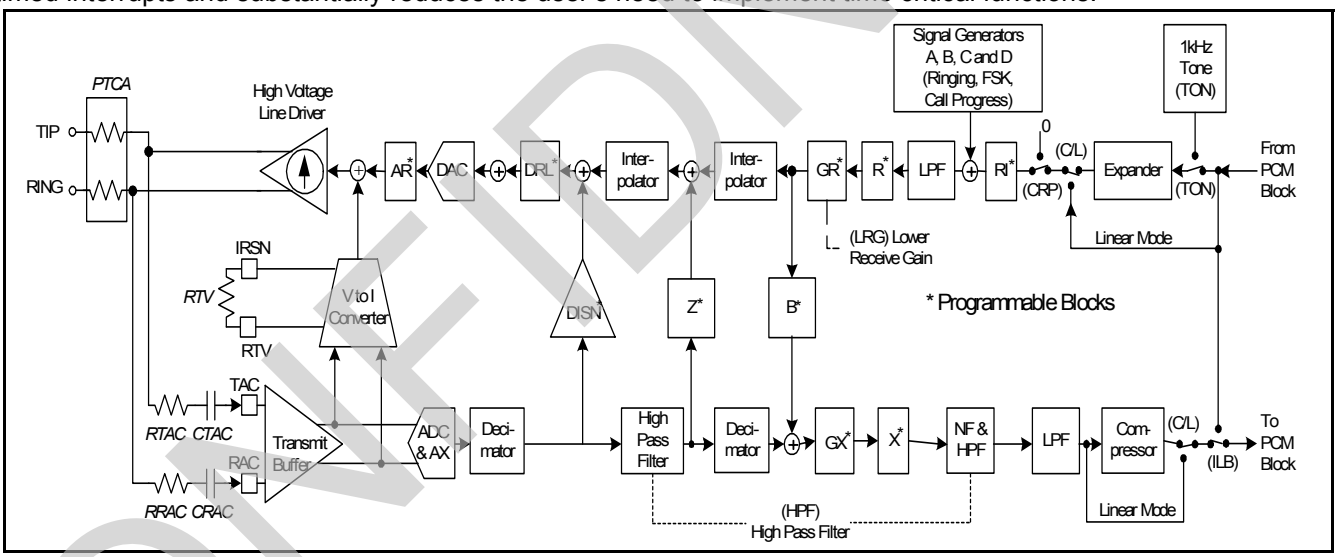



**Figure 11 - Voice Signal Processing Block Diagram**

### 3.4.1 Impedance Synthesis

The analog impedance synthesis loop is comprised of the SLIC block, the AC sense path components, the transmit amplifier, and a voltage to current converter. An external resistor, $R_{TV}$, synthesizes the nominal impedance in the analog domain. Additional refinement of the impedance is done in the DSP via the Digital Impedance Scaling Network (DISN) and Z-blocks.

The DISN path is comprised of the voice A/D and its first stage of decimation, a DISN, and the voice DAC. The 8-bit DISN synthesizes a portion of the AC impedance which appears in parallel with $R_{TV}$ and is used to modify the impedance set by the external analog network.

The Z Filter is a programmable digital filter providing an additional path and programming flexibility over the DISN in modifying the transfer function of the synthesis loop. Together $R_{TV}$, DISN, and the Z Filter enable the user to synthesize virtually all required telephony device input impedances.

### 3.4.2 Frequency Response Correction and Equalization

The voice signal processor contains programmable filters in the receive (R) and transmit (X) directions that may be programmed for line equalization and to correct any attenuation distortion caused by the Z Filter.

### 3.4.3 Transhybrid Balancing

The voice signal processor's programmable B Filter is used to adjust transhybrid balance. The filter has a single pole Infinite Impulse Response (IIR) section and an eight-tap Finite Impulse Response (FIR) section, both operating at 16 kHz.

### 3.4.4 Gain Adjustment

The transmit path of the FXS has two programmable gain blocks. Gain block AX is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2.0), located immediately before the A/D converter. GX is a digital gain block that is programmable from 0 dB to +12 dB, with a worst case step size of 0.1 dB for gain settings below +10 dB, and a worst case step size of 0.3 dB for gain settings above +10 dB. The filters provide a net gain in the range of 0 dB to 18 dB. The receive voice path has three programmable gain blocks. GR is a digital loss block that is programmable from 0 dB to 12 dB, with a worst case step size of 0.1 dB. DRL is a digital loss block of 0 dB or 6.02 dB. AR is an analog gain of 0 dB or 6.02 dB (unity gain or gain of 2) or a loss of 6.02 dB (gain of 0.5), located immediately after the D/A converter. This provides an attenuation in the range of 0 dB to 18 dB.

The gain adjustment block can also be accessed by a *VP-API-II* function directly, without using an *AC FXS Profile*.

| Function Name | Description |
|---|---|
| `VpSetRelGain()` | Adjusts transmit and/or receive gain up to +/-6 dB. Relative gain of 1 (0 dB) defined as initial value programmed by *AC FXS Profile*. Note that the supplied *AC FXS Profiles* have initial gains of -6 dBr receive and 0 dBr transmit |
| `VpSetOption()` | `VP_OPTION_ID_ABS_GAIN` -- Programs absolute gain |

**Table 2 - VP-API-II Functions for Gain Adjustment**

### 3.4.5 Transmit Signal Processing

In the transmit path (A/D) of the FXS, the AC Tip - Ring analog input signal is sensed by the TAC and RAC pins, buffered, amplified by the analog AX gain and sampled by the A/D converter, filtered, companded (for A-law or μ-law), and made available to the PCM blocks. If linear format is selected, the 16-bit data will be transmitted in two consecutive time slots starting at the programmed time slot. The B, X, and GX digital filter blocks are user-programmable digital filter sections. The first high-pass filter is for DC rejection, and the second high pass and notch filters reject low frequencies such as 50 Hz or 60 Hz.

### 3.4.6 Receive Signal Processing

In the receive path (D/A) of the FXS port, the digital signal is expanded (for A-law or µ-law), filtered, interpolated, converted to analog, and driven onto TIP and RING by the SLIC block. The AR, DRL, DISN, Z, R, and GR blocks are user programmable filter sections.

### 3.4.7 Speech Coding

The A/D and D/A conversion follows either the A-law or the µ-law standard as defined in *ITU-T Recommendation G.711.* Alternate bit inversion is performed as part of the A-law coding. Linear code is an option on both the transmit and receive sides of the device. Two successive time slots are required for linear code operation. The linear code is a 16-bit two's-complement number which appears sign bit first on the PCM highway.

### 3.4.8 Wideband Operation

Each channel on the Le9622 device can be set to operate in either Narrowband or Wideband mode under *VP-API-II* software control. In the Wideband mode, the nominal voice bandwidth is expanded and starts at 50 Hz or 200 Hz (depending on whether or not a high-pass and 50/60 Hz notch filter is enabled) to 7000 Hz to provide better voice quality. The *AC FXS Profiles* must be programmed with wideband coefficients. In the Wideband mode, the increased data rate is processed by accessing a second set of timeslots equally spaced in the frame.

| Function Name | Description |
|---|---|
| `VpSetOption()` | `VP_OPTION_ID_TIMESLOT` -- Programs transmit and receive timeslot.<br>`VP_OPTION_ID_CODEC` -- Programs speech coding mode. |
| `VpGetOption()` | `VP_OPTION_ID_TIMESLOT` -- Retrieves current values of transmit and receive timeslot.<br>`VP_OPTION_ID_CODEC` -- Retrieves current speech coding mode. |

**Table 3 - VP-API-II Functions for Speech Coding**

## 3.5 Signal Generation

Up to four programmable digital signal generators are available for the FXS channel. These signal generators can be programmed for multi-tone generation, amplitude and frequency modulation, and or the generation of complex sine, triangular or trapezoidal signals.

### 3.5.1 Multi-Tone Generation

In this configuration, up to four tone generators are summed into the output path, as shown in Figure 12 on page 21. The Bias generator produces a DC bias that can be used to provide DC offset during ringing or DC test signals during diagnostics. This generator is automatically enabled when entering the `VP_LINE_RINGING` state.

| Function Name | Description |
|---|---|
| `VpSetLineTone()` | Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually to provide Special Indication Tone (SIT). |
| `VpSetLineState()` | `VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` -- Uses Signal Generator A (and B for trapezoidal type ringing) with user selected frequency, offset, amplitude, and type. |
| `VpSendSignal()` | `VP_SENDSIG_DTMF_DIGIT` -- Generates a DTMF digit on the line. |
| `VpInitCid()` | Sending Caller ID (FSK and DTMF message data supported) on an FXS line.<br>Providing Type 2 CID Alerting tone. |
| `VpSendCid()` | |
| `VpContinueCid()` | |

**Table 4 - VP-API-II Functions Using Signal Generators**

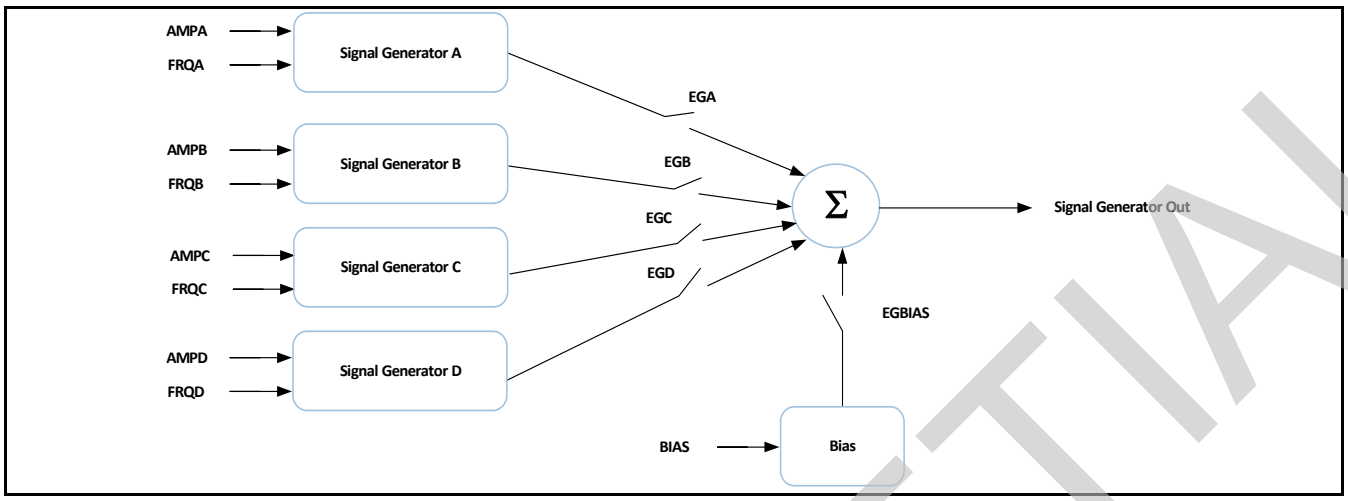



**Figure 12 - Multi-Tone Generation**

Signal Generator A is also used by the *VeriVoice* test suites to produce slow ramps. This allows a complex sequence of diagnostic test voltages to be generated in a controlled manner without generating unwanted transients on the line.

Each generator has independent frequency and amplitude parameters. The frequency accuracy is basically the same as the crystal accuracy of the system.

The EGA/B/C/D bits are controlled by the *VP-API-II* Cadencing engine.

### 3.5.2 Frequency and Amplitude Modulation

The signal generators can also be used to generate frequency and/or amplitude modulated tones in conformance with worldwide Howler (receiver off-hook) and call progress tone requirements. Frequency modulation is performed in a dedicated hardware block, while amplitude modulation is performed in software by *VP-API-II*.

To generate frequency modulated tones, Signal Generator A is configured as a modulator, while Signal Generator D is configured as a carrier. The output of Signal Generator A is the frequency input to Signal Generator D as shown in Figure 13. Note that Signal Generator A needs a positive DC bias so that its output is always positive. Caller ID generation is not available while frequency modulation is taking place. Note that Signal Generators B and C are available to be summed to the frequency modulated signal, if necessary.

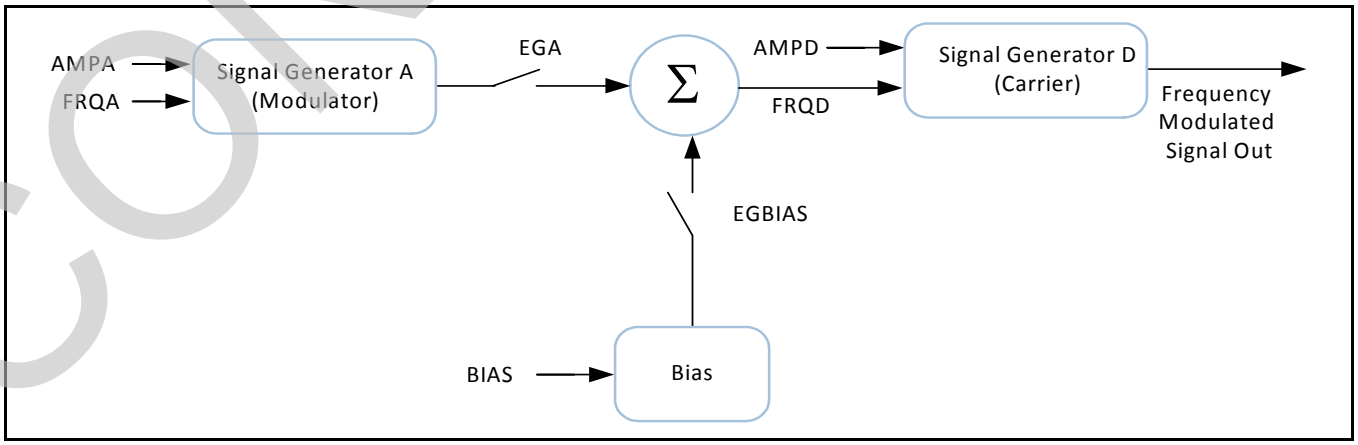



**Figure 13 - Frequency Tone Modulation**

Frequency and amplitude modulation allow the Le9622 device to meet exacting Howler tone requirements such as those specified in *BTNR 1080 Version 15* and *Draft 960-G*, *NTT Edition 5* and *Austel AUS002:2001*.

Table 5 lists the *VP-API-II* functions that are used for Howler tone generation.

| Function Name | Description |
|---|---|
| `VpSetLineState()` | `VP_LINE_HOWLER` -- Places the device in a high gain state for Howler tone generation. |
| `VpSetLineTone()` | Provides simultaneous generation of up to four tones. Note that with Tone Cadencing, tones can be enabled/disabled individually or modulated in order to generate Howler tones. |

**Table 5 - VP-API-II Functions for Howler Tone Generation**

### 3.5.3 Triangular and Trapezoidal Signal Generation

The signal generators can also be used to generate trapezoidal waveforms for ringing. Figure 14 shows a configuration that is typically used to generate trapezoidal waveforms. Triangular waveforms can also be generated.

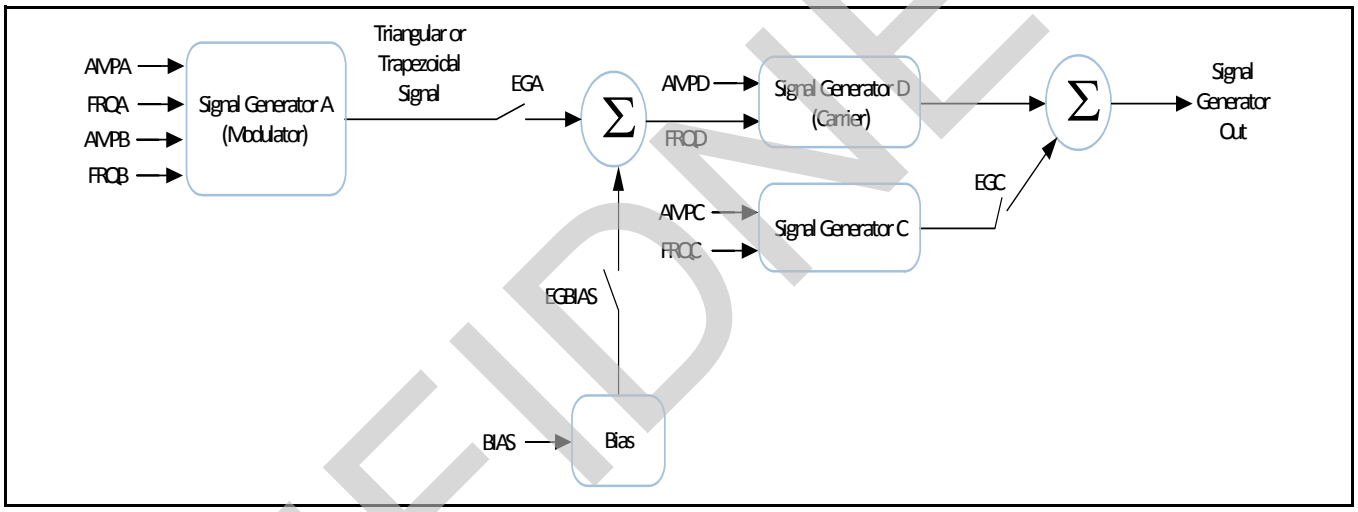



**Figure 14 - Trapezoidal Signal Generation**

## 3.6 Low Power DC Feed

The Le9622 device supports *Low Power Idle Mode (LPIM)*, which reduces the system power consumption during idle (On-Hook) state. *LPIM* provides a weak DC feed capable of at least 5 mA to the line and reacts to a change in the line voltage to create an off-hook indication when a telephone goes off-hook.

## 3.7 Normal DC Feed

DC feed is active in normal idle, talk and ringing states and the programmed characteristics appear between Tip and Ring. VAS is chosen to ensure that sufficient headroom is available for the amplifiers when on-hook to support On-Hook Transmission with the programmed open circuit (VOC) voltage. The parameters that control DC feed are summarized in Table 6 on page 23. Their values are determined by the *VP-API-II* using the `VpCalLine()` function to ensure circuit performance. In addition, the *VP-API-II* handles some internal programming depending on the selected VOC voltage.

| Parameter | Range | Description |
|---|---|---|
| ILA | 20 – 30 mA | Sets the current limit for DC feed |
| VOC | 12 – 57 V | Sets open circuit DC feed voltage.<br>Two ranges, 12 - 33 V and 36 - 57 V are supported |
| VAS | 1.5 – 7.25 V | Allows for some programmability for the automatic battery switching point |
| ABSCAL | -5.25 – +5.25 V | Allows calibration of the battery switching point per channel |
| bshv | 1.0 – 7.0 V | Battery switch hysteresis voltage |

**Table 6 - DC Feed and Battery Switch Programmable Parameters**

The DC Profile produces a DC feed curve at Tip and Ring when the fuse resistors are inside the feedback loop formed by the RTDC, RRDC feedback network. Note that the value of the combined Tip and Ring feed resistors Rfeed is programmable to 0, 50, 100, or 200 Ω to correspond to the choice of PTCs or fuse resistors that are used. Please refer to Figure 15 below for the active state I/V feed curve for Rfeed = 200 Ω.

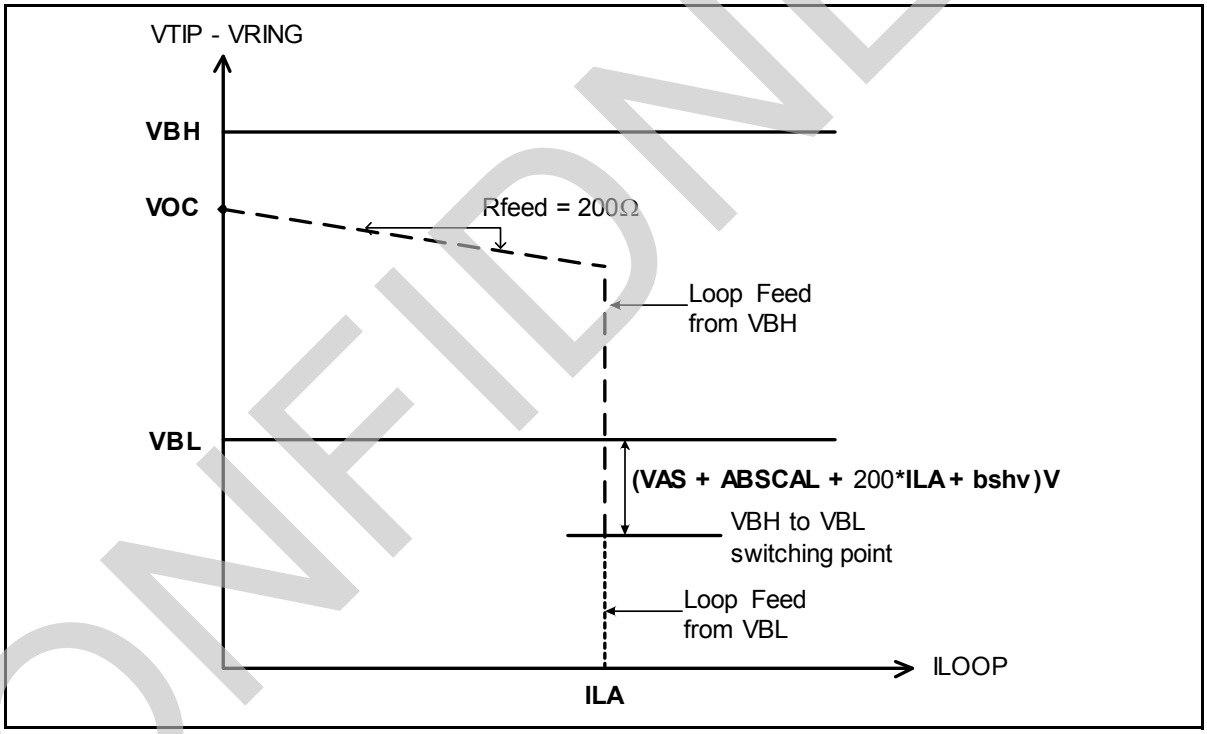



**Figure 15 - Normal DC Feed I / V Characteristic**

Figure 41, “Profile Wizard - DC Profile Configuration Example” on page 75 shows typical DC feed parameters.

### 3.8 Test Feed

The Tip Open test state presents the DC feed characteristic shown in Figure 15 between the Ring lead and ground.

## 3.9 Ringing

The Le9622 device supports balanced ringing.

### 3.9.1 Balanced Ringing

Internal balanced ringing drives the subscriber line with balanced ringing voltage waveforms (see Figure 16). In the balanced ringing mode, the ringing signal is driven differentially, thus maximizing the ringing signal swing. In this mode, the SLIC appears to the subscriber line as a voltage source with an output impedance of 200 Ω. The maximum ringing signal possible in the balanced mode for the Le9622 is $100V_{PK}$ corresponding to the maximum AC + DC voltages.

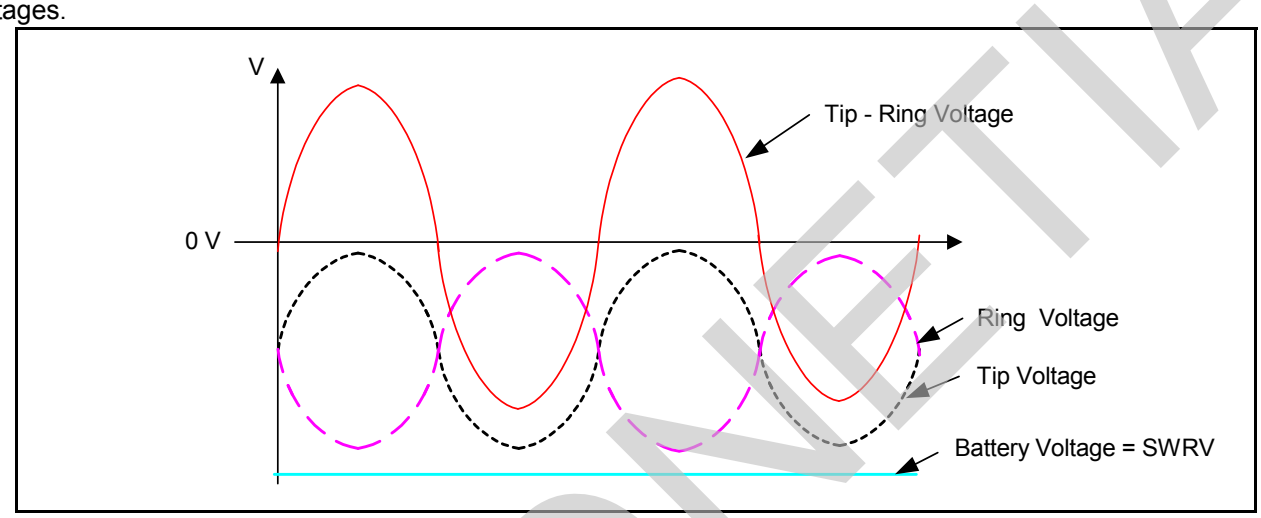



**Figure 16 - Balanced Ringing with Fixed Supply**

### 3.9.2 Adaptive Ringing Amplitude

The Le9622 device supports adaptive ringing amplitude, which limits the maximum power that is generated by the device during ringing at or below a specified level. This will contribute to greater power efficiency and will avoid the thermal shutdown of the device or ringing stoppage when driving heavy loads.

### 3.9.3 Switch Hook Detection

The FXS supervision circuits of the Le9622 device provide debounced off-hook indications to an external processor via the host port interface. The supervision circuit compares a scaled version of the Tip-Ring current to a programmed off-hook threshold, TSH. The output of the comparator is debounced by a programmable debounce timer, DSH. A debounced *Off-Hook* indication generates an interrupt to the host processor.

### 3.9.4 Ring Trip Detection

Ring trip is the process of sensing a subscriber's off-hook event during ringing. This is accomplished by sensing the rise in loop current which occurs when a phone goes Off-Hook. The Le9622 device can detect ring trip when the ringing signal is purely AC and/or when the ringing signal has a DC bias on it. To do so, the ring trip algorithm is automatically altered internally by the Le9622 device based on the user-programmed parameters.

The ring trip detector uses the Tip-Ring current as an input. This current is rectified so that AC + DC ring trip can be detected. The output of the rectified signal is compared to a programmable ring trip threshold and the output is digitally debounced. The output is blanked upon ring entry to avoid false ring trips.

The ring trip detection circuit provides debounced ring trip indications to an external processor via the host port interface. The ring trip circuit compares a scaled version of the Tip-Ring current to a programmed Ring Trip Threshold (RTTH). The output of the comparator is processed by the ring trip algorithm on a cycle by cycle basis to

provide immunity to false ring trips. In addition, spending more than 50% of the time in ringing current limit will generate a trip indication. A positive ring trip occurs if a trip indication is present for one (optional) or two (default) complete ring cycles, and an interrupt can be raised to the host processor. For AC-only ringing, the signal is half-wave rectified.

The Ring Trip Threshold (RTTH), integration method (positive half-wave for AC only or full-wave for AC+DC), the number of cycles (1 or 2), and Ringing Current Limit (ILR) are programmed in the *Ringing Profile*. Microsemi provides a number of example *Ringing Profiles* for most common ringing requirements incorporating the ringing signal parameters and corresponding ring trip settings.

The following equations can be used to select new ring trip settings when using different ringing waveforms and different loads. They allow the ratio of the open circuit ringing voltage to the ringing threshold current to vary by +/-20%, which is conservative.

| Name | Description |
|---|---|
| AMPA | Amplitude of signal generator A which is used for ringing |
| FREQA | Frequency of signal generator A which is used for ringing |
| BIAS | DC bias for ringing |
| RTDCAC | Ringing trip based on AC only or Battery Backed (DC) Ringing |
| RTTH | Ringing trip threshold in 0.5 mA steps from 0 to 63.5 mA |
| ILR | Ringing current limit programmed in 2 mA steps. ILR=0 represents 50 mA. ILR = 31 represents 112 mA |
| HOOK | Interrupt in signalling register indicating a ring trip occurred |

**Table 7 - Ring Trip Parameters**

For AC only ringing, RTDCAC is 1 and the ringing current is half-wave rectified and averaged over a ringing cycle. If this result exceeds the RTTH threshold for two successive cycles, the HOOK bit will be set. This method limits the supported loop length x depending on the minimum must not trip ringing impedance (Rmnt in Ohms) and allowing for errors in the applied ringing voltage and trip level. The maximum loop resistance is given by:

$$RLOOP(max) = 0.67 \times Rmnt - Rphone - 66\Omega$$

RLOOP (max) excludes the DC resistance of the phone (Rphone, typically 430 Ω in the U.S.), and the fuse resistance if DC line sensing is behind the fuse resistors.

For a sinusoidal ringing waveform of VRING (RMS) volts, and Rmnt impedance, the following ring trip settings should be used:

$$RTTH = \frac{0.54 \times VRING}{Rmnt + 200\Omega}$$

$$ILR = \frac{1.4 \times VRING}{Rmnt + 200\Omega}$$

In general for short loop applications, it is recommended to use AC ring trip even in the presence of a DC bias that could allow a DC based ring trip, and the above equations still apply. Note that the ringing source impedance is nominally 200 Ω.

## 3.10 Subscriber Line Testing

The Le9622 device provides the ability for the user to perform the *Telcordia GR-909-CORE / TIA-1063* diagnostic testing for the voice ports. In Test mode, a variety of input signals can be read from the voice ADC converter. These signals include the switching regulator voltage and the line DC and AC voltages.

### 3.10.1 VeriVoice Professional Test Suite Software

*VeriVoice Professional Test Suite Software* is an advanced test suite featuring the following tests:

- Line Voltage: Checks for hazardous and foreign AC and DC voltages.
- Receiver Off-Hook: Checks for longitudinal fault, off-hook resistive fault and receiver off-hook.
- Regular REN: Tests the impedance of the line and returns a fail if the Ringer Equivalence Number (REN) is too low or high.
- Electronic REN: Provides REN Tip to Ring, Tip to ground and Ring to ground based on capacitance
- Resistive Fault: Measures three-element resistance.
- GR-909-CORE / TIA-1063: Performs all of the *GR-909-CORE* outward tests in the correct sequence.
- Capacitance: Measures three element capacitance
- Master Socket: Detects master socket terminations
- Cross Connect: Detects cross connected FXS
- Loop back: Enables receive-to-transmit signal loop-back using two different methods
- Read Loop Conditions: Measures DC voltages between Tip and Ring, Tip to ground, Ring to ground, and
- VBAT to ground. Also measures metallic and longitudinal DC line currents in supported States.
- Read Battery Conditions: Reads the battery voltages connected to the line circuit.
- DC Voltage Self-Test: Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit.
- DC Feed Self-Test Measures the voltage and current across a known internal test termination using the *DC Profile* that has been programmed.
- Ringing Self-Test Verifies ring signal generation, drive capability, and ring trip.
- On/Off-Hook Self-Test Creates on-hook and off-hook conditions on the line using the internal test termination and verifies that they are properly reported.
- Draw and Break Dial Tone Verifies the capability of the line circuit to detect off-hook and on-hook as well as the voice path to/from the host
- Read Loop Conditions - Extended Reads the loop conditions of the current state of the line without disturbing the T/R feed conditions. Measures AC and DC voltages Tip and Ring, Tip to ground and Ring to ground. Measures VBAT to ground. Also measures metallic and longitudinal AC and DC line currents in supported States.

## 3.11 Manufacturing Testing

The Le9622 is supported by the *VeriVoice Manufacturing Test Package (VVMT),* a platform-independent 'C' source code module which facilitates factory testing and calibration of assembled boards with this and other Microsemi voice products.

## 3.12 Metering

The Le9622 device is capable of 0.5 $V_{RMS}$ metering into a 200 Ω metering load at either 12 kHz or 16 kHz. Smooth metering application and abrupt metering application are supported. A typical metering sequence is shown below in Figure 17.

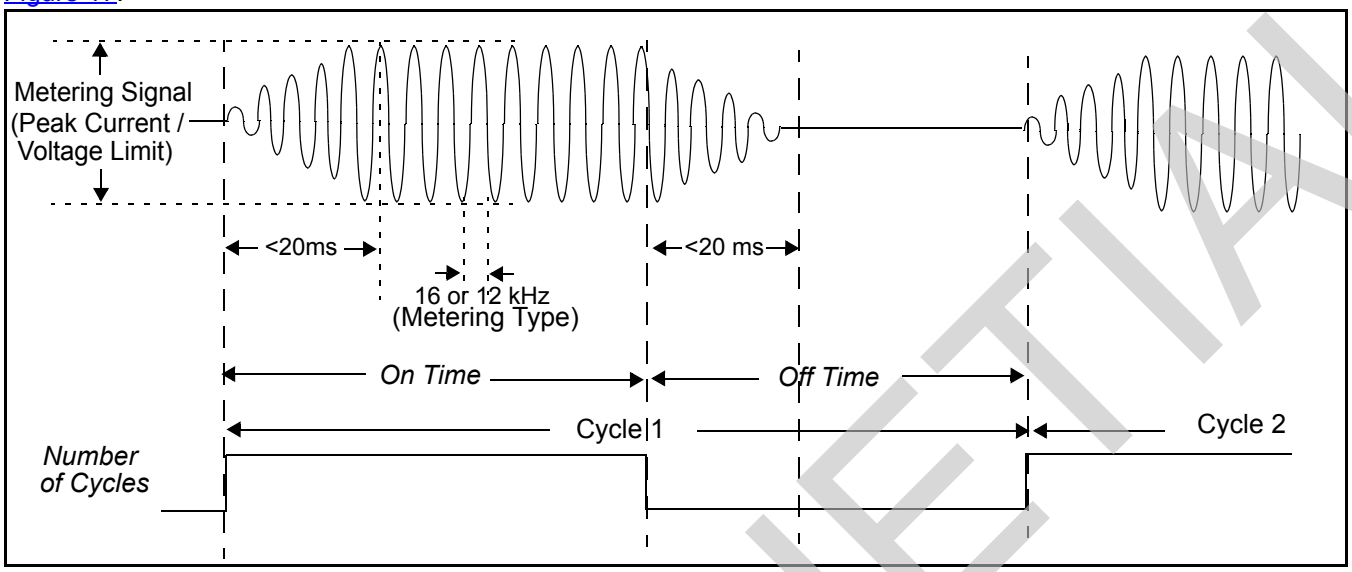



**Figure 17 - Metering Pulse Definitions**

The metering on time, off-time, and number of cycles are programmed in the *VP-API-II* function `VpStartMeter()`. This off-loads much of the timing from the host processor. Note that a ramp up / ramp down period of up to 20 ms is possible. The metering type (12 or 16 kHz), peak current and voltage limit are set in the *Metering Profile* and are used by the *VP-API-II* function `VpInitMeter()`. Note that in a normal configuration, some of the metering current flows into the CTD and CRD capacitors, so that the current sourced into an external load will be less than that programmed peak current parameter even when the metering voltage limit is not reached. The metering voltage that reaches the load is also dependent on the total fuse resistance and the minimum load resistance, which is typically 200 Ω

## 3.13 Switching Regulator Controller

### 3.13.1 Buck Boost Automatic Battery Switch (BBABS)

The BBABS switching regulator circuit uses an inverting buck-boost inductor based architecture with voltage doubler that regulates off of the low battery supply. The switching regulator controller and the external power train circuitry provide a flexible switching regulator that automatically produces the negative supply voltages required to drive each line. The controller detects over current events and terminates the output pulse on a cycle by cycle basis. The circuit uses +12V for VSW.

The switching regulator has three modes of operation: Low, Medium, and High, which roughly correspond with On-Hook, Off-Hook, and Ringing states. These modes of operation provide for increased efficiency over a wide load range. In Low Power mode the switcher produces maximum efficiency in the idle condition while providing up to one watt of output power capability. In Medium Power mode the switcher provides greater power without significant sacrifice of efficiency. In High Power mode, which is usually of short duration, the switching regulator supports up to 10 watts of output power.

Switching regulator parameters are set in the *Device Profile.*

The Le9622 controller supports the patented BBABS switching regulator circuit as shown in 8.2, “Patented BBABS Switching Regulator Circuit“ and 8.2.2, “BBABS Switching Regulator Circuit Bill of Materials (for VBATH 95V Maximum)“. The regulator is an inductor based inverting buck-boost configuration with output voltage doubler. The circuit adds the applied VSW voltage to the doubled battery voltage. The BBABS switching regulator circuit has

been crafted for extremely low cost by using low cost, low voltage components while maintaining high performance and high efficiency. The switching regulator circuit is capable of simultaneous ringing of both lines without clipping. The control switching frequency for BBABS is 24 kHz for Low Power mode and 128 kHz for Medium and High Power modes.

Switcher Y has been configured to generate one fixed supply voltage, low battery voltage VBATL. The VBATL value is programmable. The VBATL supply is regulated but the switching circuit provides good VBATH regulation when VBATL is loaded. VBATH is obtained by the formula:

VBATH = -(VSW + (2 * |VBATL|) – 2 V).

VBATL can be programmed to a low value for supervision and active states and can be programmed to a high value to perform ringing. With a VSW of +12 V, a VBATL setting of -25 V produces a VBATH of -60 V, these voltages are adequate for line supervision and active off-hook operation. VBATL can be increased to -35 V to produce a VBATH of -80 V and open circuit ringing of 50 $V_{RMS}$; or VBATL can be increased to -40 V to produce a VBATH of -90 V and open circuit ringing of 60 $V_{RMS}$. For the short period of time that one channel is ringing, the adjacent channel will consume more power due to the elevated battery voltages, but overall performance in that channel will not be affected. VBATH is applied to the VBH device pin and VBATL is applied to the $VBL_1$ and $VBL_2$ device pins.

For BBABS operation the VDDSW pin needs to be tied to DVDD (3.3 V).

### 3.13.2 Multi-Line Inverting Boost Automatic Battery Switch (ABS)

Le9622 can be expanded to support 4 to 8 FXS channels using Microsemi's Multi-line Inverting Boost topology. The multi-line design uses two independent inverting boost DC/DC converters to create the VBATL and VBATH battery supplies. Each supply is optimized for its for best efficiency and cost. The advantage to this topology versus a multi-output flyback design is that the battery voltages are independent and not restricted by the transformer turns ratio. The design also uses off the shelf inductors instead of a custom transformer. The supplies are designed to operate from a nominal 12V +/-2V supply.

The VBATL supply is usually -25V to -35V. VBATL is used to supply power when the device is in the active state. Each line typically requires about 26mA (25mA ILA + 1mA overhead) when off hook. The VBATL supply can be cost optimized to support 4 lines or with some component upgrades it can easily support 8 lines. The value of VBATL can be adjusted higher to allow support to longer loops. A typical application would set VBATL to -30V. This will allow a maximum loop resistance of 800ohms assuming loop current is limited to 25mA. The VBATL supply must be able to support a continuous load of 1W per FXS line.

The VBATH supply is usually -80V to -90V, but can be as high as -115V. The value of VBATH is set based on the maximum peak ringing voltage required. It is recommended that VBATH be set to 5V greater than the maximum expected open circuit ringing voltage. For example, 50Vrms ringing (70Vpk) requires a minimum VBATH of -75V. A -115 VBATH is enough to support 60Vrms+20Vdc which is a typical USA ringing requirement. Output voltages in excess of -90V would require some component ratings to be increased. For an 8 line application, the VBATH supply can normally support 4 lines ringing up to 5REN each at the same time. For a 4 line application, the VBATH supply can easily support 2 lines ringing.

## 3.14 Charge Pump Regulator and MOSFET Gate Driver

The Le9622 device features an internal charge pump regulator to generate a supply voltage suitable to drive a wide range of external MOSFETs. The charge pump regulator steps up the DVDD voltage to a value required by the MOSFET supply (VDDSW) to drive a logic level MOSFET (between 4.3 V to 5 V). The charge pump regulator has an output under voltage protection circuit with a threshold about 0.2 V below the target voltage. The internal charge pump voltage is filtered by an external capacitor at the VDDSW node. For any other use or connection to VDDSW, contact Microsemi Customer Applications.

The charge pump converter configuration is selected in the Device Profile.

# 4.0 Electrical Specifications

## 4.1 Absolute Maximum Ratings

Stresses above those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

| | |
|---|---|
| Storage Temperature | $-55°C < T_A < +125°C$ |
| Ambient temperature, under Bias | $-40°C < T_A < +85°C$ |
| Ambient relative humidity (non condensing) | 5 to 95% |
| VBH, $VBL_1$, $VBL_2$ with respect to GND | –125 $V_{DC}$ to +0.5 $V_{DC}$ |
| VBH w/ respect to GND (both lines active VBL, $VBL_i$< \|-50\| | –160 $V_{DC}$ to +0.5 $V_{DC}$ |
| AVDD, DVDD, VDDHPI voltages with respect to GND | –0.4 $V_{DC}$ to + 4.0 $V_{DC}$ |
| AVDD voltage with respect to DVDD | –0.4 $V_{DC}$ to + 0.4 $V_{DC}$ |
| $I/O1_1$, $I/O1_2$ current sink to GND (1) | 70 mA |
| $TIPD_i$ or $RINGD_i$ voltage with respect to GND (continuous) | VBH – 1 $V_{DC}$ to + 1.0 $V_{DC}$ |
| $TIPD_i$ or $RINGD_i$ voltage with respect to GND (10 ms, F = 0.1Hz) | VBH – 5 $V_{DC}$ to + 5.0 $V_{DC}$ |
| $TIPD_i$ or $RINGD_i$ voltage with respect to GND (1 µs, F = 0.1Hz) | VBH – 10 $V_{DC}$ to + 10 $V_{DC}$ |
| $TIPD_i$ or $RINGD_i$ voltage with respect to GND (250 ns, F = 0.1Hz) | VBH – 15 $V_{DC}$ to + 15 $V_{DC}$ |
| $TIPD_i$ or $RINGD_i$ current (continuous) | ± 150 mA |
| $TIPD_i$ or $RINGD_i$ current (1 µs) | ± 400 mA |
| Latch up immunity (any pin) | ± 100 mA |
| Maximum device junction temperature | +145°C |
| Maximum device power dissipation, continuous (2)- $T_A$ = 85°C<br>$P_D$ | 1.5 W |
| Junction to ambient thermal resistance (1)<br>$\theta_{JA}$ | 29°C/W |
| Junction to board thermal resistance (1)<br>$\theta_{JB}$ | 9°C/W |
| Junction to case thermal resistance(1)<br>$\theta_{JC}$ | 12.1°C/W |
| Junction to top characterization parameter (1, 2)<br>$\Psi_{JT}$ | 0.9°C/W |
| Reflow temperature, 10 sec., MSL3, per *JEDEC J-STD-020* | 260°C |
| ESD immunity (Human Body Model) | *JESD22 Class 1C* compliant |

***Notes:***

*1. See "Thermal Performance"*

*2. Above SLIC*

## 4.2 Thermal Performance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to a large internal copper plane. Thermal performance depends on the number of PCB layers and the size of the copper area. Please refer to Microsemi's application note *QFN Package (Document ID#: 080791)* for general design and layout guidelines.

The thermal specifications in "Absolute Maximum Ratings" assume that the device is mounted on a highly effective thermal conductivity test board (4 layers, 2s2p) per *JEDEC JESD51-7* and *JESD51-5*, and featuring the recommended 7x7 array of thermal vias shown in Figure on page 83.

## 4.3 Operating Ranges

Microsemi guarantees the performance of this device over industrial (-40ºC to 85ºC) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the *Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.*

### 4.3.1 Recommended Operating Conditions

| | |
|---|---|
| Ambient temperature | -40°C < $T_A$ < +85°C |
| Ambient relative humidity | 15% to 85% |
| GND | 0 $V_{DC}$ |
| AVDD with respect to GND | +3.3 $V_{DC}$ ± 5% |
| DVDD with respect to AVDD | ±50 $mV_{DC}$ |
| VDDHPI with respect to GND | +1.71 $V_{DC}$ to DVDD |
| VDDSW with respect to GND (Inverting Boost ABS) | +4.3 $V_{DC}$ to +5.0 $V_{DC}$ |
| VDDSW with respect to GND (BBABS) | +3.3$V_{DC}$ ±5% |
| VBH (both lines active VBL, $VBL_i$ < \|-50\| V) | –150 $V_{DC}$ to – (VOC + 7.0) $V_{DC}$ |
| VBH (all other states) | –120 $V_{DC}$ to – (VOC + 7.0) $V_{DC}$ |
| $VBL_i$ (in active states) | VBH to – 20 $V_{DC}$ |
| VBH with respect to $VBL_i$ | 0 $V_{DC}$ ≤ ($VBL_i$ – VBH) < 90 $V_{DC}$ |
| Digital pins, except $I/O1_i$, $I/O2_i$ | GND to VDDHPI |
| $I/O1_i$, $I/O2_i$ | GND to DVDD |
| Analog pins | GND – 0.3 $V_{DC}$ to AVDD +0.3 $V_{DC}$ |

# 5.0 Electrical Characteristics

## 5.1 Test Conditions

Unless otherwise noted, test conditions are:

- Typical values are for $T_A$ = 25ºC and nominal supply voltages. Minimum and maximum values are over the temperature and supply voltage ranges shown in"Recommended Operating Conditions" on page 30, except where noted
- Default (unity) gain in X, R, DRL, AX and AR blocks; default coefficients in DISN, Z and B filters
- Battery voltage for BBABS operation:
  - Active and Idle states: $VBAT_3$ = -60 V and $VBAT_{1/2}$ = -25 V
  - Ringing state: $VBAT_3$ = -80 V and $VBAT_{1/2}$ = -35 V
- DC feed programmed and calibrated to:
  - BBABS operation: ILA = 25 mA, VOC = 48.0 V, bsov = 2.92 V, and bshv = 5 V
- AC and DC load resistance $R_L$ = 600 Ω
- Fuse resistors for device tests are $R_F$ = 14 Ω
- 0 dBm0 = 0 dBm (600 Ω) = 0.775 $V_{RMS}$. Digital gains GX0 and GR0 to achieve 0 dBr relative levels are GX0 = +6.797 dB (7A20h) A-law or linear and GX0 = +6.737 dB (2A20h) µ-law to set A/D transmit gain to 0dB GR0 = -1.793 dB (6AA0h) A-law or linear and GR0 = -1.720 dB (3AA0h) µ-law to set D/A receive gain to 0dB
- BBABS ringing tests use the following conditions:
  - C1 programmed ringing 70.7 $V_{PK}$ (50 $V_{RMS}$), 0 $V_{DC}$ offset and 3 REN (2333 Ω + 24-µF) load
  - C2 programmed ringing 70.7 $V_{PK}$ (50 $V_{RMS}$), 0 $V_{DC}$ offset and 5 REN (1386 Ω + 40-µF) load

## 5.2 Supply Currents and Power Dissipation

- External Switcher circuit as shown in Figure 8.2.1 on page 59 with input voltage $V_{SW}$ = 12 $V_{DC}$
- Supply currents and power consumption are per channel of the device based on both channels in the same state
- Device or package power does not include power delivered to the load

| Operational State | Condition | $I_{DD}$ mA *(Note 2)* | $I_{VSW}$ mA *(Note 3)* | $I_{VBAT3}$ mA | $I_{VBAT1/2}$ mA | Device Power mW | System Power mW | Power | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Typ | Typ | Typ | Typ | Typ | Typ | | |
| Shutdown | Ch1/Ch2 | 1.5 | 0 | 0 | 0 | 5 | 5 | Per Channel | |
| Disconnect | Ch1/Ch2 | 5.5 | 0.7 | 0.1 | 0 | 25 | 26 | | |
| Low Power Idle Mode (LPIM) | Ch1/Ch2 | 9.5 | 1.6 | 0.3 | 0 | 47 | 51 | | |
| Idle | On-Hook | 14.5 | 5.3 | 0.8 | 0 | 99 | 112 | | |
| Active (normal or reverse polarity) | OHT | 23 | 11.9 | 1.9 | 0 | 190 | 219 | | |
| | Off-Hook, 300 Ω | 24 | 73.3 | 0.9 | 26 | 520 | 959 | | |
| LPIM/Ringing | Ch1 LPIM, Ch2 Ringing C1 | 33.5 | 275 | 31.3 | 0 | 1140 | 2319 | Both Channels | *1.* |
| | Ch1 LPIM, Ch2 Ringing C2 | 33.5 | 184 | 21 | 0 | 839 | 3406 | | |
| Active/Ringing | Ch1 Off-Hook, Ch2 Ringing C1 | 48 | 360 | 32 | 26 | 1793 | 3463 | | *1.* |
| | Ch1 Off-Hook, Ch2 Ringing C2 | 48 | 275 | 21.6 | 26 | 1523 | 4483 | | |

**Table 8 - Power Dissipation**

***Notes:***

1. *Not Tested in Production.*
2. *$I_{DD}$ supply current is the sum of $I_{AVDD}$, $I_{DVDD}$ and $I_{VDDHPI}$ for the device in normal mode divided by 2.*
3. *IVSW is not tested in production.*
4. *Ringing signal must be cadenced to produce an average power that can be handled by the package.*

## 5.3 DC Characteristics

| Symbol | Parameter Descriptions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Digital input low voltage VDDHPI = 3.3V | | | 0.8 | V | |
| $V_{IH}$ | Digital input high voltage VDDHPI = 3.3V | 2.0 | | | | |
| $V_{IL}$ | Digital input low voltage VDDHPI = 2.5V | | | 0.7 | | *2.* |
| $V_{IH}$ | Digital input high voltage VDDHPI = 2.5V | 1.7 | | | | *2.* |
| $V_{IL}$ | Digital input low voltage VDDHPI = 1.8V | | | 0.63 | | *2.* |
| $V_{IH}$ | Digital input high voltage VDDHPI = 1.8V | 1.17 | | | | *2.* |
| $I_{IL}$ | Digital input leakage current | –7 | | +7 | µA | |
| $I_{AIL}$ | Analog input leakage current | –1 | | +1 | | |
| $V_{HYS}$ | Digital input hysteresis | 0.16 | 0.25 | 0.34 | V | *1.* |
| $V_{OL}$ | Digital output low voltage<br>$I/O1_1$, $I/O1_2$ ($I_{OL}$ = 50 mA)<br>$I/O2_1$, $I/O2_2$ ($I_{OL}$ = 4 mA)<br>$I/O2_1$, $I/O2_2$ ($I_{OL}$ = 8 mA)<br>Other digital outputs ($I_{OL}$ = 2 mA) | | | 0.8<br>0.4<br>0.8<br>0.4 | V | *3.* |
| $V_{OH}$ | Digital output high voltage<br>$I/O2_1$, $I/O2_2$ ($I_{OH}$ = 4 mA)<br>$I/O2_1$, $I/O2_2$ ($I_{OH}$ = 8 mA)<br>Other digital outputs ($I_{OH}$ = 400 µA) | $V_{DVDD}$ – 0.4 V<br>$V_{DVDD}$ – 0.8 V<br>2.4 | | | | |
| $I_{OL}$ | Digital output leakage current (Hi-Z state)<br>0 < V < DVDD | –7 | | +7 | µA | |
| $V_{REF}$ | VREF output open circuit voltage ($I_{VREF}$ = +/- 100 µA) | 1.43 | 1.5 | 1.57 | V | |
| $C_{IREF}$ | IREF pin maximum load capacitance | | | 20 | pF | *1.* |
| $C_I$ | Digital input capacitance | | | 4 | | |
| $C_O$ | Digital output capacitance | | | 4 | | |
| $PSRR_1$ | AVDD, DVDD power supply rejection ratio<br>(1.02 kHz, 100 $mV_{RMS}$, either path, GX = GR = 0 dB) | 32 | 38 | | dB | |
| $PSRR_2$ | VBH, VBL power supply rejection ratio<br>(1.02 kHz, 100 $mV_{RMS}$, either path, GX = GR = 0 dB) | 40 | | | | *1.* |

***Notes:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production*
3. *$I/O1_i$, and $I/O2_i$ outputs are resistive for less than a 0.8 V drop. Total DC current must not exceed absolute maximum ratings.*

## 5.4 DC Feed and Signaling - All States Except Low Power Idle Mode

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| ILA programmable range, Active state | | 18 | | 45 | mA | *1.* |
| $I_L$, Loop current accuracy, Active state | $I_L$ in constant current region after ILA calibration | –10 | | +10 | % | |
| $I_{RINGD}$, RINGD leakage, Ring Open state | VBH = -81 V<br>$R_L$ = 0 to GND or VBH | | | 1000 | µA | *1.* |
| $I_{TIPD}$, TIPD leakage, Tip Open state | VBH = -81 V<br>$R_L$ = 0 to GND or VBH | | | 1000 | | |
| TIPD, RINGD leakage, Disconnect state | VBH = -81 V<br>$R_L$ = 0 to GND or to VBH + 2V | | | 10 | | |
| $I_{RINGD}$, RINGD current accuracy, Tip Open state | RINGD to ground | –10 | | +10 | % | *1.* |
| $V_{TIPD}$, ground start signaling | TIPD to –48 V = 7 kΩ,<br>RINGD to ground = 100 Ω | –7.5 | –5 | | V | |
| TDC, RDC input offset current | | 1.35 | 1.5 | 1.65 | µA | *1., 2.* |
| Ground key accuracy | After calibration | -1 mA - 15% | | +1 mA +15% | | |
| Switch hook accuracy | After calibration | –20 | | +20 | % | |
| Open circuit voltage, $V_{TIPD}$ - $V_{RINGD}$ | VOC = 48 V, after VOC calibration | –7 | | +7 | | |
| $V_{RINGD}$, open circuit | VOC = 48 V, after VOC calibration | –56.5 | | –49.0 | V | |

***Notes:***

*1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*

*2. Analog input pad leakage can add to this value - see specification under "DC Characteristics" on page 33.*

## 5.5 DC Feed and Signaling - Low Power Idle Mode State

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| $V_{TIPD}$ - $V_{RINGD}$ voltage | \|VBH\| > 52 V, $I_{LOAD}$ = 3 mA | 44 | | | V | *1.* |
| | $R_{LOAD}$ =3.5 KΩ | 23 | 28 | 33 | | |
| | VBH= -59 V, $R_{LOAD}$ = open | 44 | 50 | 56 | | |
| $I_{TIPD}$ current limit | TIPD sourcing current | 9 | 34 | 70 | mA | *1.* |
| $I_{RINGD}$ current limit | RINGD sinking current, $R_{LOAD}$ =600 Ω | 7.0 | 8.2 | 9.3 | | |
| Off-hook current settling time | $R_{LOAD}$ =200 Ω | | 150 | 800 | µs | *1.* |
| DC feed resistance | $I_{LOAD}$ < current limit | | 200 | | Ω | |
| | $I_{LOAD}$ > current limit | | 230K | | | |

***Note:***

*1. This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*

## 5.6 Metering

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Level accuracy | 0.5 $V_{RMS}$, 12 or 16 kHz,<br>200 or 3000 Ω AC load | –5 | | +10 | % | *1.* |
| Frequency accuracy | 12 or 16 kHz | –0.1 | | +0.1 | % | |

***Note:***

*1. This parameter is guaranteed by characterization or correlation to other tests. Typical values not tested in production.*

## 5.7 Ringing

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Ringing Voltage Accuracy | 52.5 $V_{PK}$ into a 5 REN load | –7 | | +7 | % | *1.* |
| Ringing DC offset, $V_{TIPD}$ - $V_{RINGD}$ | $R_L$ = open circuit, programmed rInging = 0 $V_{PK}$ | –2 | 0 | +2 | V | *3.* |
| Harmonic distortion | 52.5 $V_{PK}$ into a 5 REN load | | 3 | 5 | % | |
| Ringing current limit accuracy | $R_L$ = 600 Ω | –10 | | 10 | | |
| Ringing source impedance | | | 200 | | Ω | *2.* |
| DC ring trip accuracy | EGBIAS = 1 | –15 | | +15 | % | *2., 4.* |
| AC ring trip accuracy | EGBIAS = 0 | –15 | | +15 | | |
| Ring trip delay | Periods of ringing | 1 | | 3 | cycles | |

***Notes:***

1. *This production test is performed without calibration. After calibration, typical accuracy is within +/- 4 %*
2. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
3. *After calibration.*
4. *If the ringing current in the loop is near the current limit more than 50% of the time, a ring trip will occur regardless of the average current.*

## 5.8 Switching Regulator Controller

The following specifications apply to switching regulator controllers Y and Z.

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SWISx shutdown threshold | Referenced to GND | 85 | 100 | 115 | mV | |
| SWISx hysteresis | | | 25 | | | *1.* |
| SWISx input bias current | | –10 | | 10 | µA | |
| SWISx shutdown delay | $V_{SWISx}$ > 115 mV | 12 | | 88 | ns | *1., 2.* |
| SWCMPx output current | | –200 | | 200 | µA | *1.* |
| SWCMPx operating range | | 0.4 | | 2.6 | V | |
| SWVSx to SWCMPx gain | | 0.4 | | 40 | V/nA | |
| SWVSx to SWCMPx bandwidth | | 100 | | | kHz | |
| SWVSx input offset current | $R_{VSx}$ = 1.0 MΩ | 1.3 | 1.5 | 1.7 | µA | |
| LFC1 output impedance | | | 12 | | kΩ | |
| SWxV output voltage accuracy (VBL regulation) | Calibrated -30 V voltage | –33 | | –27 | V | *3.* |

***Notes:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Time from SWISx exceeding threshold to SWOUTx voltage passing through DVDD/2.*
3. *Accuracy following battery calibration depends on the battery voltage sense accuracy (+/-4 %) plus the calibration resolution of +/- 0.625 V*

## 5.9 Charge Pump Controller and MOSFET Driver

The following specifications apply to the charge pump controller when generating VDDSW and for driving the switching circuit MOSFETs.

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| VDDSW output voltage range | $I_{VDDSW}$ = 5 mA | 4.3 | 4.7 | 5.0 | V | *1.* |
| VDDSW step voltage | $I_{VDDSW}$ = 5 mA | | 0.1 | | | |
| VDDSW output voltage accuracy | VDDSW = 4.7 V, $I_{VDDSW}$ = 5 mA | –3 | | +3 | % | |
| VDDSW undervoltage lockout threshold | Below the target output voltage | 110 | 200 | 290 | mV | |
| SWOUTx peak source current | $V_{SWOUTx}$ = 2.5 V, $C_{LOAD}$ = 1.5 nF | 100 | | | mA | *1.* |
| SWOUTx peak sink current | $V_{SWOUTx}$ = 2.5 V, $C_{LOAD}$ = 1.5 nF | 200 | | | | |
| Maximum total gate switching charge (for switcher Y drive) | VDDSW = 4.7 V, F = 512 kHz, VDDSW internally generated, only one switcher used | 12 | | | nC | *1.* |

***Notes:***

*1. This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*

## 5.10 Voice ADC Signal Sense Accuracy

| Description | Code | Full Scale | Useful Range | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Metallic AC coupled voltage (Tip/Ring voice) | 00h | –3.44 to +3.44 | –3.44 to +3.44 | –4% | | +4% | V | *1., 2.* |
| Voice DAC analog loopback | 0Ah | –2.0 to +2.0 | –1.0 to +1.0 | –12% | | +12% | | |

***Notes:***

*1. All specifications assume calibration.*

*2. The % limits are defined as the % of programmed threshold value or the % of the actual voltage or current on Tip / Ring. The offset and percentage errors are independent and combine as RMS errors.*

## 5.11 Supervision ADC Signal Sense Accuracy

| Description | Code | Full Scale | Useful Range | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| $VBAT_1$ sense at SWVSY | 01h | –240 to +240 | –180 to 0 | –0.5 V – 4 % | | +0.5 V +4 % | V | 1., 2., 3., 6. |
| $VBAT_2$ sense at SWVSZ | 02h | | | –0.5 V – 4 % | | +0.5 V +4 % | | |
| $VBAT_3$ sense at VS1, VS2 | 03h | | –180 to +60 | –0.5 V – 4 % | | +0.5 V +4 % | | |
| Tip voltage to ground | 04h | | –225 to +225 | –0.5 V – 4 % | | +0.5 V +4 % | | |
| Ring voltage to ground | 05h | | | –0.5 V – 4 % | | +0.5 V +4 % | | |
| Metallic DC line voltage (Tip to Ring) | 06h | | –160 to +160 | –0.5 V – 5 % | | +0.5 V +5 % | | |
| Longitudinal DC line voltage (Tip to ground + Ring to ground) | 0Ah | | | –1.0 V – 5 % | | +1.0 V +5 % | | 1., 2., 6. |
| MOSFET drive supply, VDDSW | 10h | +2 to +10 | +2.5 to +5.5 | –0.08 V – 0.5 % | | +0.08 V +0.5 % | | |
| Metallic loop current, IM (Tip to Ring) in Normal Mode | 07h | –59.5 to +59.5[4] | –51 to +51[4] | –1.0 mA – 5 % | | +1.0 mA +5% | mA | |
| Longitudinal loop current, IL (total) in Normal Mode | 08h | –59.5 to +59.5 | –42 to +42 | –1.0 mA – 5 % | | +1.0 mA +5% | | |
| Ring current, IB (IM+IL) | 0Eh | | | –2.0 mA – 5 % | | +2.0 mA +5% | | |
| Tip current, IA (IM-IL) | 0Fh | | | –2.0 mA – 5 % | | +2.0 mA +5% | | |
| Metallic loop current (IM) in Low Gain Mode | 08h | –297.5 to +297.5 | –100 to +100 | –5.0 µA – 5 % | | +5.0 µA +5% | µA | |
| Longitudinal loop current per wire (IL) in Low Gain Mode | 07h | | –250 to +250 | –5.0 µA– 5 % | | +5.0 µA +5% | | |
| Tip voltage to Longitudinal current ratio | N/A | N/A | N/A | –6.5 | | +6.5 | % | 1., 5., 6., 7. |
| Ring voltage to Longitudinal current ratio | | | | –6.5 | | +6.5 | | |
| Metallic voltage to Metallic current ratio | | | | –6.5 | | +6.5 | | |
| Temperature sense | 0Dh | –50 to +150 | –50 to +150 | –15 | | +15 | °C | 1., 6. |

***Notes:***

1. *All specifications assume calibration.*
2. *The % limits are defined as the % of programmed threshold value or the % of the actual voltage or current. The offset and percentage errors are independent and combine as RMS errors.*
3. *This is measured in production by calibrating offset voltage and applying -26 V for voltage to ground and 20 V Metallic. Accurately measuring smaller voltage requires care in offset calibration.*
4. *The Metallic loop current scale and range during ringing are –119 mA to +119 mA.*
5. *These are ratios of voltage to current measurements in Low Gain state performed during production testing.*
6. *Full scale is defined as a digital output code of ± 32768.*
7. *Not tested in production.*

## 5.12 Transmission Characteristics - Narrowband Codec Mode

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TAC - RAC overload level | Active state, GX = AX = 0 dB | 3.4 | | | $V_{PK}$ | *1., 2.* |
| Transmit level, A/D | 0 dBm, GX = GX0, 1014 Hz | | 0 | | dBm0 | |
| Receive level, D/A | 0 dBm0, GR = GR0, 1014 Hz | | 0 | | dBm | |
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz, off-hook | –0.35 | | +0.35 | dB | |
| Gain accuracy, D/A or A/D | 0 dBm0, 1014 Hz, on-hook | –0.5 | | +0.5 | | |
| Idle channel noise<br>$V_{TIPD}$ - $V_{RINGD}$<br><br>DXA, digital out | <br>DRA, digital input = 0, A-law, 0 dBr<br>DRA, digital input = 0, µ-law, 0 dBr<br>$V_{TIPD}$ - $V_{RINGD}$ = 0 $V_{AC}$, A-law, 0 dBr<br>$V_{TIPD}$ - $V_{RINGD}$ = 0 $V_{AC}$, µ-law, 0 dBr | | | <br>–74<br>16<br>–65<br>19 | <br>dBm0p<br>dBrnC0<br>dBm0p<br>dBrnC0 | *5.* |
| Two wire return loss | 200 to 3400 Hz | 26 | 30 | | dB | |
| Longitudinal to metallic balance<br>TIPD - RINGD or DXA | 200 to 3400 Hz | 50 | | | | *7.* |
| DRA to longitudinal signal generation | 300 to 3400 Hz | 42 | | | | *7.* |
| Longitudinal current capability, per wire<br>TIPD or RINGD | Active state | 8.5 | | | $mA_{RMS}$ | *1.* |
| Longitudinal impedance at TIPD or RINGD | 0 to 100 Hz, LI = 0 | | 100 | | Ω/pin | |
| Crosstalk between channels<br>TX or RX to TX<br>RX or TX to RX | <br>0 dBm0, 1014Hz, Average<br>0 dBm0, 1014Hz, Average | | | <br>–76<br>–78 | dBm0 | |
| Attenuation distortion | 300 to 3000 Hz | –0.125 | | +0.125 | dB | *1., 3.* |
| Single frequency distortion | A-law or µ-law, off-hook | | | –46 | | *4.* |
| Second harmonic distortion, D/A | GR = 0 dB, linear mode, off-hook | | | –55 | | |
| End to end absolute group delay | B = Z = 0; X = R = 1, C/L = 0 | | | 678 | µs | *1., 6.* |
| *PESQ-LQ* voice quality score | Linear, A-law, or µ-law | | 4.30 | | | *1.* |

***Notes:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *See Figure 18, "Transmit (A to D) Path Attenuation vs. Frequency" on page 39 and Figure 19, "Receive (D to A) Path Attenuation vs. Frequency" on page 39.*
4. *0 dBm0 input signal, 300 to 3400 Hz measurement at any other frequency, 300 Hz to 3400 Hz.*
5. *No single frequency component in the range above 3800 Hz may exceed a level of –55 dBm0.*
6. *The End to End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
7. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

### 5.13 Attenuation Distortion - Narrowband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 18 and Figure 19. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

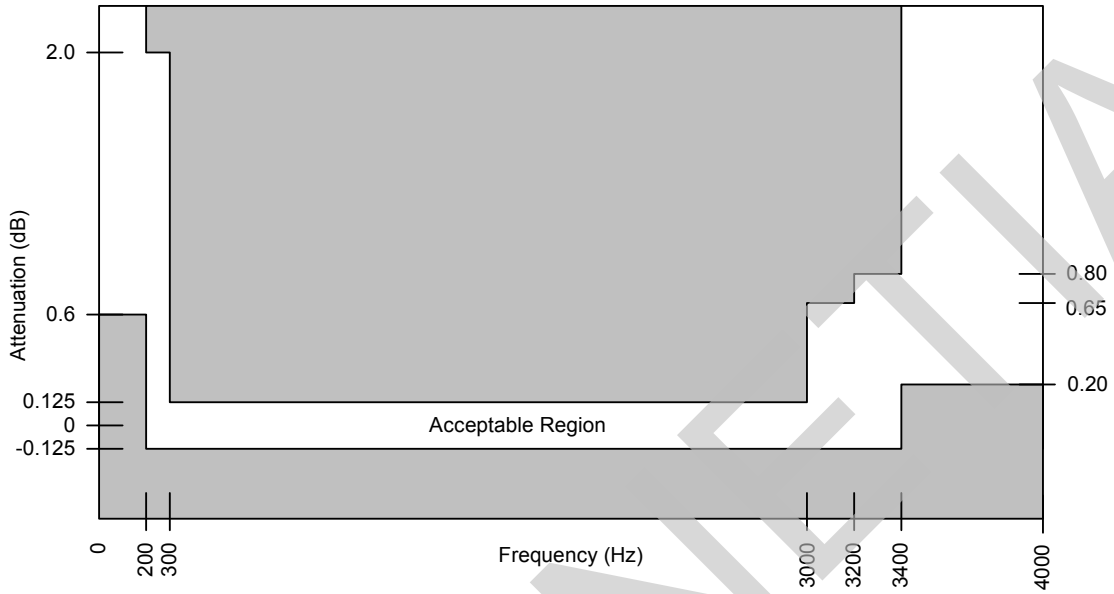



**Figure 18 - Transmit (A to D) Path Attenuation vs. Frequency**

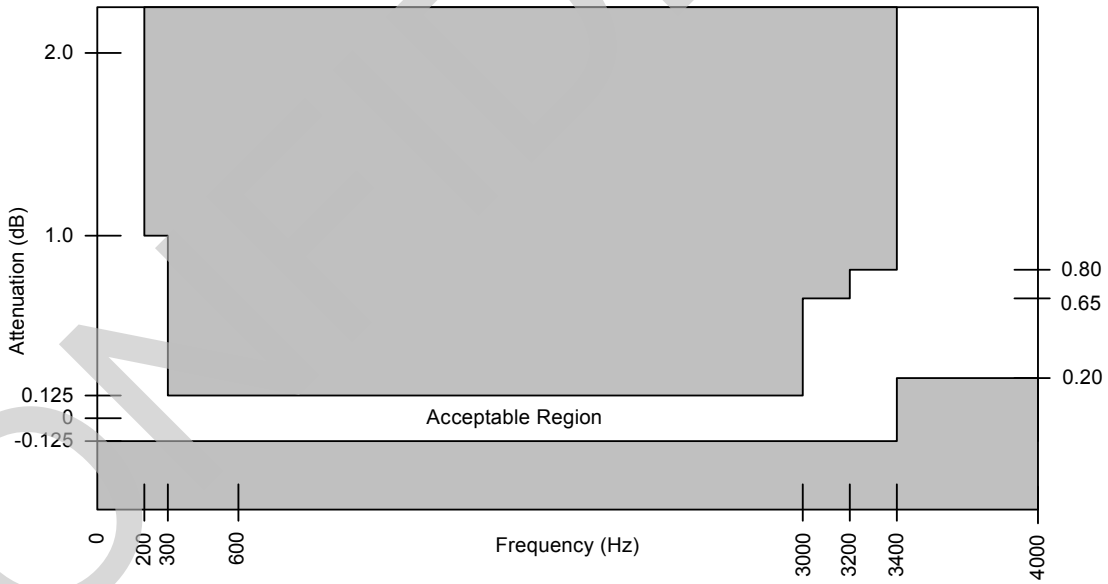



**Figure 19 - Receive (D to A) Path Attenuation vs. Frequency**

### 5.14 Discrimination Against Out-of-Band Input Signals - Narrowband Codec Mode

When an out-of-band sine wave signal of frequency f, and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The minimum specifications are

shown in Table 9. The attenuation of the waveform below amplitude A, between 3400 Hz and 4600 Hz, is given by the formula:

$$\text{Attenuation} = \left[14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

.

| Frequency of Out-of-Band Signal | Amplitude of Out-of-Band Signal | Level below A |
|---|---|---|
| 16.6 Hz < f < 45 Hz | –25 dBm0 < A ≤ 0 dBm0 | 18 dB |
| 45 Hz < f < 65 Hz | –25 dBm0 < A ≤ 0 dBm0 | 25 dB |
| 65 Hz < f < 100 Hz | –25 dBm0 < A ≤ 0 dBm0 | 10 dB |
| 3400 Hz < f < 4600 Hz | –25 dBm0 < A ≤ 0 dBm0 | see Figure 20 |
| 4600 Hz < f < 100 kHz | –25 dBm0 < A ≤ 0 dBm0 | 32 dB |

**Table 9 - Out of Band Discrimination, Narrowband Codec Mode**

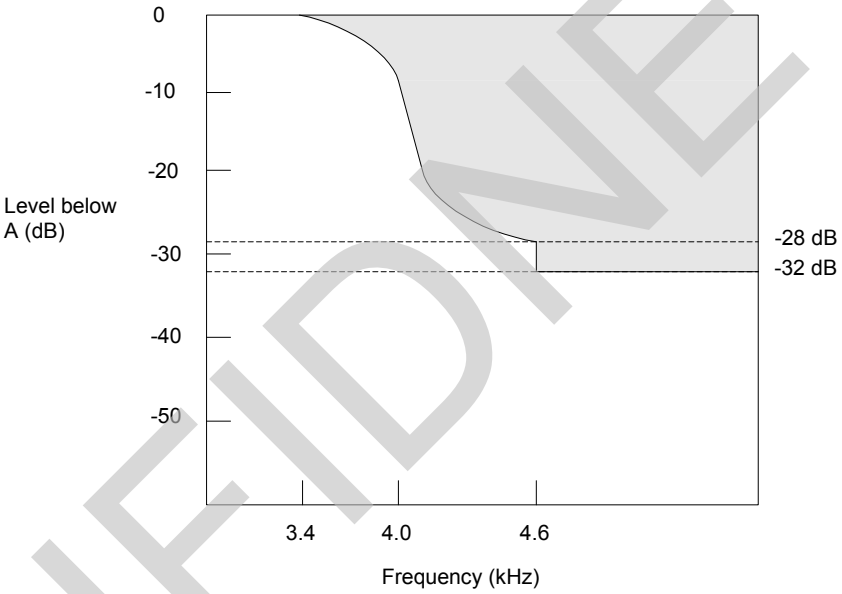



**Figure 20 - Discrimination Against Out of Band Signals**

## 5.15 Discrimination Against 12kHz and 16kHz Metering Signals - Narrowband Codec Mode

If the Le9622 device is used in a metering application where 12kHz or 16kHz tone bursts are injected onto the telephone line toward the subscriber, a portion of these tones may also appear at the transmit input. These out-of-band signals may cause frequency components to appear below 4 kHz at the digital output. For a 12kHz or 16kHz tone, the frequency components below 4 kHz are reduced from the input by at least 70 dB. The sum of the peak metering and signal voltages must be within the TAC - RAC pin overload level.

## 5.16 Spurious Out-of-Band Signals at the Analog Output - Narrowband Codec Mode

With PCM idle code being applied to the digital input and either a quiet 600 Ω termination or an open being applied to Tip and Ring, any single frequency tone between 0 and 16kHz measured at the analog output shall be less than -50 dBm0. With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of

0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output is less than the limits shown below.

| Frequency | Level |
|---|---|
| 4.6 kHz to 40 kHz | –32 dBm0 |
| 40 kHz to 240 kHz | –46 dBm0 |
| 240 kHz to 1 MHz | –36 dBm0 |

With code words representing any sine wave signal in the range 3.4 kHz to 4.0 kHz at a level of 0 dBm0 applied to the digital input, the level of the signals at the analog output are below the limits in Figure 21. The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:

$$\text{Level} = \left[-14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

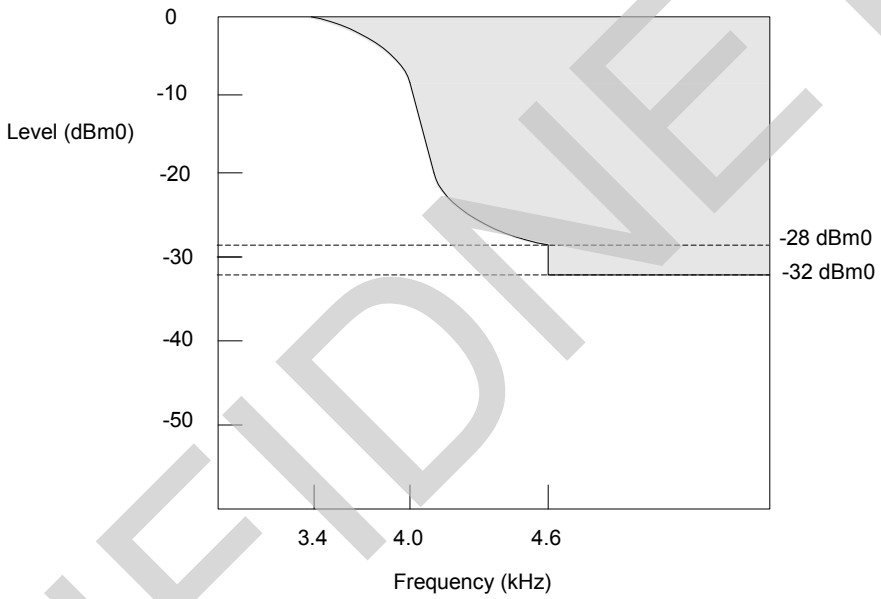



**Figure 21 - Spurious Out of Band Signals**

## 5.17 Overload Compression - Narrowband Codec Mode

Figure 22 on page 42 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

1. 1.2 dB < GX ≤ + 12 dB
2. –12 dB ≤ GR < –1.2 dB
3. Digital voice output of one VoicePort channel connected to digital voice input of a second VoicePort channel.
4. Measurement analog to analog

.

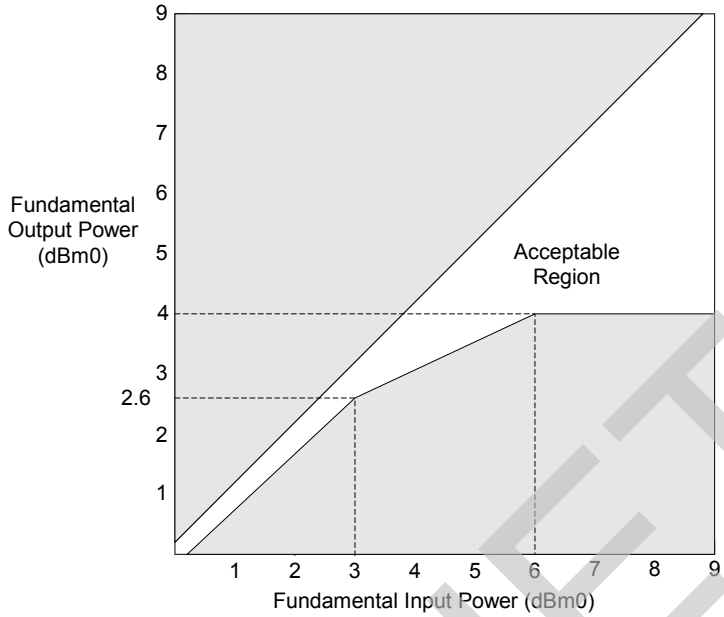



**Figure 22 - Analog to Analog Overload Compression**

## 5.18 Gain Linearity - Narrowband Codec Mode

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 23 (A-law) and Figure 24 (μ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

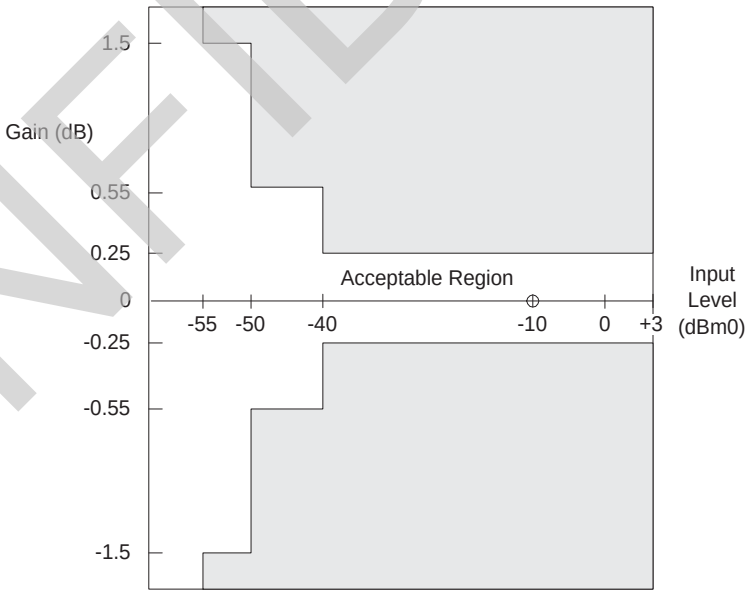



**Figure 23 - A-law Gain Linearity with Tone Input (Both Paths)**

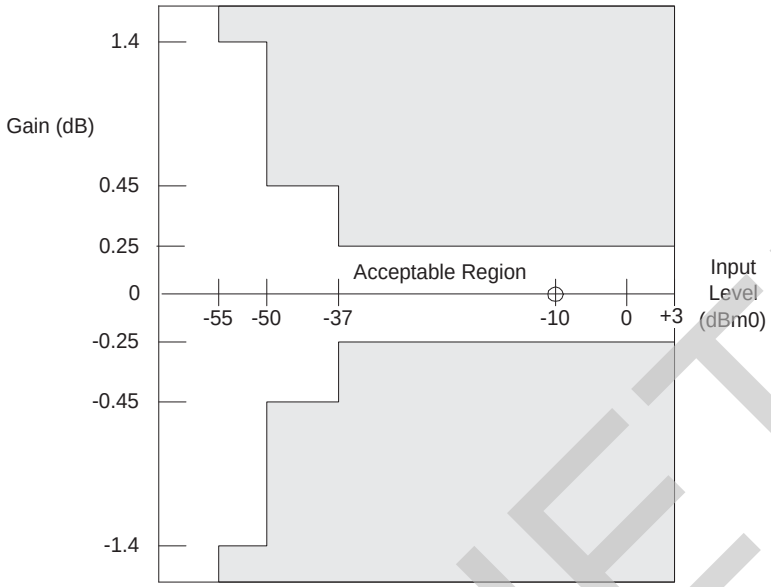



**Figure 24 - µ-law Gain Linearity with Tone Input (Both Paths)**

## 5.19 Total Distortion Including Quantizing Distortion - Narrowband Codec Mode

The signal to total distortion ratio will exceed the limits shown in Figure 25 for either path when the input signal is a sine wave with a frequency of 1014 Hz, using psophometric weighting for A-law and C-message weighting for µ-law

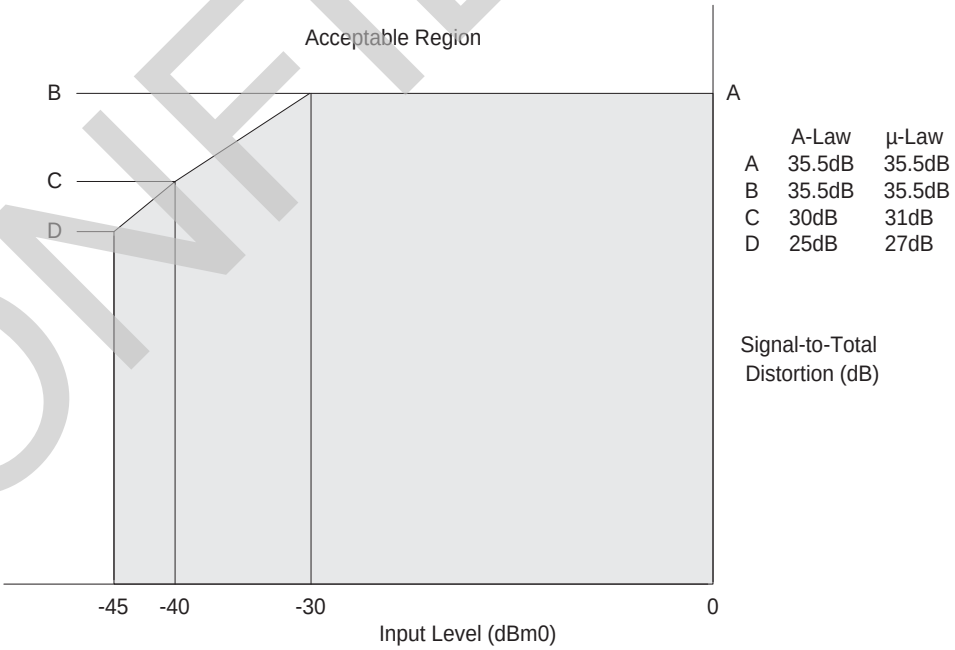



**Figure 25 - Total Distortion with Tone Input (Both Paths)**

### 5.20 Group Delay Distortion - Narrowband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in Figure 26. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

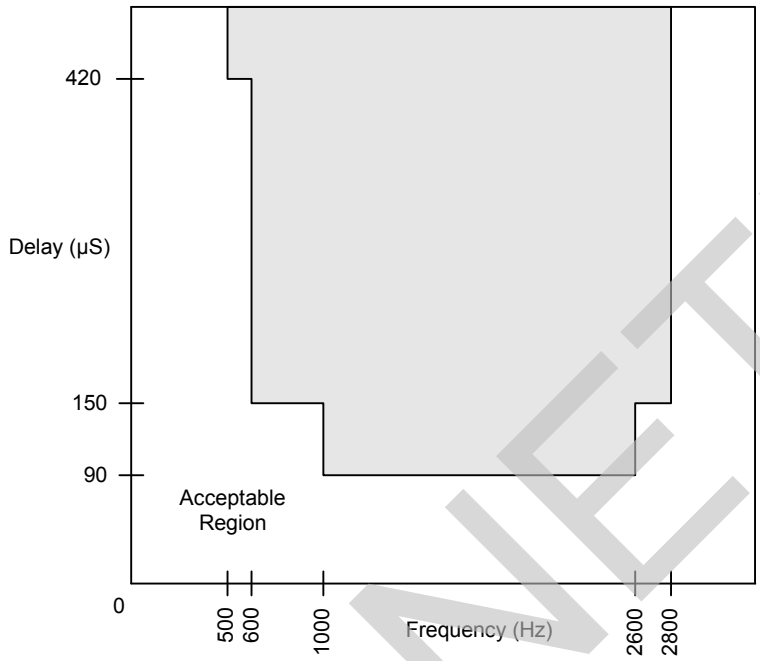



**Figure 26 - Group Delay Distortion**

## 5.21 Transmission Characteristics - Wideband Codec Mode

| Description | Test Conditions | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| TAC - RAC overload level | Active state GX = AX = 0 dB | 3.4 | | | $V_{PK}$ | *1., 2.* |
| Transmit level, A/D | 0 dBm, GX = GX0, 1014 Hz | | 0 | | dBm0 | |
| Receive level, D/A | 0 dBm0, GR = GR0, 1014 Hz | | 0 | | dBm | |
| Gain accuracy, D/A or A/D | 0 dBm0,1014 Hz, Off-hook | –0.5 | | +0.5 | dB | |
| Gain accuracy, D/A or A/D | 0 dBm0,1014 Hz, On-hook | –0.5 | | +0.5 | | *1.* |
| Attenuation distortion | 100 Hz to 6.0 kHz | –0.25 | | +0.25 | | *3.* |
| Single frequency distortion | 0dBm0, Linear Mode,<br>50 Hz to 7.0 kHz, off-hook | | | –50 | | *4.* |
| Signal to noise + distortion | 0dBm0, Linear Mode, 50 Hz to 7.0 kHz | 50 | | | | *4.* |
| Second harmonic distortion, D/A | GR = 0 dB, off-hook | | | –55 | | |
| Idle channel noise,<br>$V_{TIPD}$ - $V_{RINGD}$<br>DXA, digital out | <br>DRA, digital input = 0, linear, 0 dBr<br>$V_{TIPD}$ - $V_{RINGD}$ = 0 $V_{AC}$, linear, 0 dBr | | | <br>–67<br>–67 | <br>dBm0p<br>dBm0p | *1., 5.* |
| End to end absolute group delay | B = Z = 0; X = R = 1, C/L = 0 | | | 340 | µs | *1., 6.* |
| Two wire return loss | 50 to 7000 Hz | 20 | 26 | | dB | *1.* |
| Longitudinal to metallic balance TIPD - RINGD or DXA | 50 to 7000 Hz | 48 | | | dB | *7.* |
| DRA to longitudinal signal generation | 300 to 7000 Hz | 40 | | | | *1.* |
| Longitudinal current capability, per wire TIPD or RINGD | Active state | 8.5 | | | $mA_{RMS}$ | *1.* |
| Longitudinal impedance at TIPD or RINGD | 0 to 100 Hz, LI = 0 | | 100 | | Ω/pin | *1.* |
| *PESQ-LQ* voice quality score | Linear | | 4.30 | | | *1.* |

***Notes:***

1. *This parameter is guaranteed by characterization or correlation to other tests. Not tested in production.*
2. *Overload level is defined when THD = 1%.*
3. *See Figure 27, "Transmit (A to D) Path Attenuation vs. Frequency- (with High Pass Filter Enabled)" on page 46 and Figure 28, "Receive (D to A) Path Attenuation vs. Frequency" on page 46.*
4. *0 dBm0 input signal, 50 to 7000 Hz measurement at any other frequency, 50 to 7000 Hz.*
5. *No single frequency component in the range above 7600 Hz may exceed a level of –55 dBm0.*
6. *The End to End Group Delay is the absolute group delay of the echo path with the B filter turned off.*
7. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*

## 5.22 Attenuation Distortion - Wideband Codec Mode

The signal attenuation in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 27 and Figure 28. The reference frequency is 1014 Hz and the signal level is –10 dBm0.

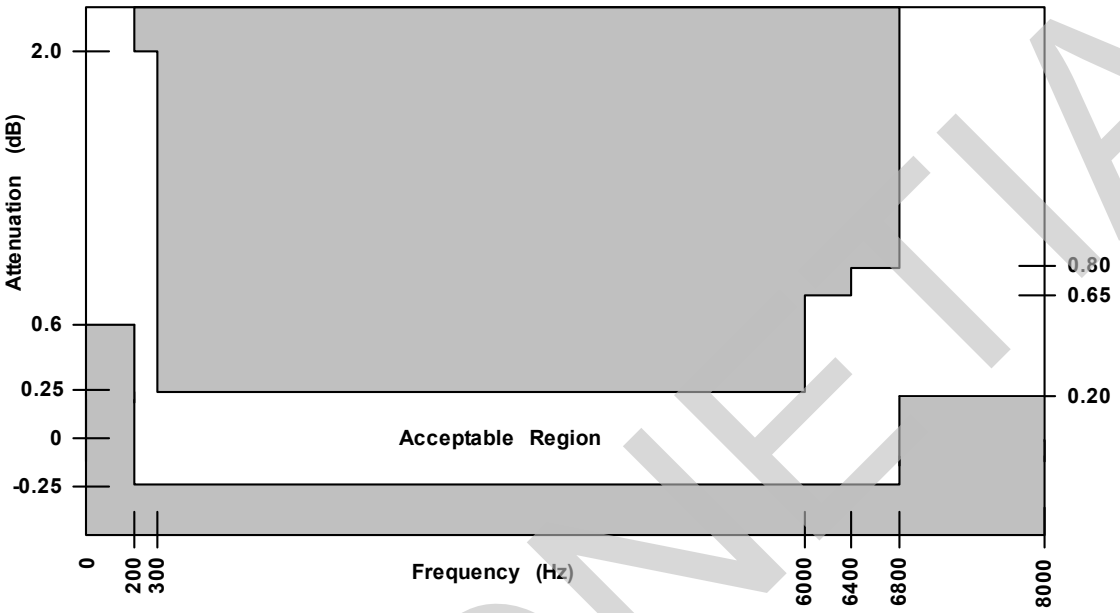



**Figure 27 - Transmit (A to D) Path Attenuation vs. Frequency- (with High Pass Filter Enabled)**

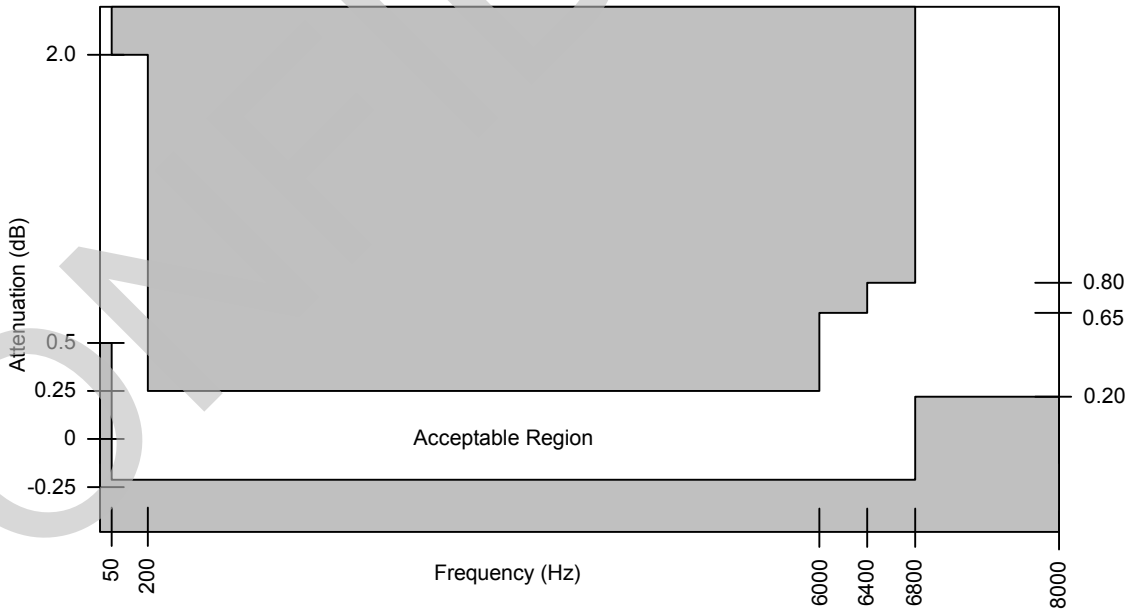



**Figure 28 - Receive (D to A) Path Attenuation vs. Frequency**

### 5.23 Group Delay Distortion - Wideband Codec Mode

For either transmission path, the group delay distortion is within the limits shown in Figure 29. The minimum value of the group delay is taken as the reference. The signal level should be 0 dBm0.

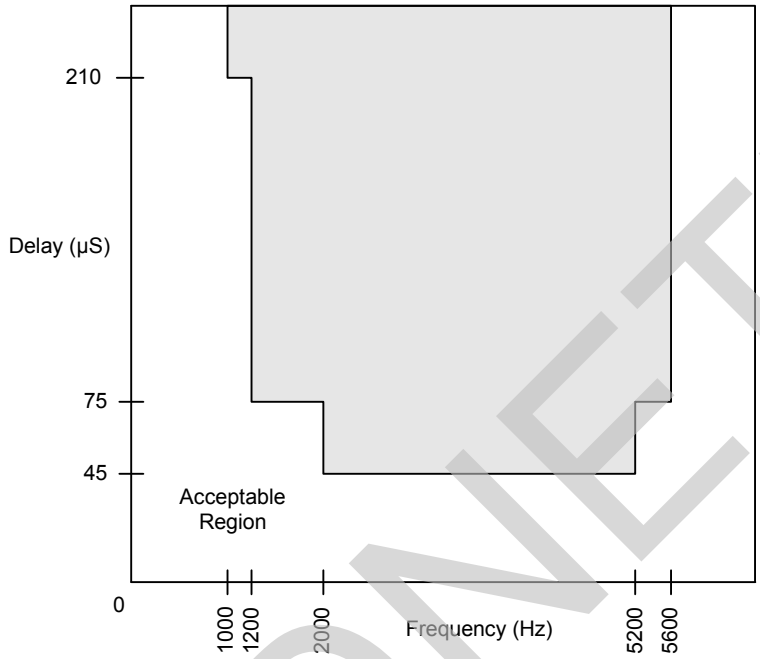



**Figure 29 - Group Delay Distortion**

## 6.0 Switching Characteristics and Waveforms

The following are the switching characteristics over operating range, unless otherwise noted. Minimum and maximum values are valid for all digital outputs with a 115 pF load.

### 6.1 PCM and SPI Mode

The PCM and SPI mode is used to communicate audio and control information to the host processor. Unless otherwise specified, the SPI timing values are valid for VDDHPI = 1.8 $V_{DC}$, 2.5 $V_{DC}$, or 3.3 $V_{DC}$.

#### 6.1.1 SPI Interface

| No. | Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | $t_{DCY}$ | Data clock period | 122 | | | ns | |
| 2 | $t_{DCH}$ | Data clock high pulse width | 48 | | | | |
| 3 | $t_{DCL}$ | Data clock low pulse width | 48 | | | | |
| 4 | $t_{DCR}$ | Rise time of clock | | | 8 | | |
| 5 | $t_{DCF}$ | Fall time of clock | | | 8 | | |
| 6 | $t_{ICSS}$ | Chip select setup time, Input mode | 5 | | | | |
| 7 | $t_{ICSH}$ | Chip select hold time, Input mode | 0 | | | | |
| 8 | $t_{ICSL}$ | Chip select pulse width, Input mode | | $8t_{DCY}$ | | | |
| 9 | $t_{ICSO}$ | Chip select off time, Input mode | 0 | | | | |
| 10 | $t_{IDS}$ | Input data setup time | 5 | | | | |
| 11 | $t_{IDH}$ | Input data hold time | 0 | | | | |
| 12 | $t_{OLH}$ | I/O1, I/O2 output latch valid | | | 2500 | | |
| 13 | $t_{OCSS}$ | Chip select setup time, Output mode | 5 | | | | |
| 14 | $t_{OCSH}$ | Chip select hold time, Output mode | 0 | | | | |
| 15 | $t_{OCSL}$ | Chip select pulse width, Output mode | | $8t_{DCY}$ | | | |
| 16 | $t_{OCSO}$ | Chip select off time, Output mode | 0 | | | | *z* |
| 17 | $t_{ODD}$ | Output data turn on delay | | | 16 | | *1., 2.* |
| 18 | $t_{ODH}$ | Output data hold time | 2 | | | | *3.* |
| 19 | $t_{ODOF}$ | Output data turn off delay | 0 | | 10 | | |
| 20 | $t_{ODC}$ | Output data valid | | | 16 | | *1.* |
| – | $t_{RST}$ | Reset pulse width | 5 | | | µs | |

***Notes:***

1. *Values shown for VDDHPI = 3.3 V. Maximum $t_{ODD}$ and $t_{ODC}$ is 25 ns at 1.8 V and 18 ns at 2.5 V.*
2. *The first data bit is enabled on the falling edge of $\overline{CS}$ or the falling edge of DCLK, whichever occurs last.*
3. *This parameter is guaranteed by characterization or correlation to other tests. It is not tested in production.*

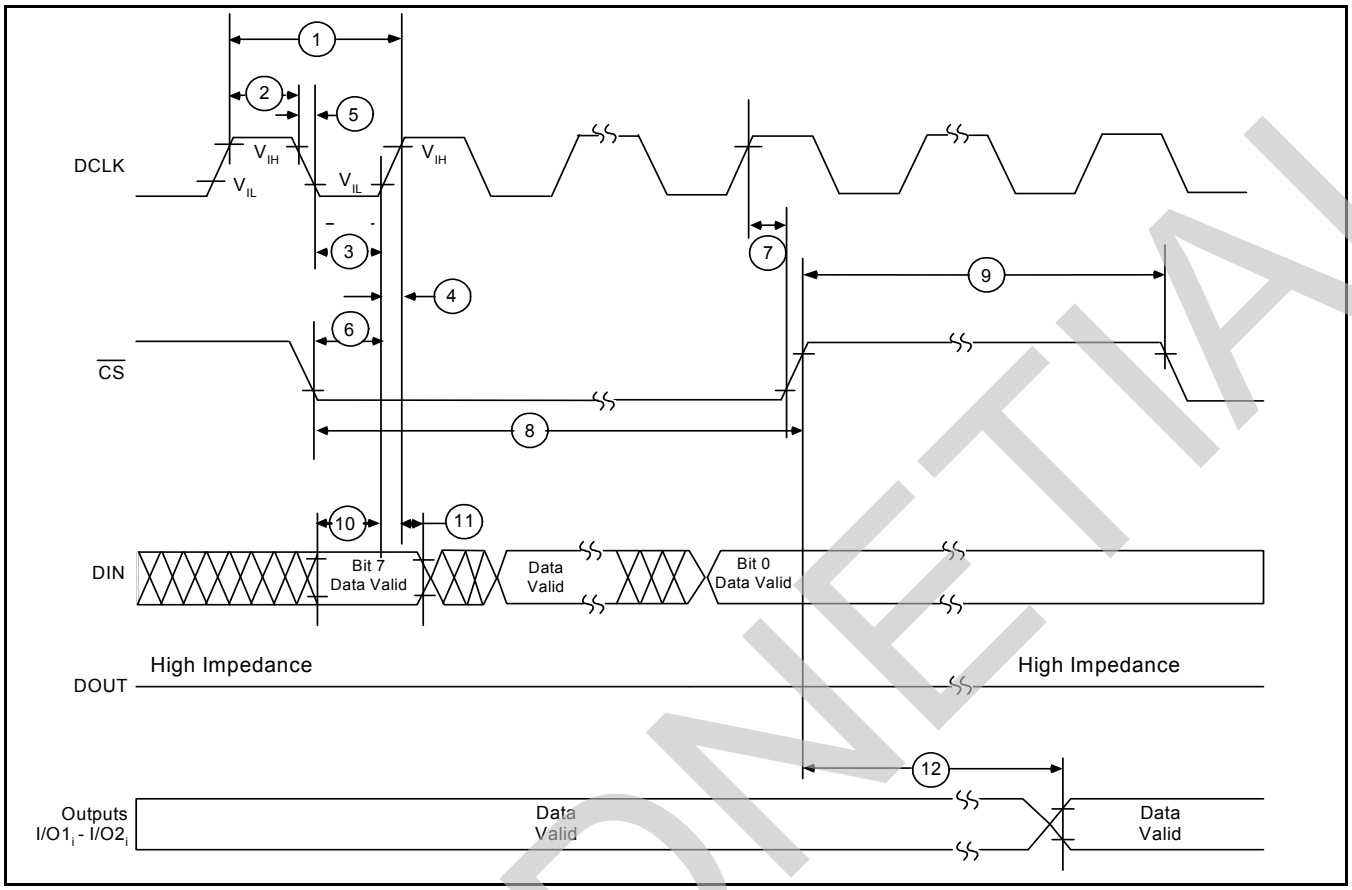



**Figure 30 - SPI Interface (Input Mode)**

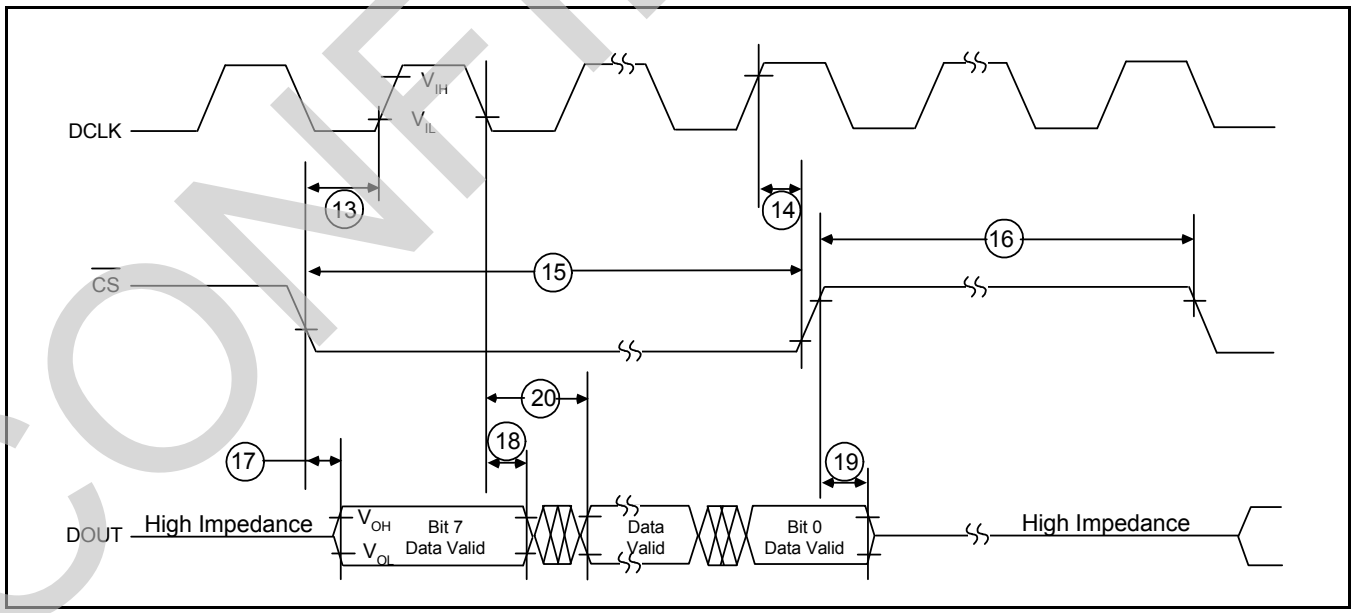



**Figure 31 - SPI Interface (Output Mode)**

### 6.1.2 PCM Interface

PCLK shall not exceed 8.192 MHz. Unless otherwise specified, the PCM timing values are valid for VDDHPI = 1.8 $V_{DC}$, 2.5 $V_{DC}$, or 3.3 $V_{DC}$. See Figure 32 through Figure 34 on page 52 for the PCM interface timing diagrams.

| No. | Symbol | Parameter | Min. | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 21 | $t_{PCY}$ | PCM Clock (PCLK) period | 122 | | 977 | ns | *1.* |
| 22 | $t_{PCH}$ | PCLK high pulse width | 48 | | | | |
| 23 | $t_{PCL}$ | PCLK low pulse width | 48 | | | | |
| 24 | $t_{PCR}$ | PCLK rise time | | | 8 | | |
| 25 | $t_{PCF}$ | PCLK fall time | | | 8 | | |
| 26 | $t_{FSS}$ | FS setup time | 5 | | $t_{PCY}$–30 | | |
| 27 | $t_{FSH}$ | FS hold time | 0 | | | | *2.* |
| – | $t_{FST}$ | Allowed PCLK or FS jitter time | –25 | | 25 | | *1.* |
| 30 | $t_{DXD}$ | PCM data output delay | | | 16 | | *3.* |
| 31 | $t_{DXH}$ | PCM data output hold time | 2 | | | | |
| 32 | $t_{DXZ}$ | PCM data output delay to high Z | 0 | | 10 | | |
| 33 | $t_{DRS}$ | PCM data input setup time | 5 | | | | |
| 34 | $t_{DRH}$ | PCM data input hold time | 0 | | | | *2.* |
| – | $t_{FSL}$ | FS low pulse width | 1.5 $t_{PCY}$ | | | | *5.* |

***Notes:***

1. *The PCLK frequency must be an integer multiple of the Frame Sync (FS) frequency. Frame Sync is expected to be an accurate 8 kHz pulse train. The actual PCLK rate depends on the CSEL bit setting in the Chip Configuration register. The minimum frequency is 1.024 MHz and the maximum frequency is 8.192 MHz. If PCLK has jitter, care must be taken to ensure that all setup, hold, and pulse width requirements are met.*
2. *Values shown for VDDHPI = 3.3 V. Minimum $t_{FSH}$ and $t_{DRH}$ is 0.3 ns at 1.8 V and 0.2 ns at 2.5 V.*
3. *Values shown for VDDHPI = 3.3 V. Maximum $t_{TSD}$ and $t_{DXD}$ is 25 ns at 1.8 V and 18 ns at 2.5 V.*
4. *$t_{TSO}$ is defined as the time at which the output achieves the Open Circuit state.*
5. *Applies only when FS is active low.*

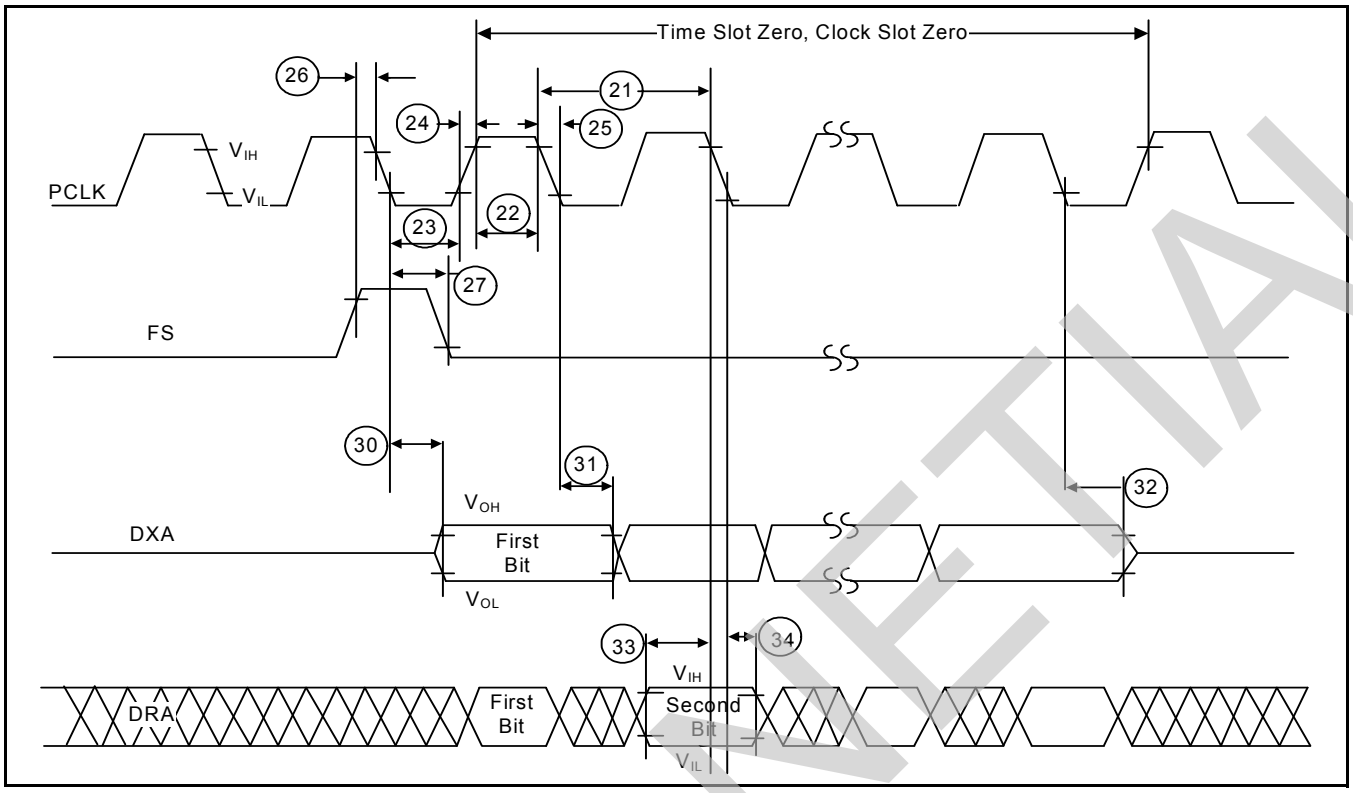



**Figure 32 - PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)**

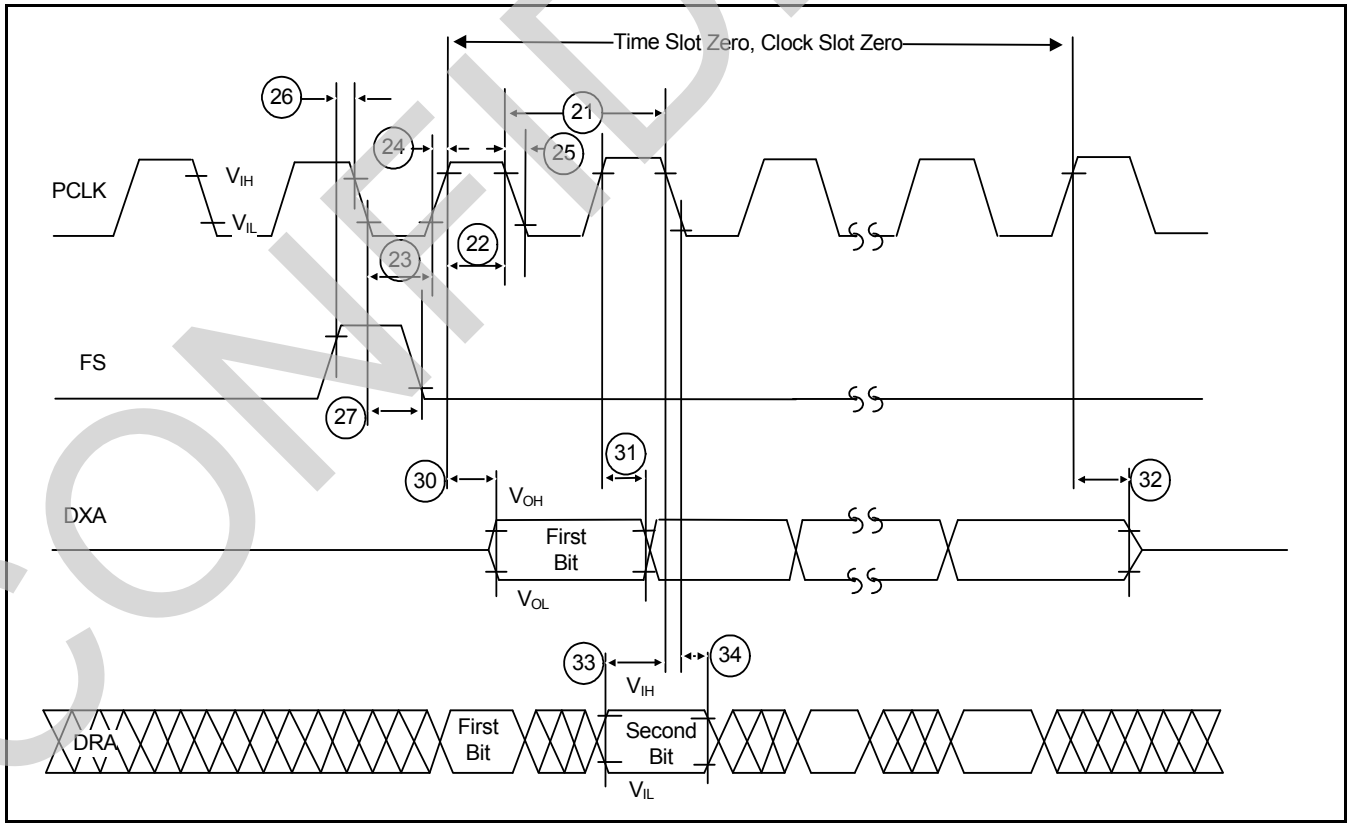



**Figure 33 - PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)**

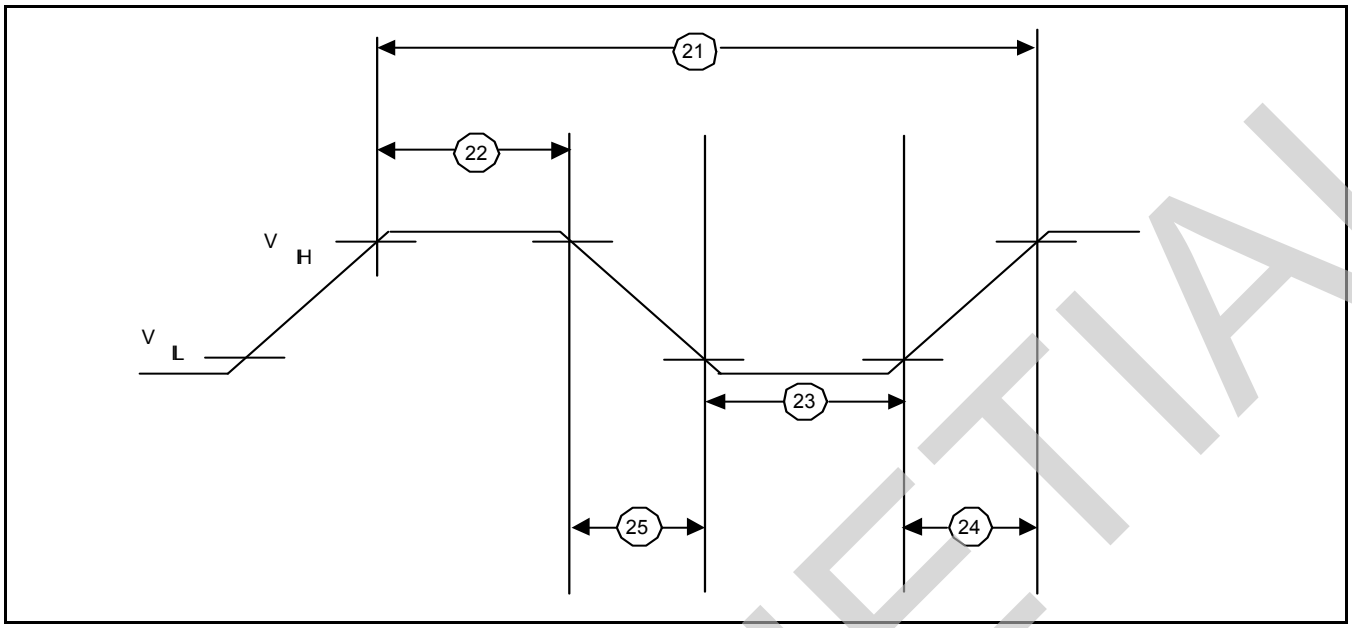



**Figure 34 - PCM Clock Timing**

## 6.2 Switcher Output Timing

(See Figure 35 for the SWOUTY, SWOUTZ timing diagram)

| No. | Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Tfall | Output fall time | | 15 | | ns | *1.* |
| 2 | Trise | Output rise time | | 30 | | | |
| 3LP | TPeriod | Period for Low Power mode | | 20.833 | | µs | *2., 5.* |
| 4LP | Tmax | Max on-time for Low Power mode | | 1.017 | | | |
| 3MP | TPeriod | Period for Medium Power mode | | 1.953 | | | *3., 5.* |
| 4MP | Tmax | Max on-time for Medium Power mode | | 1.017 | | | |
| 3HP | TPeriod | Period for High Power mode | | 1.953 | | | *4., 5.* |
| 4HP | Tmax | Max on-time for High Power mode | | 1.017 | | | |
| – | Duty Cycle LP | Duty cycle Low Power mode | 0 | 2.5 | | % | *2., 5.* |
| – | Duty Cycle MP | Duty cycle Medium Power mode | 0 | 52 | | | *3., 5.* |
| – | Duty Cycle HP | Duty cycle High Power mode | 0 | 52 | | | *4., 5.* |
| 5 | Y to Z offset | Delay from SWOUTZ to SWOUTY on | | 1.302 | | µs | |
| – | | SWISY leading edge blanking period | | 120 | | ns | *6.* |

***Notes:***

1. *Measured with a 1.5 nF load between SWOUTx and ground.*
2. *Register E6/E7h Write/Read Switching Regulator Control is loaded with low power mode 01h.*
3. *Register E6/E7h Write/Read Switching Regulator Control is loaded with medium power mode 02h.*
4. *Register E6/E7h Write/Read Switching Regulator Control is loaded with high power mode 03h.*
5. *Timing values assume SWFS[1:0] = 00b in E4/E5h Write/Read Switching Regulator Parameters. Stated periods and on times scale inversely with frequency selected.*
6. *This is a programmable setting with the default value shown here.*

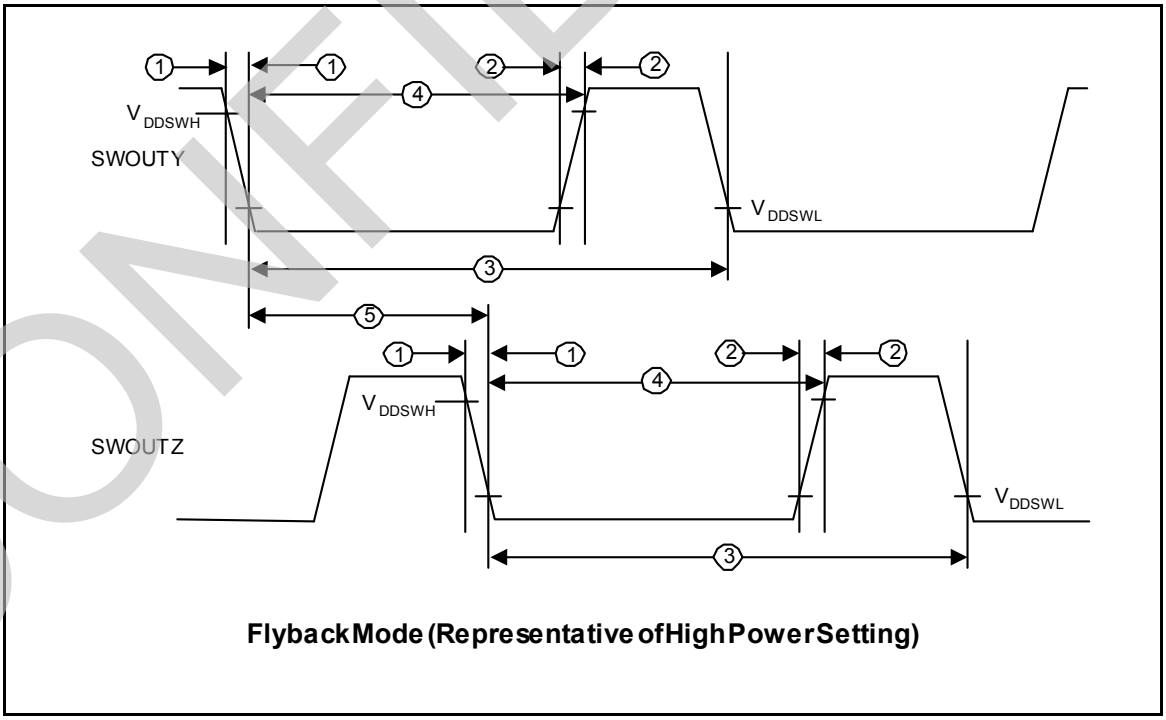



**Figure 35 - Switcher Output Waveform SWOUTY, SWOUTZ**

## 7.0 Device Pinout

The pins of the Le9622 device are listed and described in this section. Note that there are no ground pins. All ground connections inside this device are made through the exposed pad.

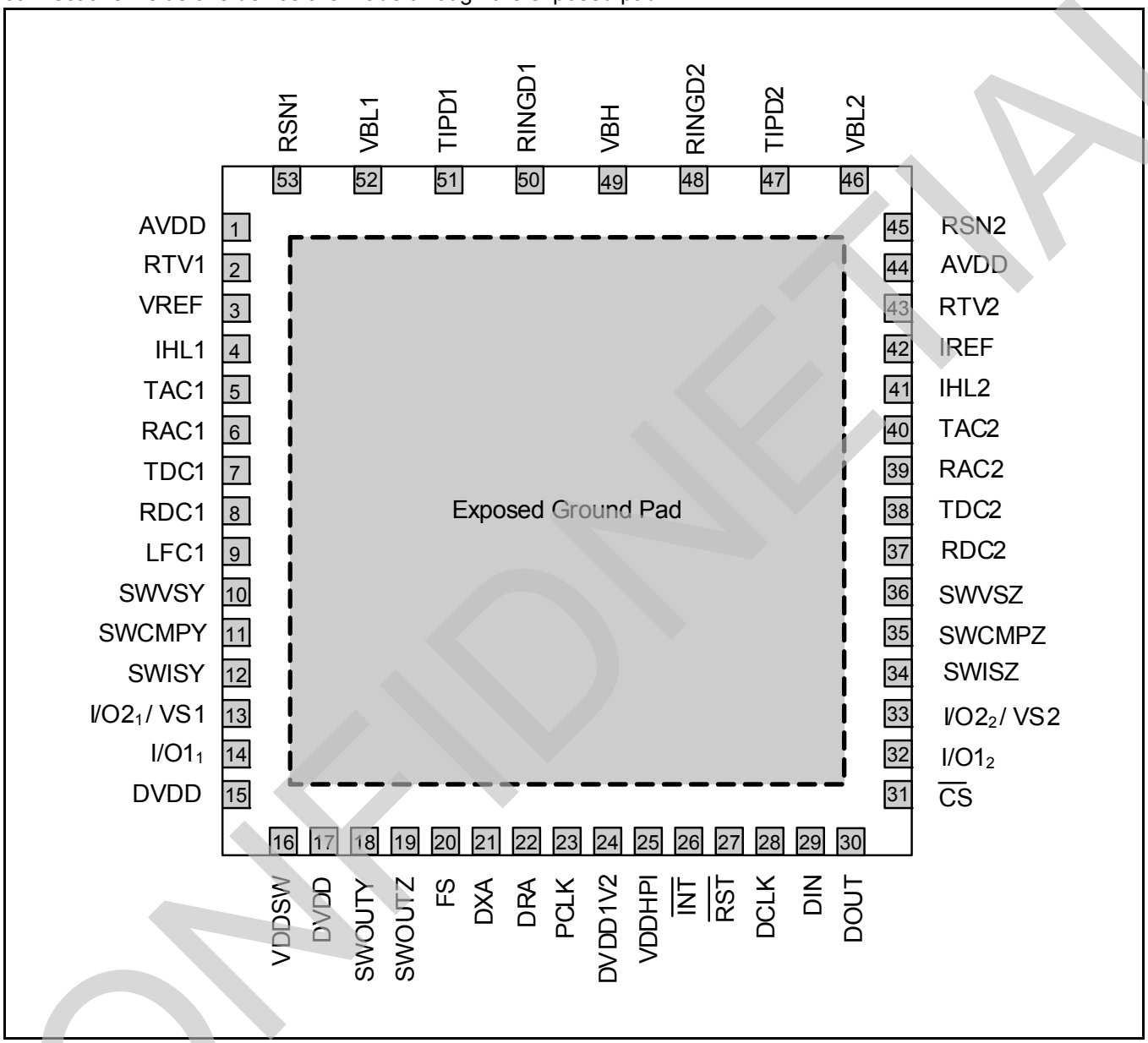



**Figure 36 - Le9622 Device Pinout (QFN-53) - Top View**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | AVDD | Power | 3.3 V Analog supply inputs. |
| 2 | $RTV_1$ | Output | Drive output for two wire AC impedance scaling resistor. |
| 3 | VREF | Output | Analog Voltage Reference. The VREF output has an external 10 µF ceramic capacitor connected to ground, filtering noise present on the internal voltage reference. |
| 4 | $IHL_1$ | Output | High Level Current Drive Filter. |
| 5 | $TAC_1$ | Input | Tip lead AC Sense. A series R + C network is connected from this pin to the Tip lead. |
| 6 | $RAC_1$ | Input | Ring lead AC sense. A series R + C network is connected from this pin to the Ring lead. |
| 7 | $TDC_1$ | Input | Tip lead DC Sense. A resistor is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor. |
| 8 | $RDC_1$ | Input | Ring lead DC Sense. A resistor is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor. |
| 9 | $LFC_1$ | Output | Connection for longitudinal filter capacitor. |
| 10 | SWVSY | Input | Voltage sense for switching regulator controller. |
| 11 | SWCMPY | Output | Compensation connection for switching regulator controller. |
| 12 | SWISY | Input | Current sense input for switching regulator controller. |
| 13 | $I/O2_1$ / VS1 | I/O or Input | General Purpose Input/ Output 2 on Channel 1 or Voltage Sense 1. When configured as a voltage sense input, connect a 1.0 MΩ 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage. |
| 14 | $I/O1_1$ | I/O | General Purpose Input/ Output 1 on Channels 1 and 2, respectively. Each of these two I/O's is capable of driving a 150 mW, 3 V relay (external catch diode required) or an LED, sinking up to 70 mA. |
| 15 | DVDD | Power | +3.3 V Digital power supply inputs. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board. |
| 16 | VDDSW | Power | This voltage is used to drive the switching regulator circuit and is dependent upon the switching regulator design used. This pin must be connected to a +3.3 V supply for bipolar Buck-Boost Automatic Battery Switch designs. Leave open for Inverting Boost Design, with the charge pump enabled. For either design place a 0.1µF ceramic decoupling capacitor between this pin and ground. |
| 17 | DVDD | Power | +3.3 V Digital power supply inputs. For best performance, all of the VDD power supply pins should be connected together at the power supply or power connection to the printed circuit board. Add a 10nF capacitor to ground. |
| 18 | SWOUTY, | Output | Pulse output for gate drive to switching regulator. |
| 19 | SWOUTZ | Output | Pulse output for gate drive to switching regulator. |
| 20 | FS | Input | Interface synchronization signal for PCM voice |
| 21 | DXA | Output | PCM Data Output. PCM is written serially out of the device through this pin, most significant bit first. PCLK determines the data rate. |
| 22 | DRA | Input | PCM Data Input. PCM voice is written serially into the device though this pin, most significant bit first. PCLK determines the data rate. |
| 23 | PCLK | Input | PCM Data Clock 1.024 to 8.192 MHz. This is the clock for the PCM interfaces. |
| 24 | DVDD1V2 | Output | Internally generated 1.2 V supply. Connect a 0.1 µF ceramic decoupling capacitor between this pin and ground. |
| 25 | VDDHPI | Power | Digital power supply input for SPI and PCM pins. Place a 0.1 µF ceramic decoupling capacitor between this pin and ground. |
| 26 | $\overline{INT}$ | Output | Interrupt. $\overline{INT}$ is an active low output signal, which is programmable as either 3 V CMOS compatible or open drain (with external 4.7 KΩ pull up resistor to VDDHPI required). This pin features a weak (1.0 MΩ ) internal pull up to VDDHPI. |
| 27 | $\overline{RST}$ | Input | Device Hardware Reset. A logic Low signal at this pin resets the device to its default state. |

| Pin | Name | Type | Description |
|---|---|---|---|
| 28 | DCLK | Input | Data Clock. In the PCM and SPI mode, the Data Clock input shifts data into and out of the microprocessor interface of the device. The maximum clock rate is 8.192 MHz. This pin features a weak (1.0 MΩ ) internal pull up to VDDHPI. |
| 29 | DIN | Input | Data Input. Control data is serially written into the device via the DIN pin, most significant bit first. The Data Clock determines the data rate. This pin features a weak (1.0 MΩ ) internal pull up to VDDHPI. |
| 30 | DOUT | Output | Data Output. Control data is serially written out of the device via the DOUT pin, most significant bit first. The Data Clock determines the data rate. DOUT is high impedance except when data is being transmitted, which allows DIN and DOUT to be directly tied together in systems which use a single line for data input and output. This pin features a weak (1.0 MΩ ) internal pull up to VDDHPI. |
| 31 | $\overline{CS}$ | Input | Chip Select input (active low) enables the device so that control data can be written to or read from the part. This pin features a weak (1.0 MΩ ) internal pull up to VDDHPI. |
| 32 | $I/O1_2$ | I/O | General Purpose Input/ Output 1 on Channels 1 and 2, respectively. Each of these two I/O's is capable of driving a 150 mW, 3 V relay (external catch diode required) or an LED, sinking up to 70 mA. |
| 33 | $I/O2_2$ / VS2 | I/O or Input | General Purpose Input/ Output 2 on Channel 2 or Voltage Sense 2. When configured as a voltage sense input, connect a 1.0 MΩ 1% resistor between this pin and the voltage to be monitored. The maximum working voltage rating of the resistor must be higher than the monitored voltage. |
| 34 | SWISZ | Input | Current sense input for switching regulator controller. |
| 35 | SWCMPZ | Output | Compensation connection for switching regulator controller. |
| 36 | SWVSZ | Input | Voltage sense for switching regulator controller. |
| 37 | $RDC_2$ | Input | Ring lead DC Sense. A resistor is connected from this pin to the Ring lead. The connection can be to either side of the protection resistor. |
| 38 | $TDC_2$ | Input | Tip lead DC Sense. A resistor is connected from this pin to the Tip lead. The connection can be to either side of the protection resistor. |
| 39 | $RAC_2$ | Input | Ring lead AC sense. A series R + C network is connected from this pin to the Ring lead. |
| 40 | $TAC_2$ | Input | Tip lead AC Sense. A series R + C network is connected from this pin to the Tip lead. |
| 41 | $IHL_2$ | Output | High Level Current Drive Filter. |
| 42 | IREF | Input | Current Reference. An external resistor RREF connected between this pin and analog ground generates an accurate current reference used by the analog circuits on the chip. |
| 43 | $RTV_2$ | Output | Drive output for two wire AC impedance scaling resistor. |
| 44 | AVDD | Power | 3.3 V Analog supply inputs. |
| 45 | $RSN_2$ | Input | High voltage line drive receive current summing node for each channel. |
| 46 | $VBL_2$ | Supply | Low (Off Hook) Battery Supply. |
| 47 | $TIPD_2$ | Output | TIP-lead (A) output to two wire line. |
| 48 | $RINGD_2$ | Output | RING-lead (B) output to the two wire line. |
| 49 | VBH | Supply | High (On Hook, OHT, and Ringing) Battery Supply, and bias voltage for the high voltage line driver. |
| 50 | $RINGD_1$ | Output | RING-lead (B) output to the two wire line. |
| 51 | $TIPD_1$ | Output | TIP-lead (A) output to two wire line. |
| 52 | $VBL_1$ | Supply | Low (Off Hook) Battery Supply. |
| 53 | $RSN_1$ | Input | High voltage line drive receive current summing node for each channel. |
| | Exposed Ground Pad (EPAD/GND) | Power | Thermal Pad and Circuit Ground. Connect to a ground plane on the printed circuit board for thermal conduction and electrical connection to ground return. This is the only ground connection on the device. |

# 8.0 Application Information

## 8.1 Line Interface Circuit

Figure 37 below shows a typical line interface circuit for the Le9622. Decoupling, filtering, and reference generation components are also shown. An example ABS switching regulator circuit is shown in Figure 8.2.1 on page 59. Consult Microsemi for the latest reference design.

### 8.1.1 Line Interface Circuit Schematic

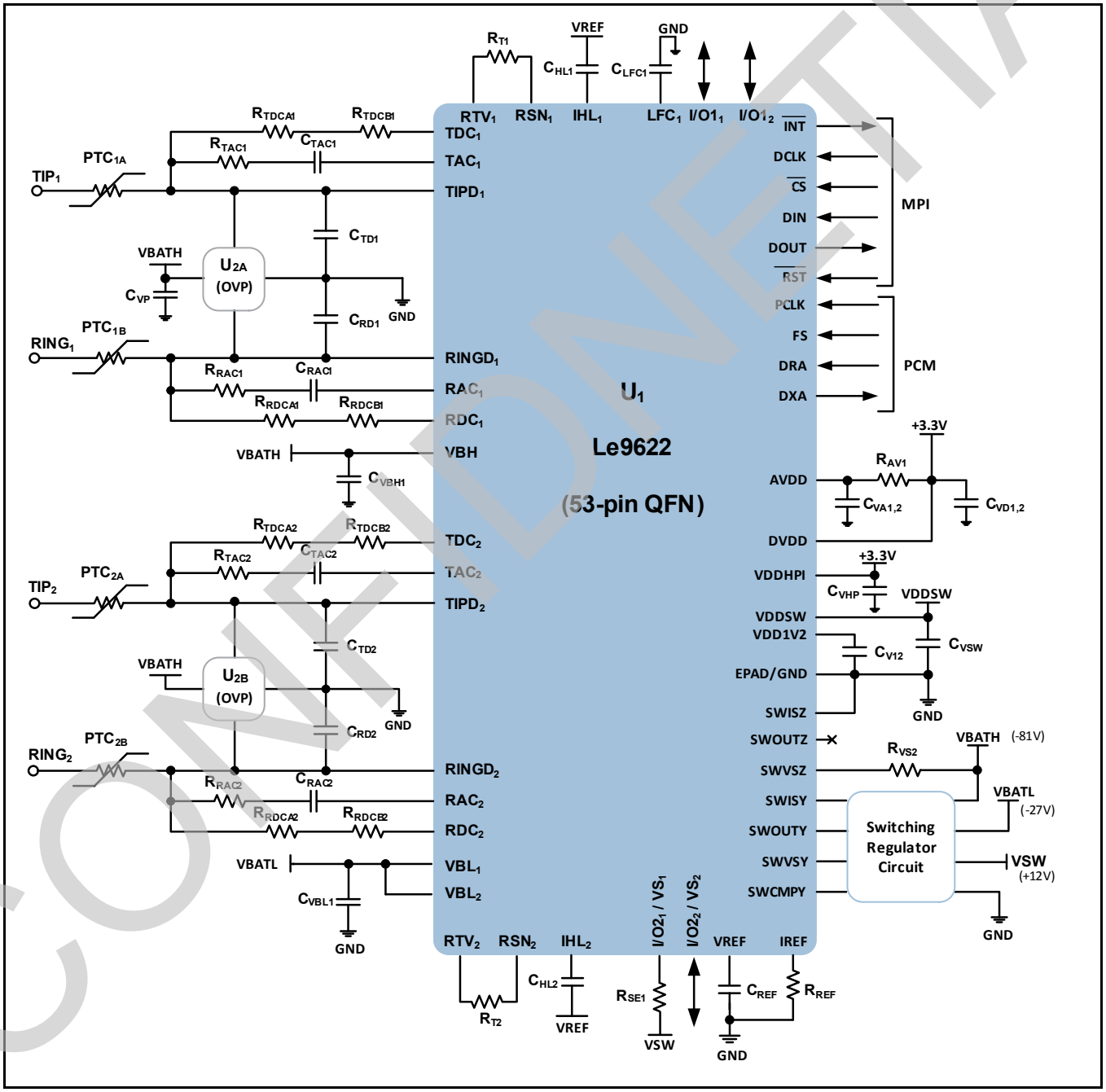



**Figure 37 - Le9622 Line Interface Circuit**

### 8.1.2 Line Interface Circuit Bill of Materials

| Qty. | Item | Type | Value | Tol. | Rating | Size | Note |
|---|---|---|---|---|---|---|---|
| 4 | $C_{HL1}$, $C_{HL2}$, $C_{VA1}$, $C_{VD1}$ | Ceramic Capacitor | 4.7 µF, X5R | 20% | 6.3 V | 0402 | |
| 3 | $C_{LFC1}$, $C_{V12}$, $C_{VA2}$ | Ceramic Capacitor | 0.1 µF, X7R | 10% | 16 V | 0402 | |
| 8 | $C_{RAC1}$, $C_{RAC2}$, $C_{RD1}$, $C_{RD2}$, $C_{TAC1}$, $C_{TAC2}$, $C_{TD1}$, $C_{TD2}$ | Ceramic Capacitor | 0.022 µF, X7R | 10% | 100 V | 0603 or 0805 | *1.* |
| 1 | $C_{REF}$ | Ceramic Capacitor | 10 µF, X5R | 10% | 6.3 V | 0603 | |
| 1 | $C_{VBH1}$ | Ceramic Capacitor | 0.01 µF, X7R | 20% | 250 V | 0805 | |
| 1 | $C_{VBL1}$ | Ceramic Capacitor | 0.01 µF, X7R | 10% | 50 V | 0603 | |
| 2 | $C_{VD2}$, $C_{VHP}$ | Ceramic Capacitor | 0.01 µF, X7R | 10% | 16 V | 0402 | |
| 1 | $C_{VP}$ | Ceramic Capacitor | 0.1 µF, X7R | 10% | 100 V | 0805 | *1.* |
| 1 | $C_{VSW}$ | Ceramic Capacitor | 0.1 µF, X7R | 10% | 16 V | 0402 | |
| 2 | $P_{TC1}$, $P_{TC2}$ | Dual Matched PTC Thermistors | 7 Ω, 0.13 A Hold | 20% | 250 $V_{RMS}$ / 3A | | *2., 3.* |
| 1 | $R_{AV1}$ | Resistor | 1.0 Ω | 5% | 1/10 W | 0402 | |
| 1 | $R_{RAC1}$,$R_{RAC2}$, $R_{TAC1}$, $R_{TAC2}$ | Resistor | 10 KΩ | 1% | 150 V | 0805 | |
| 8 | $R_{RDCA1}$,$R_{RDCA2}$, $R_{RDCB1}$,$R_{RDCB2}$, $R_{TDCA1}$, $R_{TDCA2}$, $R_{TDCB1}$, $R_{TDCB2}$ | Resistor | 499 KΩ | 1% | 200 V | 1206 | |
| 1 | $R_{REF}$ | High-Precision Thin Film Resistor | 75.0 KΩ | 0.5%, 25ppm | 1/16 W | 0402 | *4.* |
| 1 | $R_{SE1}$ | Resistor | 1.0 MΩ | 1% | 50 V | 0402 | *5.* |
| 1 | $R_{T1}$, $R_{T2}$ | Resistor | 47.5 KΩ | 1% | 1/16 W | 0402 | |
| 1 | $R_{VS2}$ | Resistor | 1.00 MΩ | 1% | 150 V | 0805 | |
| 1 | $U_1$ | IC, Dual Channel Wideband ABS VoicePort | *Microsemi Le9622* | | -100 V/-120 V | QFN-53 | |
| 1 | $U_2$ | IC, Programmable Dual Channel SLIC Protector | *Bourns TISP61089Q* or *TISP6NTP2C*, *STMicro LCDP1521S* | | -150 V/30 A | SOIC-8 | *2.* |

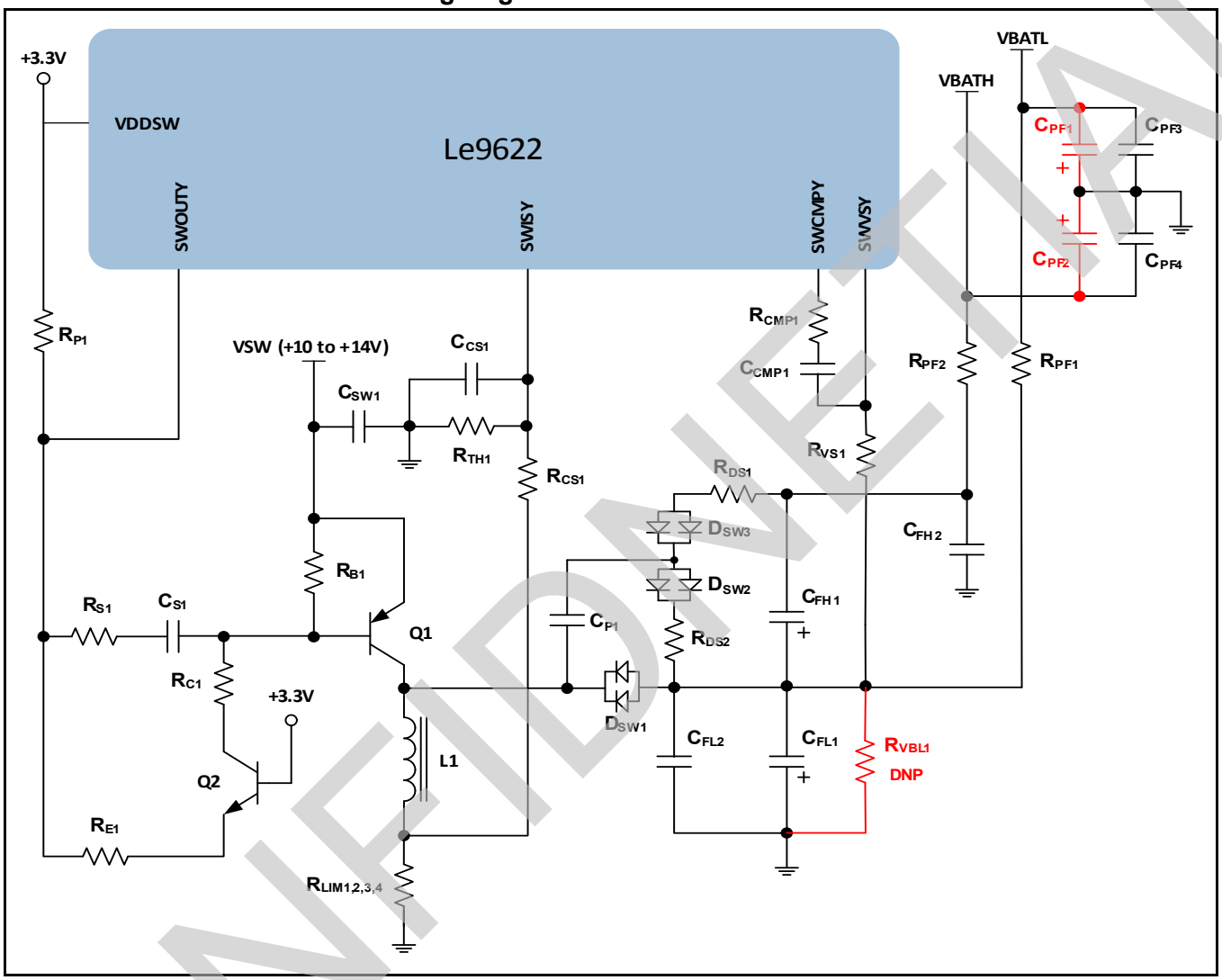
***Notes:***

1. *For Le9622 based designs with ≥ 70 $V_{PK}$ maximum ringing, the rating of these capacitors should be increased to 200 V or 250 V.*
2. *Protection components depend on the target application. The components on the BOM are believed to be suitable for ITU-T Recommendation K.21 (Basic Level) and Telcordia GR-1089-CORE Intra-Building compliance. Please check with Microsemi CMPG Customer Applications for component selection for other safety or EMC standards.*
3. *Recommended dual PTCs include Bourns CMF-SDP07 or MF-SD013/250.*
4. *The tolerance and stability of this resistor are critical as they affect calibration and measurement accuracy. Microsemi recommends using resistors with 0.5% tolerance and 25 ppm/°C temperature coefficient for most applications. Examples include Susumu RR0510P-753-D, Panasonic ERA-2AED753X, and Yageo RT0402DRD0775KL. For high performance applications, 0.1% 25 ppm/°C resistors such as Panasonic ERA-2AEB753X or Yageo RT0402BRD0775KL are recommended.*
5. *Populate only to sense the voltages shown on the schematic. Always make sure that these resistors are selected so that their maximum working DC voltage rating is more than the desired sensed voltage.*

## 8.2 *Patented* BBABS Switching Regulator Circuit

The Patented BBABS switching regulator circuit uses an inverting buck-boost inductor based architecture with voltage-doubler that regulates off of the low battery supply. Consult Microsemi for the most recent reference design.

### 8.2.1 *Patented* BBABS Switching Regulator Circuit



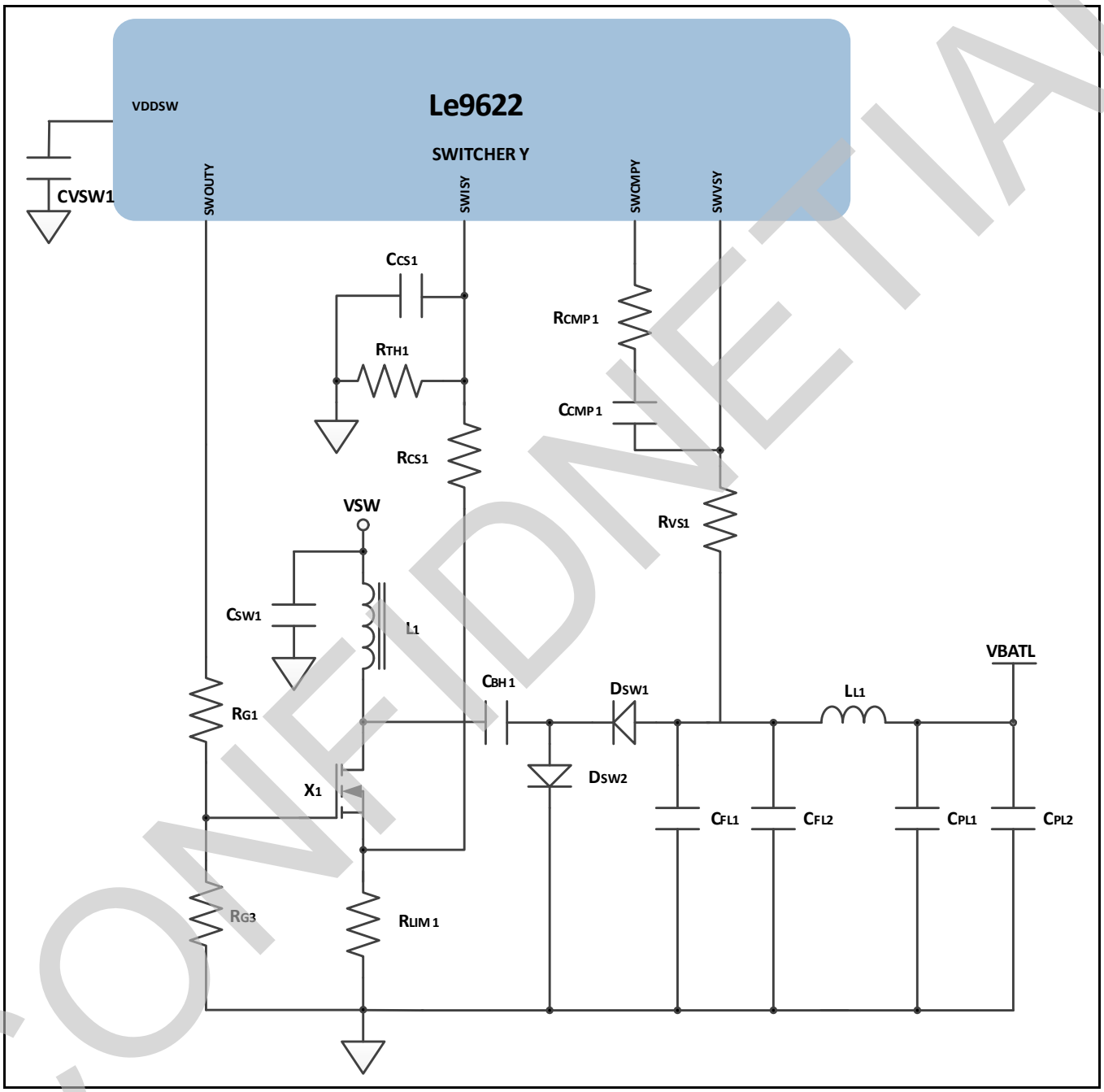
### 8.2.2 BBABS Switching Regulator Circuit Bill of Materials (for VBATH 95V Maximum)

| Qty. | Item | Type | Value | Tol. | Rating | Size | Notes |
|---|---|---|---|---|---|---|---|
| 1 | $C_{CMP1}$ | Ceramic Capacitor | 0.0022 µF, X7R | 10% | 16 V | 0402 | |
| 1 | $C_{CS1}$ | Ceramic Capacitor | 220 pF, X7R | 10% | 25 V | 0402 | |
| 2 | $C_{FH1}$, $C_{FL1}$ | Electrolytic Capacitor | 10 µF | 20% | 63 V | | |
| 2 | $C_{FH2}$, $C_{PF4}$ | Ceramic Capacitor | 0.1 µF, X7R | 10% | 100 V | 0805 | |
| 2 | $C_{FL2}$, $C_{PF3}$ | Ceramic Capacitor | 0.1 µF, X7R | 10% | 50 V | 0603 | |
| 1 | $C_{P1}$ | Ceramic Capacitor | 0.22 µF, X7R | 10% | 100 V | 0805 | |
| 1 | $C_{PF1}$ | Electrolytic Capacitor | 2.2 µF | 20% | 50 V | | Do not populate |
| 1 | $C_{PF2}$ | Electrolytic Capacitor | 1.0 µF | 20% | 100 V | | Do not populate |
| 1 | $C_{S1}$ | Ceramic Capacitor | 0.1 µF, X7R | 10% | 25 V | 0603 | |
| 1 | $C_{SW1}$ | Electrolytic Capacitor | 220 µF, Low ESR | 20% | 25 V | | |
| 3 | $D_{SW1}$,$D_{SW2}$, $D_{SW3}$ | Ultrafast Diode | BAV70 | | 70 V | | |
| 1 | L1 | Power Inductor | 47 µH | 20% | 1.5 A $I_{SAT}$ | | |
| 1 | $Q_1$ | Transistor | PNP, Low Vce, *ZXTP2013G Diodes Inc.® or equivalent* | | 100 V | SOT223 | |
| 1 | $Q_2$ | Transistor | NPN, *MMBT3904 Diodes Inc.® or equivalent* | | | SOT23 | |
| 1 | $R_{B1}$ | Resistor | 1 KΩ | 5% | 1/16 W | 0402 | |
| 2 | $R_{C1}$, $R_{E1}$ | Resistor | 75 Ω | 5% | 1/10 W | 0603 | |
| 1 | $R_{CMP1}$ | Resistor | 1.0 MΩ | 1% | 1/16 W | 0402 | |
| 1 | $R_{CS1}$ | Resistor | 3.48 KΩ | 1% | 1/16 W | 0402 | |
| 2 | $R_{DS1}$, $R_{PF2}$ | Resistor | 10 Ω | 5% | 1/4 W | 1206 | |
| 2 | $R_{DS2}$, $R_{PF1}$ | Resistor | 5.1 Ω | 5% | 1/4 W | 1206 | |
| 4 | $R_{LIM1}$, $R_{LIM2}$, $R_{LIM3}$, $R_{LIM4}$ | Resistor | 1.0 Ω | 5% | 1/16 W | 0402 | |
| 1 | $R_{P1}$ | Resistor | 10 KΩ | 5% | 1/16 W | 0402 | |
| 1 | $R_{S1}$ | Resistor | 0 Ω | 5% | 1/16 W | 0402 | |
| 1 | $R_{TH1}$ | Resistor | 1 KΩ | 1% | 1/16 W | 0402 | |
| 1 | $R_{VBL1}$ | Resistor | 51 KΩ | 5% | 1/10 W | 0603 | Do not populate |
| 1 | $R_{VS1}$ | Resistor | 1.0 MΩ | 1% | 1/8 W | 0805 | |

## 8.3 Multi-Line Inverting Boost Automatic Battery Switch (ABS) Switching Regulator Circuit

The multi-line design uses two independent inverting boost DC/DC converters to create the VBATL and VBATH battery supplies. Consult Microsemi for the most recent reference design.

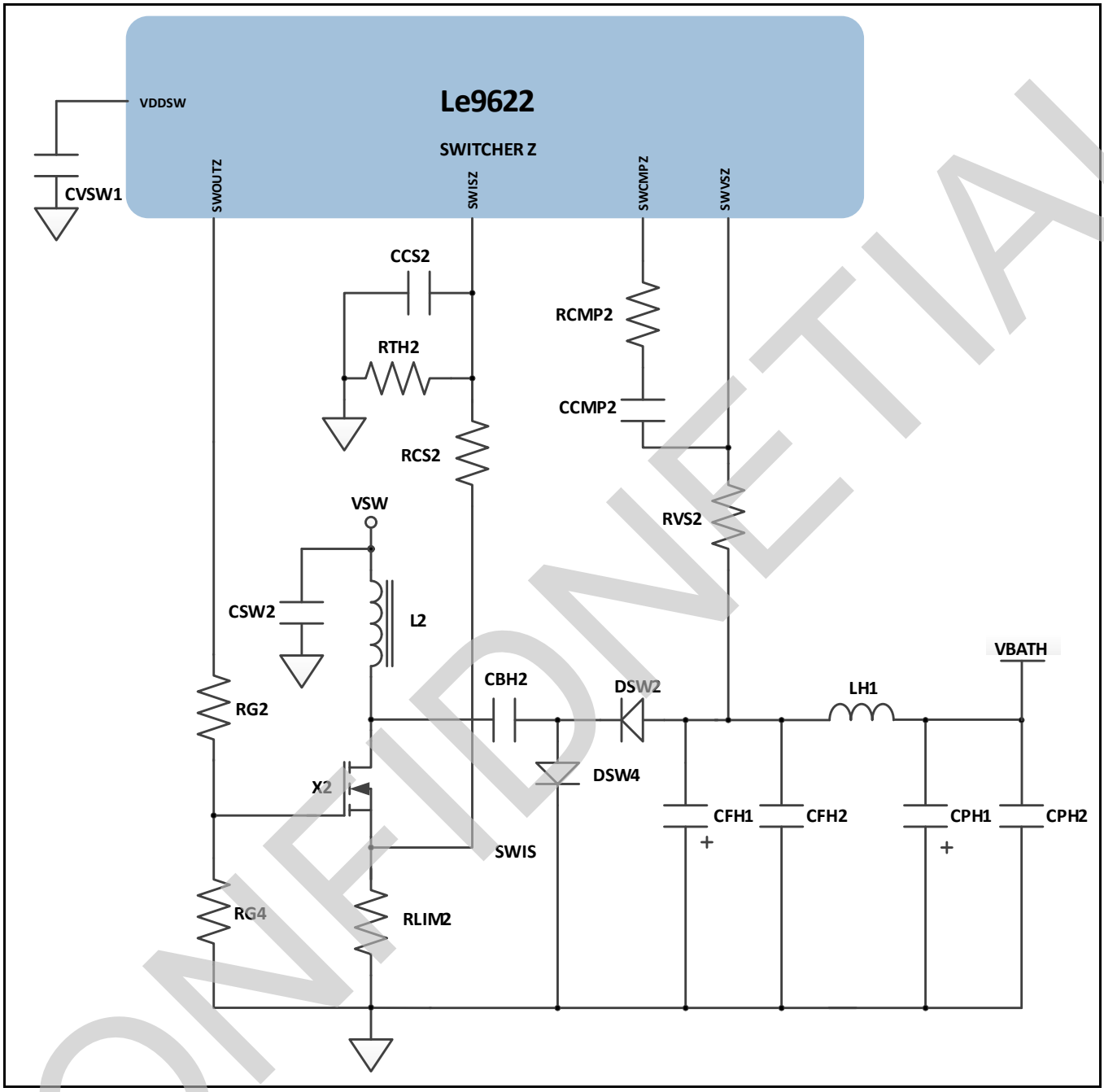
### 8.3.1 Multi Line ABS - VBATL Schematic



### 8.3.2 Multi Line ABS - VBATL Bill of Materials (for VBATL 50V Maximum)

| Qty | Item | Type | Value | Tol. | Rating | Size | Note |
|---|---|---|---|---|---|---|---|
| 1 | $C_{CMP1}$ | Ceramic Cap | 1800pF X7R | 10% | 16V | 0402 | |
| 1 | $C_{CS1}$ | Ceramic Cap | 220pF X7R | 10% | 16V | 0402 | |
| 1 | $C_{SW1}$ | Ceramic Cap | 10uF X5R | 10% | 25V | 1206 | |
| 1 | $C_{BH1}$ | Ceramic Cap | 0.22uF X7R | 10% | 100V | 0805 | |
| 4 | $C_{FL1}$ $C_{LF2}$ $C_{PL1}$ $C_{PL2}$ | Ceramic Cap | 1uF X5R | 10% | 100V | 1206 | |
| 2 | $D_{SW1}$ $D_{SW2}$ | Rectifier Diode | ES1D | | 200V | SMA | Trr<50ns |
| 1 | $L_1$ | Power Inductor | 6.8uH | 20% | 3.8A | 6mm | Bourns SRN6045-6R8Y NIC NPIS65LS6R8MTRF |
| 1 | $L_{L1}$ | Chip Inductor | 10uH | 20% | Isat>250ma | 1008 | Taiyo Yuden CBC2518T100M |
| 1 | $R_{G1}$ | Resistor | 10R | 5% | 1/16W | 0402 | |
| 1 | $R_{G3}$ | Resistor | 10K | 5% | 1/16W | 0402 | |
| 1 | $R_{CS1}$ | Resistor | 2K | 1% | 1/16W | 0402 | |
| 1 | $R_{CMP1}$ | Resistor | 1Meg | 1% | 1/16W | 0402 | |
| 1 | $R_{TH1}$ | Resistor | 3.01K | 1% | 1/16W | 0402 | |
| 1 | $R_{LIM1}$ | Resistor | 0.05ohm | 1% | 1/4W | 1206 | Stackpole CSR1206FT050L0 |
| 1 | $X_1$ | MOSFET | <100mohm | | 60V | SOT223 | Diodes DMN6068SE |

### 8.3.3 Multi Line ABS - VBATH Schematic



### 8.3.4 Multi Line ABS - VBATH Bill of Materials (for VBATH 90V Maximum)[1]

| Qty | Item | Type | Value | Tol. | Rating | Size | Note |
|---|---|---|---|---|---|---|---|
| 1 | CSWB1 | Electrolytic Cap | 220uF Low Imp | 20% | 25V | 8mm TH | Panasonic EEUFM1E221 |
| 1 | $C_{CMP1}$ | Ceramic Cap | 1800pF X7R | 10% | 16V | 0402 | |
| 1 | $C_{CS1}$ | Ceramic Cap | 220pF X7R | 10% | 16V | 0402 | |
| 1 | $C_{SW1}$ | Ceramic Cap | 10uF X5R | 10% | 25V | 1206 | |
| 1 | $C_{BH1}$ | Ceramic Cap | 0.22uF X7R | 10% | 200V | 1210 | |
| 1 | $C_{FL1}$ | Electrolytic Cap | 22uF Low Imp | 20% | 100V | 8mm TH | Panasonic EEUFC2A220 |
| 1 | $C_{PH1}$ | Electrolytic Cap | 1uF | 20% | 100V | 5mm TH | Nichicon UPW2A010MDD |
| 2 | $C_{FH2}$ $C_{PH2}$ | Ceramic Cap | 0.1uF X7R | 10% | 100V | 0805 | |
| 2 | $D_{SW1}$ $D_{SW2}$ | Rectifier Diode | ES1D | | 200V | SMA | Trr<50ns |
| 1 | $L_1$ | Power Inductor | 4.7uH | 20% | 4.7A | 8mm | Bourns SRN8040-4R7Y<br>Taiyo Yuden NR8040T4R7N |
| 1 | $L_{L1}$ | Chip Inductor | 10uH | 20% | Isat>250ma | 1008 | Taiyo Yuden CBC2518T100M |
| 1 | $R_{G1}$ | Resistor | 10R | 5% | 1/16W | 0402 | |
| 1 | $R_{G3}$ | Resistor | 10K | 5% | 1/16W | 0402 | |
| 1 | $R_{CS1}$ | Resistor | 2K | 1% | 1/16W | 0402 | |
| 1 | $R_{CMP1}$ | Resistor | 1Meg | 1% | 1/16W | 0402 | |
| 1 | $R_{TH1}$ | Resistor | 2K | 1% | 1/16W | 0402 | |
| 1 | $R_{LIM1}$ | Resistor | 0.05ohm | 1% | 1/4W | 1206 | Stackpole CSR1206FT050L0 |
| 1 | $X_1$ | MOSFET | <200mohm | | 100V | SOT223 | Fairchild FDT86113<br>Fairchild FDT86106 |

*1. Consult Microsemi Applications for -115V Maximum VBATH Design*

# 9.0 Programming the Le9622

The Le9622 device is programmed through the *VoicePath Application Program Interface II (VP-API-II).* This API hides the complexity of the device and its internal registers and provides a much simpler interface to the software engineer. The *VoicePath Software Development Kit (SDK)* accelerates the development cycle and reduces the development time. It also allows the user to build on proven software that is currently used to control over 100 million subscriber lines worldwide.

## 9.1 Programmable Features

The features directly supported by *VP-API-II* are dependent upon the underlying device capabilities. The following features are supported by the *VP-API-II* for the Le9622:

- AC and DC coefficient programming
- Ringing parameter (amplitude, frequency, bias, type) and power management
- Tone generation (frequency, amplitude, and modulation)
- Programmable tone and ringing cadence
- Universal Caller ID generation (Types 1 and 2) with FSK and DTMF signaling
- Loop start signaling, including dial pulse detection
- Ground start signaling
- Seamless integration of the Microsemi *VeriVoice Professional Test Suite Software* for *Telcordia® GR-909-CORE* metallic loop testing
- Three modes of interrupt support (Level Triggered, Efficient Polling and Simple Polling)

## 9.2 VoicePath SDK Overview

The *VP-API-II* is an OS independent, C source library that abstracts the Microsemi ZL880, VE880, VE890 and miSLIC™ device registers into a common application interface used for configuration and control of the devices.

Two versions of the *VP-API-II* are available from the Microsemi Software Delivery System (SDS) web site – http://sds.microsemi.com/software.php. The first version of the software (*LE71SK0002*) contains the full software source and requires a Software License Agreement (SLA). The second version of the software (*LE71SDKAPIL*) called *VP-API-II Lite* is a subset of the full *VP-API-II* source and allows for basic configuration, control and event handling of the devices. The *Lite* version does not include Caller ID generation, tone or ringing cadence support. *VP-API-II Lite* does not require an SLA and is suitable for open-source applications. The miSLIC device is supported by *VP-API-II* versions 2.25.0 and later.

The following sections cover the more commonly used aspects of the *VP-API-II*. See the *VoicePath API-II Reference Guide (Doc ID #143271)* for complete coverage of this software.

### 9.2.1 Introduction

The Microsemi V*oicePath Application Programming Interface II* (*VP-API-II*) is a C source code module that provides a standard software interface for controlling, testing, and passing digitized voice through a set of subscriber lines using the Microsemi family of voice termination devices. This section describes a few of the device and line control capabilities using the *VP-API-II* interface. For a complete list, refer to *VP-API-II Reference Guide*. *VP-API-II* uses the layered architecture shown below. The block in the diagram in blue outline and bold print is Microsemi provided code, the blocks in gray outline are customer provided code. The solid blue block is the actual Microsemi device.

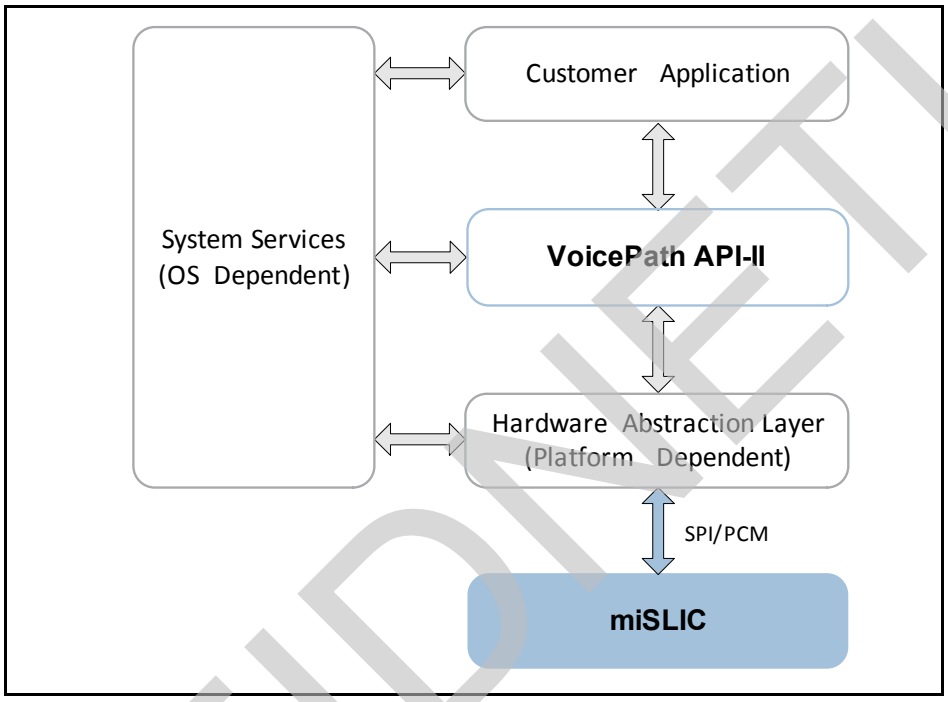



**Figure 38 - VP-API-II Software Architecture**

### 9.2.2 Customer Application

This block represents the user's line management module that performs tasks such as initializing the system, configuring lines, changing the line states in response to line events and other inputs, switching digitized voice traffic, etc. Microsemi provides example implementations of this layer as part of the *VoicePath SDK*.

### 9.2.3 VoicePath API-II

The *VoicePath API-II* is the core component of the Microsemi *VoicePath SDK*. This software module runs on the host microprocessor that controls one or more Microsemi voice telephony devices. This code is provided by Microsemi and should not require modification by the application developer.

### 9.2.4 Hardware Abstraction Layer

The Hardware Abstraction Layer (HAL) provides access to Microsemi voice telephony devices through the SPI interface, depending on the selected device and mode. The HAL software is platform dependent and must be implemented by the *VP-API-II* user. Microsemi provides example HAL source code with the *VoicePath SDK*.

### 9.2.5 System Services Layer

The System Services layer provides critical section, timing and interrupt control functions. These functions are system dependent and must be implemented specifically for each platform on which the *VP-API-II* is used. Microsemi provides example System Services code for use with the Microsemi *ZTAP*. The following functions are included in the System Services layer.

| Function Name | Description |
|---|---|
| `VpSysEnterCritical()` | A semaphore operation to provide protected access to device or shared memory. Required only in multi-threaded architectures. |
| `VpSysExitCritical()` | A semaphore operation to release protected access to device or shared memory. Required only in multi-threaded architectures. |
| `VpSysWait()` | Delay operator used to suspend program/thread execution. Delay parameter passed in 125 µs steps. |
| `VpSysDebugPrintf()` | Print mechanism used by *VP-API-II* debug features. |
| `VpSysTestInt()` | Interrupt function for Efficient Poll Mode. Required for backward compatibility with *VE880* code. |

**Table 10 - VP-API-II Functions for System Services**

## 9.3 System Configuration Functions

Two main functions in *VP-API-II* are required in all applications are listed below:

| Function Name | Description |
|---|---|
| `VpMakeDeviceObject()` | Configures a specific device (chip select) to a device context. Provides *VP-API-II* with device specific type (*`deviceType`*). |
| `VpMakeLineObject()` | Configures a specific line (channel) to a line and device context. Provides *VP-API-II* with line specific type (*`termType`*). |

**Table 11 - VP-API-II Functions for System Configuration**

When using the Le9622 device, the following settings must be used:

- The value for *`deviceType`* in `VpMakeDeviceObject()` must be: `VP_DEV_886_SERIES`
- The value for *`termType`* in `VpMakeLineObject()` must be:
  - `VP_TERM_FXS_GENERIC` when *`channelId`* = 0 and Normal Standby operation is desired
  - `VP_TERM_FXS_LOW_PWR` when *`channelId`* = 0 and Low Power Standby operation is desired.

Please refer to *VP-API-II Reference Guide* for additional details.

## 9.4 Initialization

The *VP-API-II* functions that perform initialization are listed below.

| Function Name | Description |
|---|---|
| `VpInitDevice()` | Resets and initializes device with parameters defined in the specified *Profiles*. |
| `VpInitLine()` | Resets and initializes line with parameters defined in the specified *Profiles*. |
| `VpInitRing()` | User function to provide Ringing Cadence. Also allows use selection of *Caller ID Profile* associated with ringing. |

## 9.5 Line State Control

The following sections describe the Line State information to perform control functions such as DC feed, ringing generation, and channel line test.

| Function Name | Description |
|---|---|
| VpSetLineState() | Sets line to state specified. After VpInitDevice() or VpInitLine(), the default line state is VP_LINE_DISCONNECT. |

**Table 12 - VP-API-II Functions for Line State Control**

### 9.5.1 VP_LINE_DISCONNECT

In the VP_LINE_DISCONNECT state, the SLIC block outputs are shut off providing a high impedance to the line. This state can be used for denial of service. The switching regulator is active and outputs the programmed SWFV floor voltage. The voice channel is normally deactivated, but can be activated and used with the converter configuration command to monitor the voltages on Tip or Ring for line diagnostics.

### 9.5.2 VP_LINE_STANDBY

The VP_LINE_STANDBY state is used when On-Hook. This state behaves differently based on the FXS line termination type selected according to "System Configuration Functions" on page 67.

If the termination type VP_TERM_FXS_GENERIC is selected, the DC feed is active, and hook supervision functions are enabled. The loop feed polarity is controlled by the *VP-API-II*. The high voltage switching regulator only generates the voltage needed to support the DC line voltage defined by the DC feed curve shown in Figure 3.8 on page 23. The DC feed drives Tip and Ring to the programmed VOC. Voice transmission is disabled to save power.

If the termination type VP_TERM_FXS_LOW_PWR is selected, a special *Low Power Idle Mode (LPIM)* state is supported to reduce on-hook power consumption, while still being able to detect off-hook transitions. In this mode, the DC feed is not active and a voltage is presented to the Ring lead. The line voltage is monitored so that any transitions to off-hook state can be detected. Voice transmission is disabled in this state.

### 9.5.3 VP_LINE_OHT, VP_LINE_OHT_POLREV

In the VP_LINE_OHT states, the DC feed is activated and voice transmission is enabled. VP_LINE_OHT allows the transmission of Caller ID information. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

### 9.5.4 VP_LINE_ACTIVE, VP_LINE_ACTIVE_POLREV, VP_LINE_TALK, VP_LINE_TALK_POLREV

In the VP_LINE_ACTIVE and VP_LINE_TALK states, the DC feed is activated. The PCM highway is enabled in VP_LINE_TALK and disabled in VP_LINE_ACTIVE. Both states allow the transmission of Caller ID information for Type 2 Caller ID. Hook supervision functions are operating. The switching regulator only generates the negative high voltage needed to support the DC line voltage defined by the DC feed curve. In this way, power consumption is minimized.

### 9.5.5 VP_LINE_TIP_OPEN

In the VP_LINE_TIP_OPEN state, the device provides a high impedance on the Tip lead and drives the Ring lead to the programmed VOC voltage. The loop supervision detector monitors the ground key current. When this current is larger than the programmed threshold, the *VP-API-II* reports a ground start event. This state can also be used to determine Ring to ground leakage and Ring to ground capacitance in combination with the appropriate converter configuration.

### 9.5.6 VP_LINE_RING_OPEN

In the VP_LINE_RING_OPEN state, the device provides a high impedance on the Ring lead and drives the Tip lead to the programmed VOC voltage. The loop supervision detector monitors the ground key current. When this current is larger than the programmed threshold, the *VP-API-II* reports a ground start event. This state can also be used to determine Tip to ground leakage and Tip to ground capacitance in combination with the appropriate converter configuration.

### 9.5.7 VP_LINE_RINGING, VP_LINE_RINGING_POLREV

In the VP_LINE_RINGING state, the voice DAC is used to apply the ringing signal generated from Signal Generator A and the Bias generator to the SLIC block. Internal feedback maintains a low (200 Ω) system output impedance during ringing. The current limit is increased in the *Ringing* state and is programmable via the parameter, ILR. In order to minimize line transients, entry and exit from the VP_LINE_RINGING states are intelligently managed by the Le9622. When ringing is requested by the user, the corresponding signal generators are started but not applied to the subscriber line until the ringing voltage is equal to the on-hook Tip-Ring voltage. This algorithm, known as *Ring Entry*, assures that there is a smooth line transition when entering the VP_LINE_RINGING state. *Ring Entry* is guaranteed to occur within one period of the programmed ringing frequency. *Ring Exit i*s an analogous procedure whereby the ringing signal is not immediately removed from the line after a ring trip or new state request. The ringing signal will persist until its voltage is equal to the required line voltage. Ring Entry and Ring Exit are configured using the VP-API-II function VP_OPTION_ID_RING_CNTRL.

While in the VP_LINE_RINGING state, the integrated switching regulator must be programmed for ABS mode. Note that these three topologies require different external switching power supply components. See “Device Profile” on page 73 for information on setting the switcher topology.

### 9.5.8 VP_LINE_HOWLER, VP_LINE_HOWLER_POLREV

In the VP_LINE_HOWLER state, the transmit (A to D) voice path and impedance generation are disabled. Gain is increased by 11.5 dB compared to a 0 dBr D/A setting.

## 9.6 VpShutdownDevice()

This function puts all lines into the VP_LINE_DISABLED state, shuts down all power supplies, stops all timers, and masks all interrupts for the specified device. The device must be reinitialized with VpInitDevice() to be used again.

## 9.7 Line Status Monitoring

Line Status is monitored by the *VP-API-II* using the functions listed in Table 13.

| Function Name | Description |
|---|---|
| VpGetEvent() | Typically used to implement event driven method to monitor line status. Provides event queue such that a single event reported for each instance function is called (when an event is active). |
| VpGetLineStatus() | Typically used to implement polling method to monitor line status. |
| | • VP_INPUT_HOOK -- Hook Status timing per Dial Pulse Detection. |
| | • VP_INPUT_RAW_HOOK -- Real time hook status. Changes during Dial Pulse |
| | • VP_INPUT_GKEY -- Real time ground key status. |

**Table 13 - VP-API-II Functions for Line Status Monitoring**

## 9.8 Input / Output Control

The Le9622 device features four general purpose I/O pins that can be configured by the user as inputs, outputs, or relay drivers. All I/O pins are configured and accessed through the *VP-API-II* using the functions listed in Table 14

| Function Name | Description |
|---|---|
| `VpSetOption()` | `VP_DEVICE_OPTION_ID_DEVICE_IO` - Used to configure pins individually as input, output, or as a voltage sense pin. The parameter *`directionPins_31_0`* used to set pin as input (0) or output (1). The bit in *`directionPins_31_0`* corresponding to I/O is ($I/O1_1$ = 0x1, $I/O1_2$ = 0x2, $I/O2_1$= 0x4, and $IO2_2$ = 0x8). Other bits in *`directionPins_31_0`* are ignored.<br>Configuring output type done by setting corresponding bit location in *`outputTypePins_31_0`* with `VP_OUTPUT_DRIVEN_PIN` (driven). Note that when writing a '1' to a driven pin results in voltage being present on the corresponding I/O pin. |
| `VpGetOption()` | `VP_DEVICE_OPTION_ID_DEVICE_IO` - Retrieves current I/O pin configuration. When calling `VpGetOption()`, an event (Response Category, Event ID `VP_LINE_EVID_RD_OPTION`) is generated and must be processed by the host application. The host application then calls `VpGetResults()` with pointer to structure of type `VpOptionDeviceIoType` that is filled in by *VP-API-II* with current I/O configuration data. |
| `VpDeviceIoAccess()` | The *`accessMask_31_0`* parameter provides bit field access to the I/O pins as ($I/O1_1$ = 0x1, $I/O1_2$ = 0x2, $I/O2_1$= 0x4, and $IO2_2$ = 0x8). Access is by 'OR' combination, so *accessMask_31_0* = 0x0F provides access to all lines simultaneously.<br>The `accessType` parameter indicates read (`VP_DEVICE_IO_READ`) or write (`VP_DEVICE_IO_WRITE`) operation.<br>For write operation, *`deviceIOData_31_0`* is used to set lines to '0' or '1'. The bit mask is same as *`accessMask_31_0`* ($I/O1_1$ is set to value in *`deviceIOData_31_0`* location 0x1, $I/O1_2$ in *`deviceIOData_31_0`* location 0x2, and so on). All other parameters (*`accessMask_63_32`* and *`deviceIOData_63_32`*) are ignored for the Le9622) |

**Table 14 - VP-API-II Functions for Configuring and Accessing I/O Lines**

## 9.9 VoicePath API-II Software and QuickStarts

Both versions of the *VP-API-II* software are distributed with minimalistic examples known as QuickStarts. These examples are intended to provide *VP-API-II* users with a starting point for their end application. The QuickStarts show how to properly setup, initialize, and configure the VP-API. Additionally, the examples show how to properly respond to VP-API events. The QuickStarts code also provide examples of the platform specific Hardware Abstraction Layer and System Service Layer functions discussed in 9.2.4, "Hardware Abstraction Layer" and 9.2.5, "System Services Layer".

## 9.10 DTMF

The VP-API II offers a software based DTMF (Dual-tone Multi-frequency) signal detection feature for Microsemi miSLIC™ devices. This feature can be used for applications where the host processor does not have access to voice data and therefore cannot run its own DTMF decode algorithm.

## 10.0 VP-API-II Profiles

*Profiles* are structures that contain design data to meet specific system requirements. Many *VP-API-II* functions take *Profiles* as one or more arguments. There are several types of *Profiles*. Each defines a different set of parameters for a service aspect of the device. Table 15 provides a summary of all the *Profiles* that are used by the *VP-API-II* with the Le9622 device. *Profiles* are created using *VP Profile Wizard*.

| Profile Name | Description |
|---|---|
| Device | The *Device Profile* provides default start-up values for device specific configuration options that are normally set at initialization and never changed. These options include the Pulse Code Modulation (PCM) bus clock frequency and configuration information, interrupt mode, voltage monitoring mode, dial pulse correction, device mode register, and switching regulator configuration. |
| AC FXS | Used for programming the transmission characteristics of the system, the *AC FXS Profile* holds the programmable gain and filter coefficient data. Over 70 country specific *AC FXS Profiles* are provided and the user can select the one or ones that are required for his or her application. |
| DC | The *DC Profile* holds the DC feed and loop supervision parameters. |
| Ringing | The *Ringing Profile* contains the necessary commands and data to set up the ring generator of an FXS channel. Different *Profiles* can be used to vary the ringing characteristics of a line. Options available in the *Ringing Profile* include ringing waveform, frequency, amplitude, DC offset, ring trip method, maximum peak power, and ring cadence control. |
| Tone | The *Tone Profile* defines the various call progress tones that might be used in the FXS channel. The tones include dial tone, busy, ring back, re-order, and howler. This *Profile* is compatible with the one used with the *VE880* family. |
| Ringing Cadence | The *Ringing Cadence Profile* defines the cadence that is associated with ringing. This *Profile* is compatible with the one used with the *VE880* family. |
| Tone Cadence | The *Tone Cadence Profile* defines the various call progress cadences that might be used in a system. The cadences include stutter dial, busy, ring back, and reorder. This *Profile* is compatible with the one used with the *VE880* family. |
| Caller ID | The *Caller ID Profile* defines the on- and off-hook signal generation for services such as Caller ID and message waiting indication. This *Profile* abstracts the physical and data link layers of the protocol. FSK and DTMF signaling are supported. This *Profile* is compatible with the one used with the *VE880* family. |
| Metering | The *Metering Profile* sets the frequency (12kHz or 16kHz), transition type, peak current, and echo voltage limits. This *Profile* is not compatible with the one used with the *VE880* family due to added parameters. |

**Table 15 - VP-API-II Profile Types**

### 10.1 Profile Wizard Project Definition

The *Profile Wizard* application allows the user to define the requirements of the telephone line characteristics, switching and signaling with an intuitive user interface. After selecting the requirements, the user can generate the corresponding *Profiles* (.c and .h files) which the *VP-API-II* software uses to initialize and control the Le9622 device. Microsemi provides many example *Profiles* based on known country or standard requirements.

After launching *Profile Wizard*, it presents the user with the option of creating a new project based on a Microsemi telephony device family or reference design or to open an existing project.

## 10.2 Profile Wizard Main Menu

Figure 39 shows a typical screen shot of the main menu of *Profile Wizard*. Note that the user can select from many standard country *Profiles*. In this example, the default files for Australia are selected.

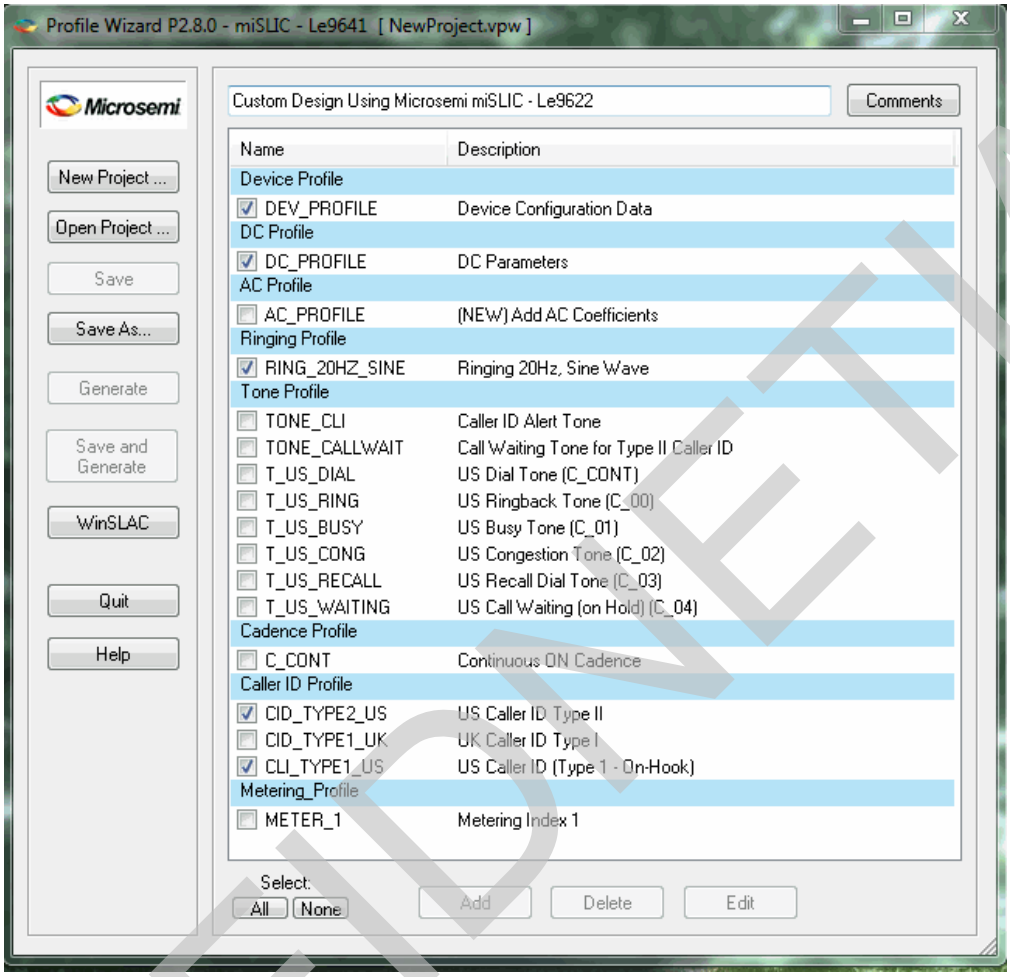



**Figure 39 - Profile Wizard - Main Menu**

## 10.3 Device Profile

### 10.3.1 Overview

The *Device Profile* configures device or circuit level parameters for the entire device. This *Profile* is required to enable reliable host communication with the device, to configure the switching regulator, and to define *VP-API-II* driver parameters. An example *Device Profile* configuration for the *miSLIC*$^{TM}$ using *VP Profile Wizard* is shown below.

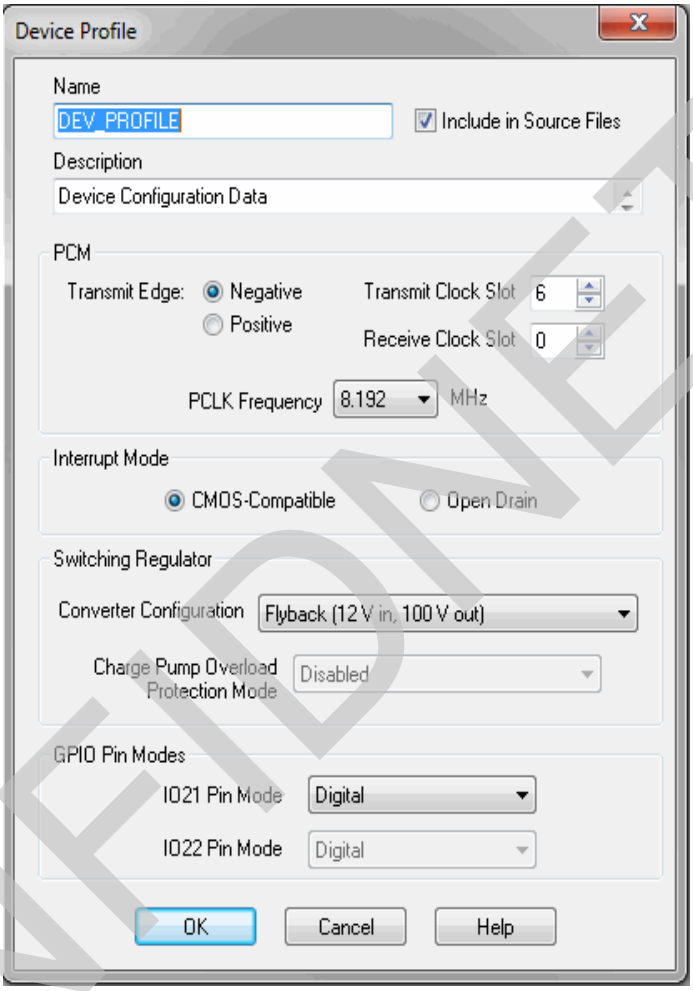



**Figure 40 - Profile Wizard - Device Profile Configuration**

Table 16 lists the *VP-API-II* functions which use values that are defined in the *Device Profile*.

| Function Name | Description |
|---|---|
| `VpInitDevice()` | Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters. |
| `VpCalLine()` | This function may need to be called under some circumstances following the above function. Refer to the *VP-API-II Reference Guide* for more details. |

**Table 16 - VP-API-II Functions for Device Configuration**

## 10.4 AC FXS Profiles

*AC FXS Profiles* are used to define the input impedance, receive and transmit frequency response, hybrid balance, and initial gain values. Microsemi provides *AC FXS Profile* examples for over 70 countries including the following:

| Input Impedance | Network Balance Impedance | Notes |
|---|---|---|
| 150 Ω + (510 Ω // 47 nF) | 150 Ω + (510 Ω // 47 nF) | Russia |
| 200 Ω + (680 Ω // 100 nF) | 200 Ω + (680 Ω // 100 nF) | China |
| 220 Ω + (820 Ω // 115 nF) | 220 Ω + (820 Ω // 115 nF) | Bulgaria, Germany, and South Africa |
| 220 Ω + (820 Ω // 120 nF) | 220 Ω + (820 Ω // 120 nF) | Australia |
| 270 Ω + (750 Ω // 150 nF) | 270 Ω + (750 Ω // 150 nF) | Belgium, Croatia, Denmark, Egypt, Estonia, France, Greece, Hungary, Iceland, Ireland, Israel, Italy, Ivory Coast, Netherlands, Nigeria, Norway, Portugal, Romania, Spain, Sweden, Switzerland, and Turkey |
| 270 Ω + (910 Ω // 120 nF) | 270 Ω + (1200 Ω // 120 nF) | Finland |
| 370 Ω + (620 Ω // 310 nF) | 370 Ω + (620 Ω // 310 nF) | New Zealand |
| 300 Ω + (1000 Ω // 220 nF) | 370 Ω + (620 Ω // 310 nF) | United Kingdom |
| 600 Ω | 600 Ω | USA, Argentina, Armenia, Belarus, Canada, Chile, Colombia, Czech Republic, Ecuador, El Salvador, Georgia, Hong Kong, India, Indonesia, Jordan, Korea, Kuwait, Malaysia, Mexico, Pakistan, Paraguay, Peru, Philippines, Poland, Qatar, Saudi Arabia, Singapore, South Korea, Taiwan, Thailand, Ukraine, UAE, Uruguay, and Venezuela. |
| 600 Ω + 1.0 µF | 600 Ω + 1.0 µF | Japan and PBX |
| 900 Ω | 900 Ω | Brazil |
| 900 Ω + 2.16 µF | 800 Ω // (0.05 µF + 100 Ω) | *Telcordia GR-57-CORE* Non-Loaded Loop |

**Table 17 - Supported AC Source Impedances**

**Notes:**

1. *Table 17 provides suggested AC source impedances for the listed countries and are believed to be accurate as of the date of publication of this document. However, standards can and do change from time to time or new ones may be introduced. Some countries may support more than one standard AC source impedance. Customers are responsible for using the appropriate AC FXS Profiles for their application.*
2. *VP Profile Wizard makes it easy to add additional countries as long as they are based on the supported impedances.*
3. *The standard files provided with VP Profile Wizard are for FXS interfaces with two 7 ohm PTC's in series with Tip and Ring. Please contact Microsemi CMPG Customer Applications if alternate series resistor or PTC resistance values are planned.*
4. *Narrowband and Wideband versions of these Profiles are available.*

Table 18 below lists the *VP-API-II* functions that which use values that are defined in the *AC FXS Profile*.

| Function Name | Description |
|---|---|
| `VpInitDevice()` | Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters. |
| `VpInitLine()` | Resets and initializes line with AC, DC, and Ringing parameters. |
| `VpConfigLine()` | Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters. |
| `VpCalLine()` | This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details. |

**Table 18 - VP-API-II Functions Using AC FXS Profile**

## 10.5 DC Profile

*DC Profiles* are used to define the feed and loop supervision conditions of the line. An example *DC Profile* for *miSLIC*™ devices using *VP Profile Wizard* is shown in Figure 41 below.

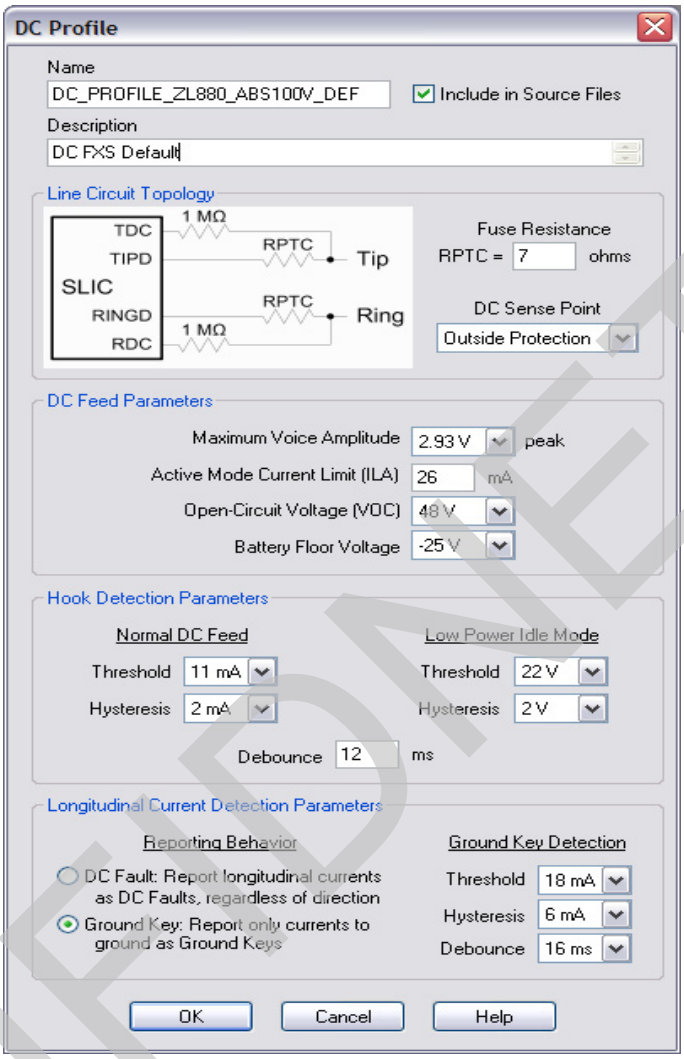



**Figure 41 - Profile Wizard - DC Profile Configuration Example**

Table 19 lists the *VP-API-II* functions which use values that are defined in the *DC Profile*.

| Function Name | Description |
|---|---|
| `VpInitDevice()` | Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters. |
| `VpInitLine()` | Resets and initializes line with AC, DC, and Ringing parameters. |
| `VpConfigLine()` | Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters. |
| `VpCalLine()` | This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details. |

**Table 19 - VP-API-II Functions for DC Feed and Hook Detection Configuration**

## 10.6 Ringing Profile

The *Ringing Profile* is used to define the type of ringing, ringing frequency, amplitude, offset, ring trip threshold, and ringing current limit. The *Ringing Profile* for the Le9622 using *VP Profile Wizard* is shown in Figure 42 below.

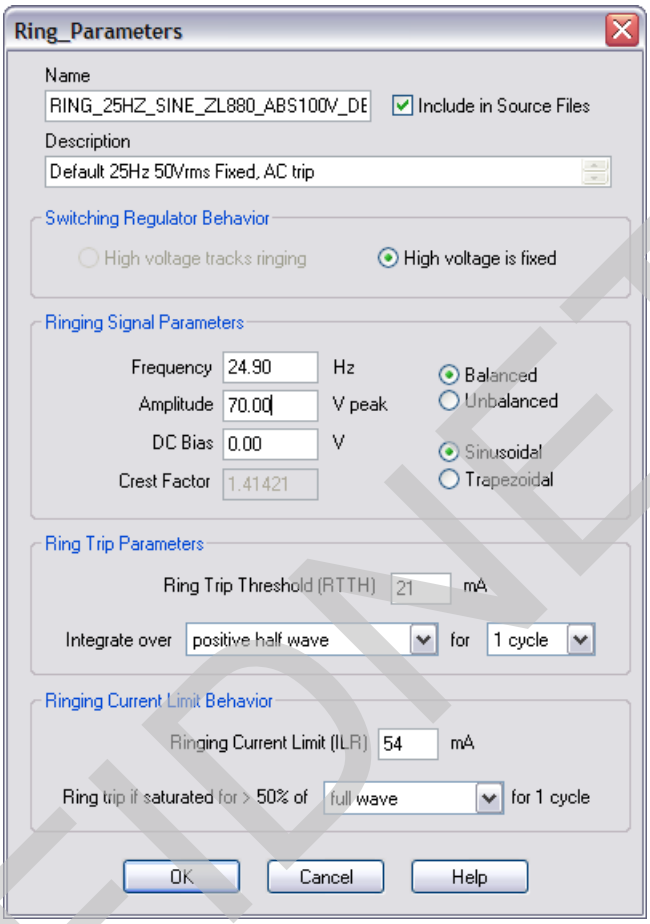



**Figure 42 - Profile Wizard - Ringing Profile Configuration Example**

Table 20 lists the *VP-API-II* functions which use values that are defined in the *Ringing Profile*.

| Function Name | Description |
|---|---|
| `VpInitDevice()` | Resets and initializes device with parameters defined in *Device Profile* and optionally configures all lines on the device with AC, DC, and Ringing parameters. |
| `VpInitLine()` | Resets and initializes line with AC, DC, and Ringing parameters. |
| `VpConfigLine()` | Configures line with AC, DC, and Ringing parameters. Similar to `VpInitLine()` but line is not reset. Values not provided in function call result in line retaining previously set parameters. |
| `VpCalLine()` | This function may need to be called under some circumstances following the functions listed above. Refer to the *VP-API-II Reference Guide* for more details. |

**Table 20 - VP-API-II Functions for Ringing and Ring Trip Definition**

## 10.7 Tone Profile

*Tone Profiles* provide the capability to program up to four simultaneous tones on the line. The *Tone Profile* for the Le9622 using *VP Profile Wizard* is shown in Figure 43 below.

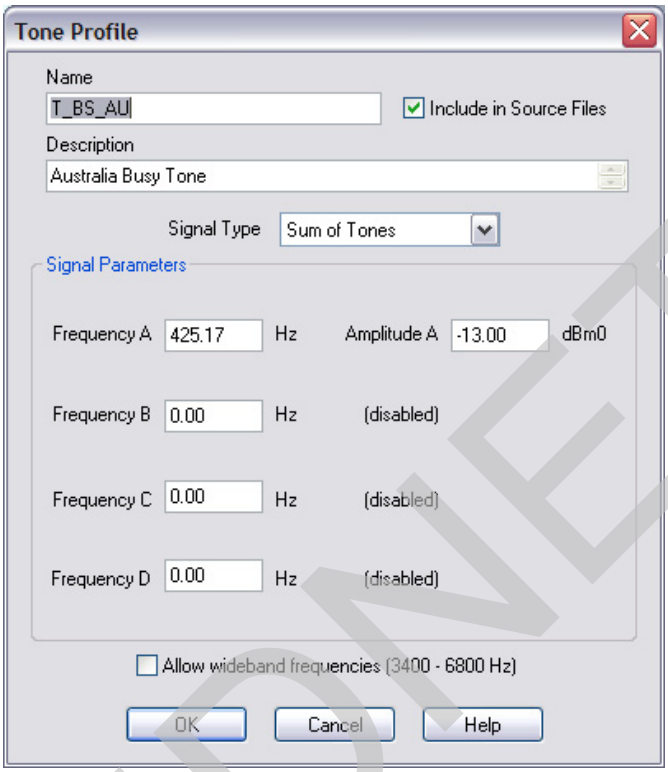



**Figure 43 - Profile Wizard - Tone Profile Configuration Example**

Table 21 lists the *VP-API-II* function which uses values that are defined in the *Tone Profile*.

| Function Name | Description |
|---|---|
| `VpSetLineTone()` | Starts a tone on the line. The tone can be cadenced or “always on”. |

**Table 21 - VP-API-II Function Using Tone Profile**

## 10.8 Tone Cadence Profile

*VP-API-II* Tone Cadencing is a highly flexible set of operators the user selects to implement any country specific ringing or tone cadence requirements including Special Information Tones (SIT) and howler tones. Figure 44 shows how to define cadences for call progress tones with *VP Profile Wizard*.

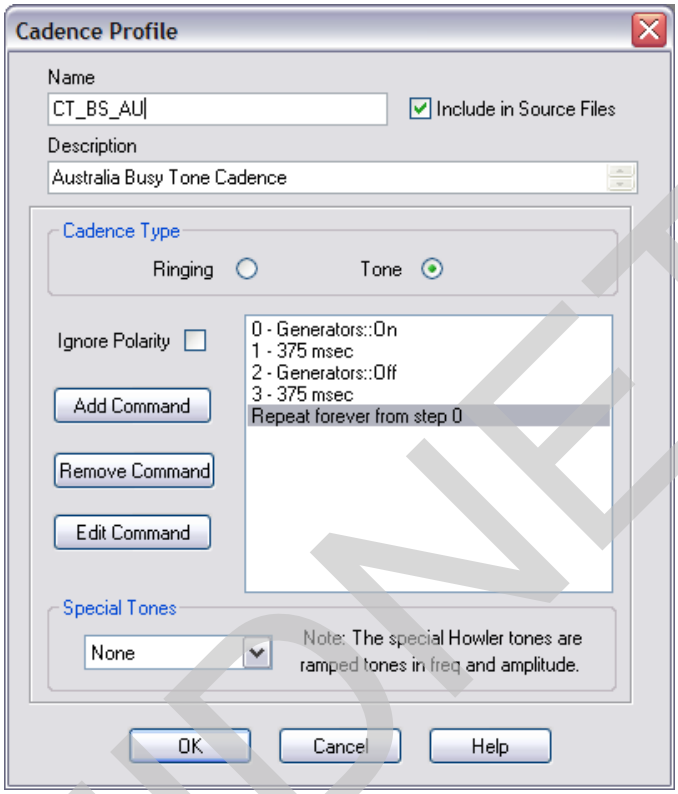



**Figure 44 - Profile Wizard - Tone Cadence Profile Example**

The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* line state.

Table 22 lists the *VP-API-II* function which uses values that are defined in the *Tone Cadence Profile*.

| Function Name | Description |
|---|---|
| `VpSetLineTone()` | Provides tone cadencing for up to four tones. Also supports country specific howler tone cadencing (AUS, UK, NTT) with ramp frequency and amplitude. |

**Table 22 - VP-API-II Function For Tone Cadencing**

## 10.9 Ringing Cadence Profile

*VP-API-II* ringing cadencing is a flexible set of operators the user selects to implement any country specific ringing cadence. Figure 45 shows how to define cadences for ringing generation with *VP Profile Wizard*. Note that events that are associated with Type 1 (on-hook) Caller ID ringing are included by this Profile.

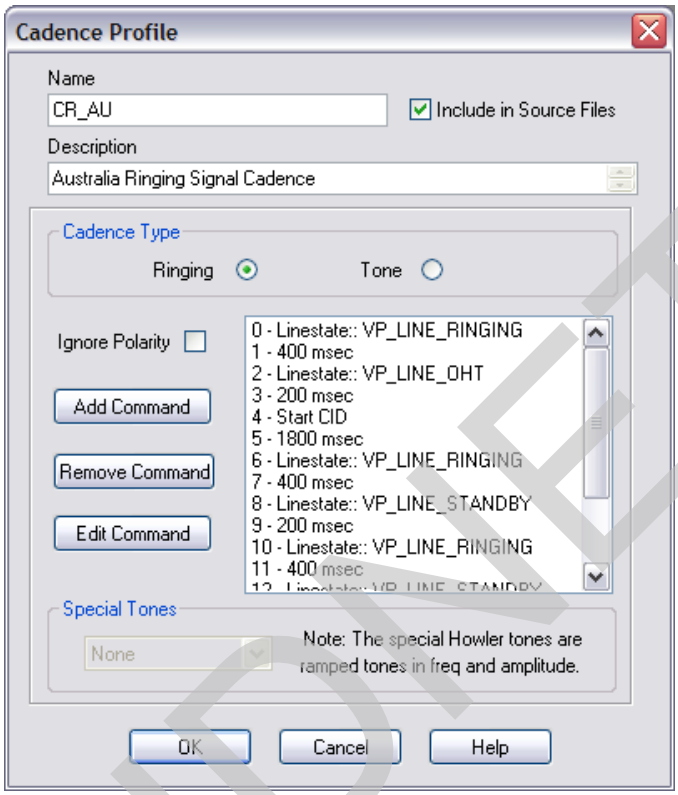



**Figure 45 - Profile Wizard - Ringing Cadence Profile Example**

The *VP-API-II* Cadencer supports the following operations:

1. Time -- Delays (in a non-blocking fashion) program execution.
2. Generator Control -- Enable/Disable selection on a per-generator basis.
3. Branch -- Forces the cadencing to return to a previous step with "repeat" for *n* number of times. If *n* == 0, repeat forever.
4. Line State -- Sets line to specific *VP-API-II* Line State.
5. Send CID -- Starts Caller ID (CID) on the line while continuing to run cadence. Used for Type 1 Caller ID when CID occurs after first regular ringing cycle in order to achieve a precise delay between the first and second rings.
6. Wait On Caller ID -- Starts Caller ID on the line and suspends currently running cadence. Used for Type 1 Caller ID when CID occurs prior to the first regular ringing cycle.

Table 23 lists the *VP-API-II* functions which use values that are defined in the *Ringing Cadence Profile*.

| Function Name | Description |
|---|---|
| `VpSetLineState()` | `VP_LINE_RINGING` and `VP_LINE_RINGING_POLREV` for Ringing Cadence. |
| `VpInitRing()` | User function to provide Ringing Cadence. Also allows use selection of *Caller ID Profile* associated with ringing. |

**Table 23 - VP-API-II Functions For Ringing Cadencing**

## 10.10 Caller ID Profile

The Caller ID block uses Generators C and D to generate phase continuous 1200 baud FSK tones for on- or off-hook information such as Calling Line ID (or Caller ID) and Visual Message Waiting Indication (VMWI). The duration of each (bit) tone is fixed at 0.833 ms (1200 baud).

*Bell 202* tone frequencies are used in the North American and some international markets, and the *ITU-T Recommendation V.23* tone frequencies are used in most of Europe and other international markets. The signal generator amplitude may need to be adjusted depending on the programmed loss plan. Data transmission levels are normally specified as -13.5 dBm +/-1.5 dB.

Exact preamble and mark sequences are generated by adjusting the framing mode and sending the appropriate number of characters. The *VP-API-II* abstracts this into a simple driver level interface. *VP Profile Wizard* enables the user to select the Caller ID parameters and build them into the *Caller ID Profile*, which generates the necessary coefficients and instructions for the *VP-API-II*. Note that the signal level in the example below is -7.5 dBm0, which corresponds to a transmitted signal of -13.5 dBm0 to the line due to the 6 dB D/A loss in the default *AC Profile*.

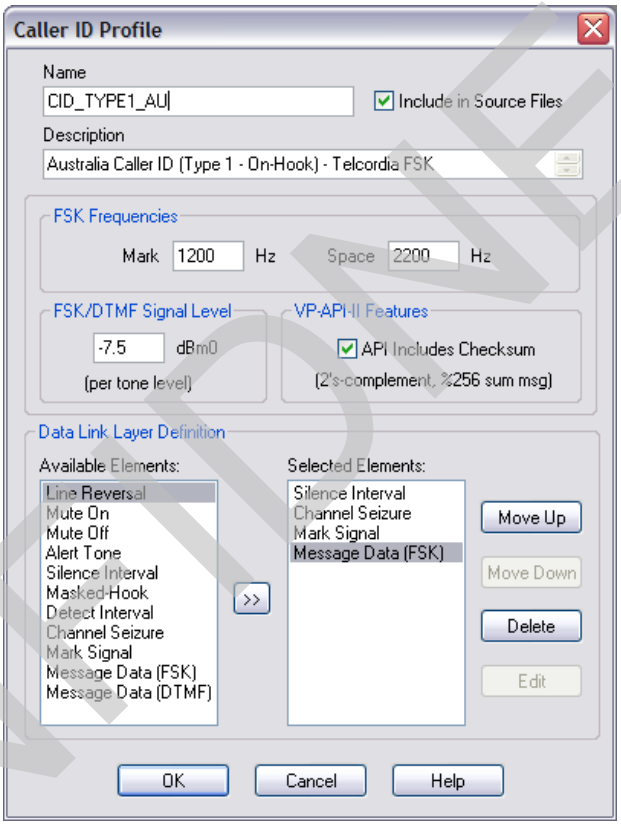



**Figure 46 - Profile Wizard - Type 1 Caller ID Profile Example**

Table 24 lists the *VP-API-II* functions which use values that are defined in the *Caller ID Profile*.

| Function Name | Description |
|---|---|
| `VpInitRing()` | User function to provide *Caller ID Profile* associated with ringing. |
| `VpSendCid()` | Configures and starts Caller ID immediately. Used for Type 2 Caller ID. |
| `VpInitCid()` | Input for Caller ID Message Data up to 32 bytes. |
| `VpContinueCid()` | Input for Caller ID Message Data up to 16 bytes. Called after `VpInitCid()` or `VpSendCid()` when event `VP_LINE_EVID_CID_DATA` is generated. |

**Table 24 - VP-API-II Functions for Caller ID**

### 10.11 Metering Profile

The *Metering Profile* allows the user to define the pulse metering frequency (12 or 16 kHz), peak current, and voltage limit. Figure 47 shows an example screen shot of the *Metering Profile* definition in *VP Profile Wizard*.

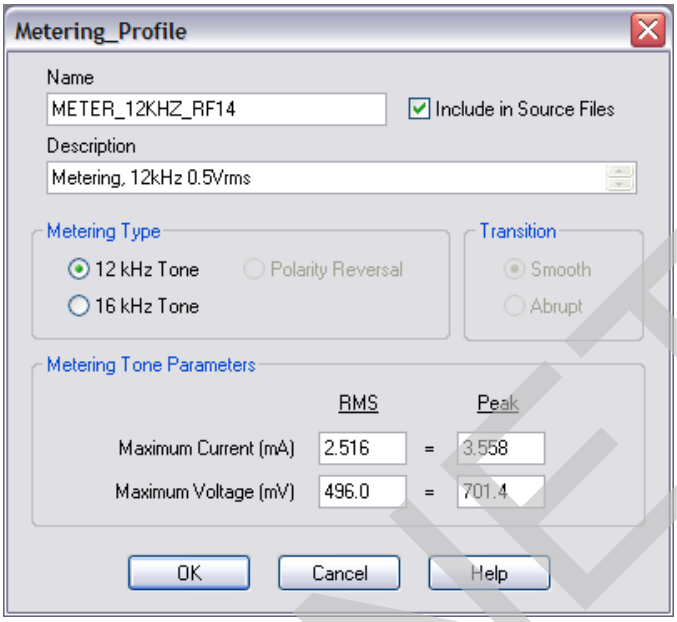



**Figure 47 - Profile Wizard - Metering Profile Example**

Table 25 lists the *VP-API-II* functions which use values that are defined in the *Metering Profile*.

| Function Name | Description |
|---|---|
| `VpInitMeter()` | Configures the metering signal generator of an individual line. |
| `VpStartMeter()` | Starts metering pulses. |

**Table 25 - VP-API-II Functions for Metering**

## 11.0 Package Outline

The package outline and recommended land pattern of the *Le9622 are* described in this section.

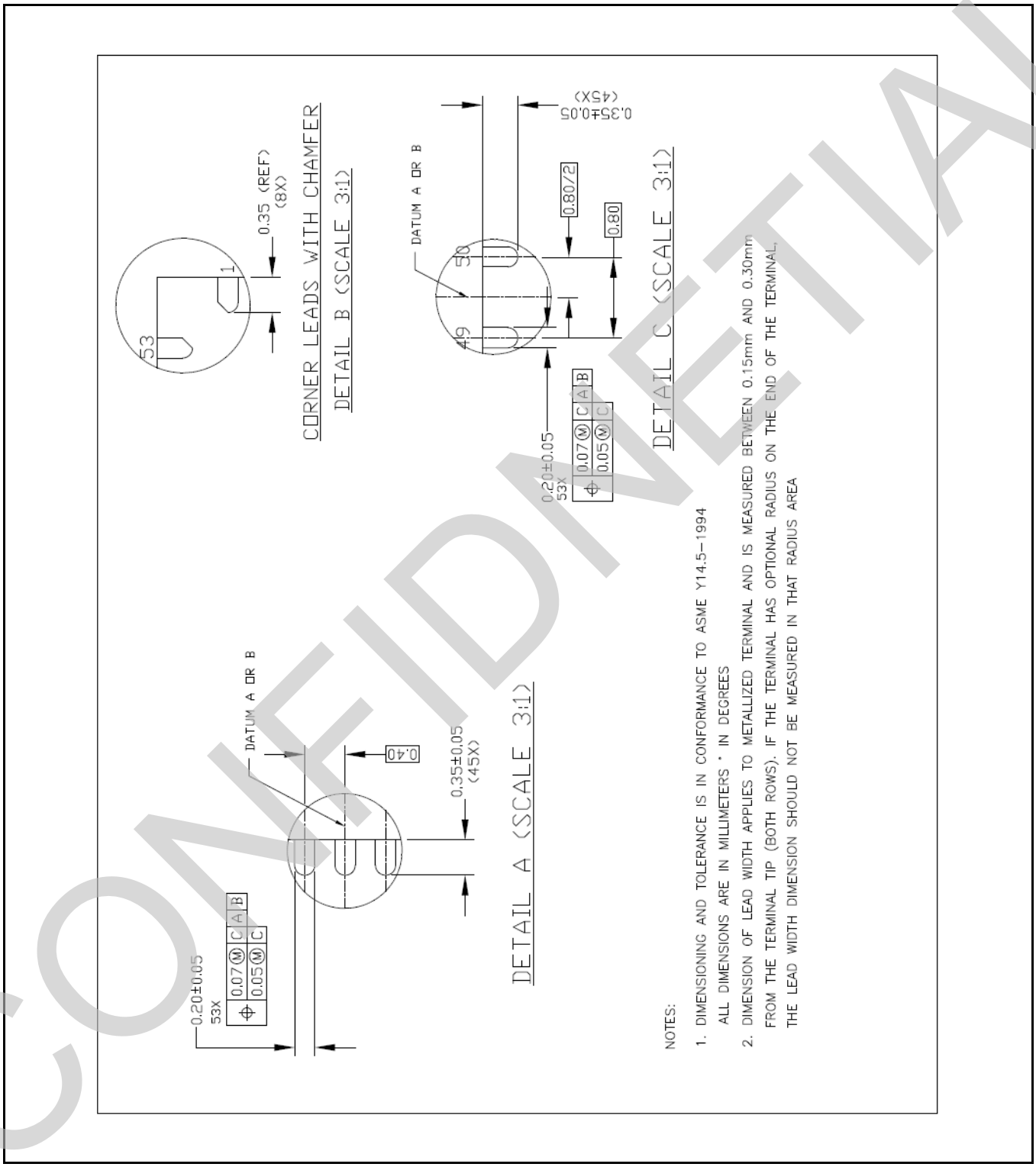



**Figure 48 - Le9622 Package Pin Pitch**

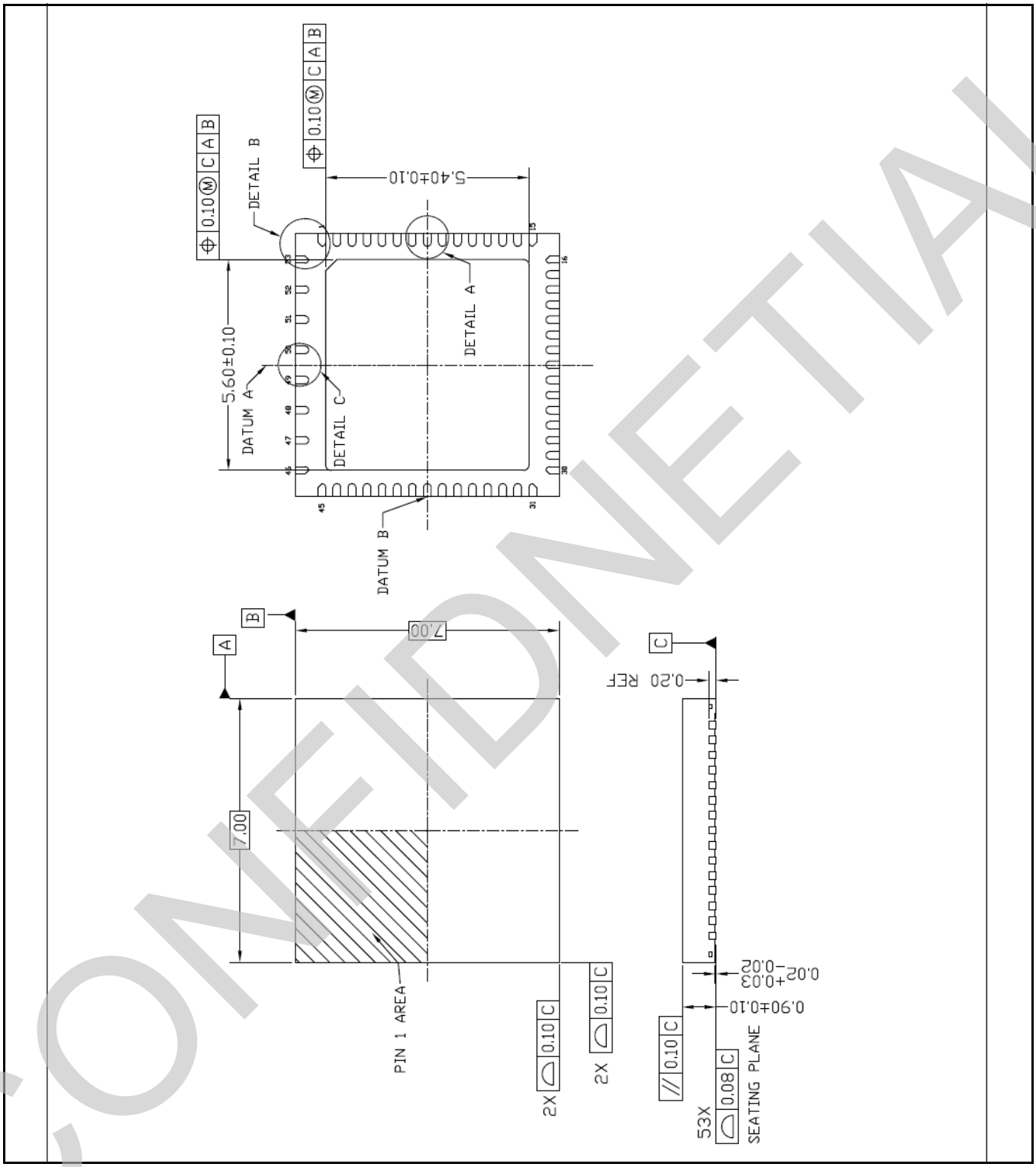
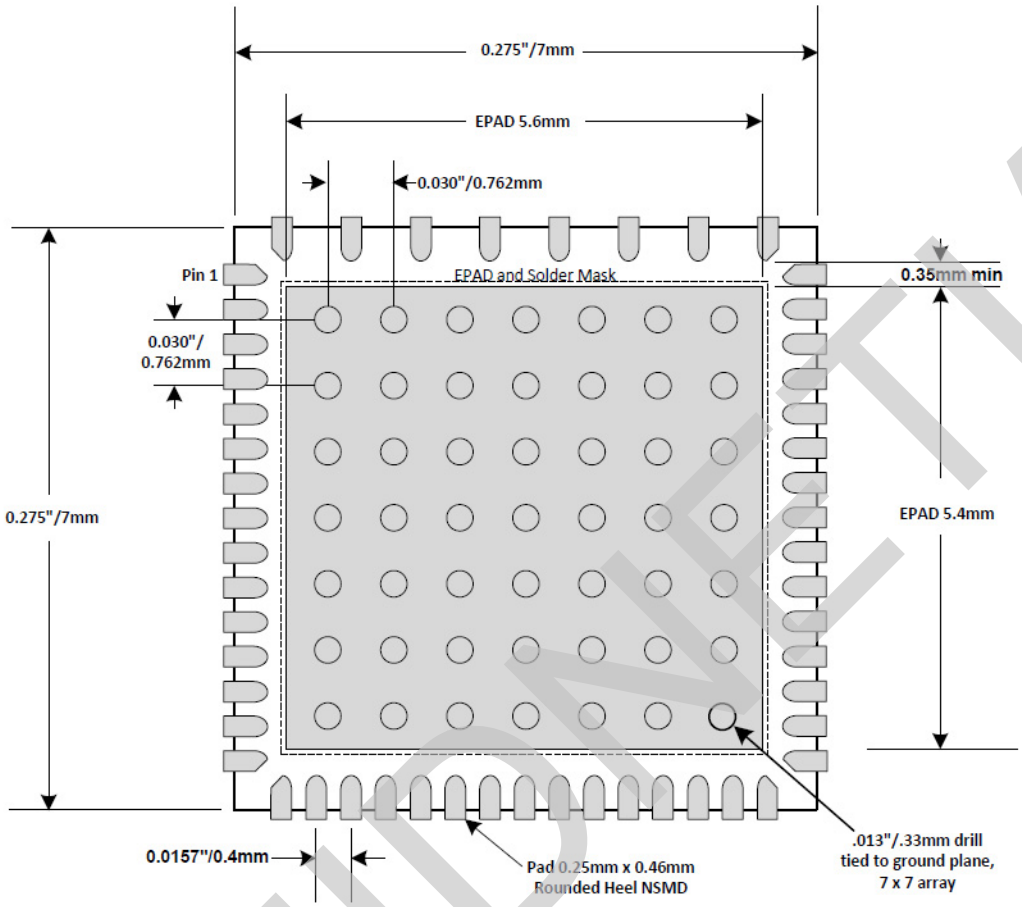



**Figure 49 - Le9622 Package Outline Drawing**

dd




**Microsemi 53-pin QFN**
**7 mm x 7 mm, 0.4 mm pitch**

*Minimum spacing between pins and EPAD must be 0.35 mm.
Recommended EPAD configuration uses 5.4mm x 5.6mm pad tied to a ground plane with an 7x7 array of 0.33 mm vias. This is necessary for good thermal performance.

**Figure 50 - Recommended Land Pattern (QFN-53) - Top View**

# 12.0 Related Collateral

The following documentation is available on the Microsemi website **www.microsemi.com/voice-line-circuits.**

## 12.1 Documentation

- **Le9622 Data Sheet *Document Number* 157378**
- **Le9632Data Sheet *Document Number* 157379**
- **Le9643 Data Sheet *Document Number 157127***
- **Le9653 Data Sheet *Document Number 157152***
- **Le9622/Le9632 Product Brief *Document Number 157380***
- **Le9643/Le9653 Product Brief *Document Number 157126***
- **VP-API-II Reference Guide *Document Number 143271* (*included with software download*)**
- **Line Test API (LT-API) User's Guide *Document Number 081470* (*included with software download*)**
- **VeriVoice Professional Data Sheet *Document Number 1457775* (*included with software download*)**

### 12.1.1 Application Notes

- **EMI Radiated Immunity *Document Number 146127***
- **Two Layer PCB Design *Document Number 146669***
- **VP-API II Based DTMF Detection *Document Number 154520***

## 12.2 Development Hardware

Contact your sales representative for the latest Le9622 reference design hardware.

- **ZLR962282L Line Module**
  - The *ZLR962282L Line Module* features four Le9622 *miSLIC*™ Line Circuits operating in SPI/PCM mode with Microsemi's Multi-line Inverting Boost topology. The multi-line design uses two independent inverting boost DC/DC converters to create the VBATL (25V) and VBATH (75V) battery supplies. Each supply is optimized for its for best efficiency and cost. The design also uses off the shelf inductors instead of a custom transformer. The supplies are designed to operate from a nominal 12V +/-2V supply.
- **ZLR962282H Line Module**
  - 3 Battery version with external battery switch. VBATL (30V) and VBATM (60V) are off of the VBATL supply. VBATH (90V) is from an independent supply.

## 12.3 Downloads, Firmware and Drivers

- **Le9622 IBIS Model,** available at **www.microsemi.com/voice-line-circuits.**

## 12.4 Development Software

URLs for the following software is available on the Microsemi website **www.microsemi.com/voice-line-circuits.**

- **Le71SK0002 VoicePath API-II Software**
  - The *VP-API-II* is a set of C source used by the host application to interface to the *VE880*, *VE890*, *ZL880, and miSLIC Series* and other Microsemi voice product families.
- **Le71SDKAPIL API-II Lite**
  - The *VP-API-II Lite* is identical to *VP-API-II*, with reduced functionality. *VP-API-II Lite* does not support tone or ringing cadencing, Caller ID, or Metering signal generation.
- **Le71SDKTK Microsemi CMPG Toolkit**
  - The Microsemi CMPG Toolkit application is a scripting environment that allows for the development and distribution of Tcl related collateral for Microsemi CMPG hardware and software products. The Toolkit includes several custom Microsemi CMPG Tcl extension packages, i.e. *VP-Script* and *Mini-PBX*.
  - The *VP-Script* application is intended to provide a robust interactive GUI and scripting environment for each of Microsemi CMPG's currently manufactured Microprocessor Interface (MPI) devices as well as for the next generation Host Bus Interface (HBI) devices.
  - *Mini-PBX* provides an interactive GUI for the *Voice Path API-II* and the *LT-API* libraries, i.e. *VeriVoice* and *LineCare*.
- **Le71SDKPRO Profile Wizard**
  - The *VP Profile Wizard* is a *Microsoft Windows* GUI application that aids in the organization and creation of country *Profiles* used in the *VP-API-II* into a single project file.
- **Le71SDKZTAP ZTAP Support Package**
  - The *ZTAP* is the latest in Microsemi CMPG's hardware platforms designed to provide a demonstration and development vehicle for Microsemi CMPG's voice devices. In standalone mode, it operates as a basic call control environment that will automatically run Microsemi CMPG line modules. When used with Microsemi CMPG Toolkit, devices/lines can be monitored and programmed with user specified parameters. Voice quality measurements can be made in either E1 or T1 mode by connecting standard test equipment to the *ZTAP*.
- **ZL880SLVVP VeriVoice Professional Test Suite**
  - The *VeriVoice™ Professional Test Suite* provides customers with the most cost effective, reliable VoIP line testing tools available on the market. The *VeriVoice Test Suite Software* is used in conjunction with *VoicePath™ API-II and API-II Lite* software to provide line test and self-test for select devices from the miSLIC™ Series and ZL880 VoicePort™ Series. The *VeriVoice™ Professional Test Suite* software is available in C code, allowing for easy integration and customization by a developer.
- **ZLS880VVMT VeriVoice Manufacturing Test Package**
  - The *VeriVoice™ Manufacturing Test Package* is a stand-alone, self contained test package intended to facilitate factory testing of new products based on Microsemi CMPG's *miSLIC™ Series, ZL880 Series, VE880 Series, and VE890 chipsets*. The software is distributed as a portable, platform-independent C source code module. The software is architected as a rapid set of tests which provide thorough test cover. The software eliminates the need for expensive test equipment.
- **LE71SDKWIN WinSLAC™ Software (available in Software Delivery System)**
  - The *WinSLAC™* utility is a software program that aids in the design and development of telephony interfaces and related voice band applications.

# 13.0 Revision History

## 13.1 Revision 2 to Revision 3

- Change Status from Advance to Preliminary
- Added Maximum device junction temperature in 4.1, “Absolute Maximum Ratings“
- Modify thermal constants to align with latest simulations, replace $\theta_{JC\ (BOTTOM)}$ with JEDEC standard $\theta_{JC}$ in 4.1, “Absolute Maximum Ratings“.

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