Ordering Information

Part Number	Temperature Range	Package
MICRF220AYQS	–40°C to +105°C	16-Pin QSOP

Pin Configuration

MICRF220AYQS

Pin Description

Pin Number	Pin Name	Pin Function
1	RO1	Reference resonator connection to the Pierce oscillator. May also be driven by external reference signal of 200mVp-p to 1.5V p-p amplitude maximum. Internal capacitance of 7pF to GND during normal operation.
2	GNDRF	Ground connection for ANT RF input. Connect to PCB ground plane.
3	ANT	Antenna Input: RF Signal Input from Antenna. Internally AC coupled. It is recommended to use a matching network with an inductor-to-RF ground to improve ESD protection.
4	GNDRF	Ground connection for ANT RF input. Connect to PCB ground plane.
5	VDD	Positive supply connection for all chip functions. Bypass with 0.1µF capacitor located as close to the VDD pin as possible.
6	SQ	Squelch Control Logic-Level Input. An internal pull-up (5µA typical) pulls the logic-input HIGH when the device is enabled. A logic LOW on SQ squelches, or reduces, the random activity on DO pin when there is no RF input signal.
7	SEL0	Demodulator Filter Bandwidth Select Logic-Level Input. This pin has an internal pull-up (3µA typical) when the chip is on. Use in conjunction with SEL1 to control demodulation bandwidth.
8	SHDN	Shutdown Control Logic-Level Input. A logic-level LOW enables the device. A logic-level HIGH places the device in low-power shutdown mode. An internal pull-up (5µA typical) pulls the logic input HIGH.
9	GND	Ground connection for all chip functions except for RF input. Connect to PCB ground plane.
10	DO	Data Output. Demodulated data output. A current limited CMOS output during normal operation, 25kΩ pull-down is present when device is in shutdown.
11	SEL1	Demodulator Filter Bandwidth Select Logic-Level Input. This pin has an internal pull-up (3µA typical) when the chip is on. Use in conjunction with SEL0 to Demodulation bandwidth.
12	CTH	Demodulation Threshold Voltage Integration Capacitor. Connect a 0.1µF capacitor from CTH pin-to-GND to provide a stable slicing threshold.
13	CAGC	AGC Filter Capacitor. Connect a capacitor from this pin to GND. Refer to the *AGC Loop and CAGC* section for information on the capacitor value.
14	RSSI	Received Signal Strength Indicator. The voltage on this pin is an inversed amplified version of the voltage on CAGC. Output is from a switched capacitor integrating op amp with 250Ω typical output impedance.
15	NC	No Connect. Leave this pin floating.
16	RO2	Reference resonator connection to the Pierce oscillator. Internal capacitance of 7pF to GND during normal operation.

Electrical Characteristics (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
Demodulator					
CTH Source Impedance, Note 6	f_{REF} = 9.81713MHz		165		kΩ
	f_{REF} = 13.52313MHz		120		
CTH Leakage Current In CTH Hold Mode	T_A = +25ºC T_A = +105ºC		1 10		nA
Digital / Control Functions					
DO Pin Output Current	As output source @ 0.8 V_{DD} As output sink @ 0.2 V_{DD}		300 680		µA
Output Rise Time	15pF load on DO pin, transition time between 0.1xV_{DD} and 0.9xV_{DD}		600		ns
Output Fall Time			200		
Input High Voltage	SHDN, SEL0, SEL1, SQ	0.8V_{DD}			V
Input Low Voltage	SHDN, SEL0, SEL1, SQ			0.2V_{DD}	V
Output Voltage High	DO	0.8V_{DD}			V
Output Voltage Low	DO			0.2V_{DD}	V
RSSI					
RSSI DC Output Voltage Range	–110dBm RF input level		0.5		V
	–50dBm RF input level		2.0		
RSSI Output Current	5kΩ load to GND, –50dBm RF input level		400		µA
RSSI Output Impedance			250		Ω
RSSI Response Time	V_{SEL0} = V_{SEL1} = 0V, RF input power stepped from no input to –50dBm		10		ms

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside of its operating rating.
3. Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.
4. Encoded bit rate is 1/(shortest pulse duration) that appears at MICRF220 DO pin.
5. In an ON/OFF keyed (OOK) signal, the signal level goes between a “mark” level (when the RF signal is ON) and a “space” level (when the RF signal is OFF). Sensitivity is defined as the input signal level when “ON” necessary to achieve a specified BER (bit error rate). BER measured with the built-in BERT function in Agilent E4432B using the PN9 sequence. Sensitivity measurement values are obtained using an input matching network corresponding to 315MHz or 433.92MHz.
6. CTH source impedance is inversely proportional to the reference frequency. In production testing, the typical source impedance value is verified with 12MHz reference frequency.

Functional Diagram

Figure 1. Simplified Block Diagram

Functional Description

The simplified block diagram (Figure 1) illustrates the basic structure of the MICRF220 receiver. It is made up of four sub-blocks:

- UHF Down-Converter
- ASK/OOK Demodulator
- Reference and Control logic
- Squelch Control

Outside the device, the MICRF220 receiver requires just a few components to operate: a capacitor from CAGC to GND, a capacitor from CTH-to-GND, a reference crystal resonator with associated loading capacitors, LNA input matching components, and a power-supply decoupling capacitor.

Receiver Operation

UHF Downconverter

The UHF down-converter has six sub-blocks: LNA, mixers, synthesizer, image reject filter, band pass filter and IF amplifier.

LNA

The RF input signal is AC-coupled into the gate of the LNA input device. The LNA configuration is a cascoded common source NMOS amplifier. The amplified RF signal is then fed to the RF ports of two double balanced mixers.

Mixers and Synthesizer

The LO ports of the mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal (Figure 2). The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will be demodulated by the detector of the device. The image reject mixer suppresses the image frequency which is below the wanted signal by two times the IF frequency. The local oscillator frequency (f_{LO}) is set to 32 times the crystal reference frequency (f_{REF}) via a phase-locked loop synthesizer with a fully-integrated loop filter:

$$f_{LO} = 32 \times f_{REF} \quad \text{Eq. 1}$$

MICRF220 uses an IF frequency scheme that scales the IF frequency (f_{IF}) with f_{REF} according to:

$$f_{IF} = f_{REF} \times \frac{87}{1000} \quad \text{Eq. 2}$$

Therefore, the reference frequency f_{REF} needed for a given desired RF frequency (f_{RF}) is approximately:

$$f_{REF} = f_{RF} / \left(32 + \frac{87}{1000}\right) \quad \text{Eq. 3}$$

Figure 2. Low-Side Injection Local Oscillator

Image-Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature-down converted IF signals. These IF signals are low-pass filtered to remove higher-frequency products prior to the image reject filter where they are combined to reject the image frequency. The IF signal then passes through a third order band pass filter. The IF bandwidth is 330kHz @ 433.92MHz, and will scale with RF operating frequency according to:

$$BW_{IF} = BW_{IF@433.92\ MHz} \times \left(\frac{\text{Operating Freq (MHz)}}{433.92}\right) \quad \text{Eq. 4}$$

These filters are fully integrated inside the MICRF220.

After filtering, four active gain controlled amplifier stages enhance the IF signal to its proper level for demodulation.

ASK/OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

The value of CAGC impacts the time to good data (TTGD), which is defined as the time when signal is first applied, to when the pulse width at DO is within 10% of the steady state value. The optimal value of CAGC depends upon the setting of the SEL0 and SEL1 pins. A smaller CAGC value does NOT always result in a shorter TTGD. This is due to the loop dynamics, the fast discharge current being 600µA, and the charge current being only 1.5µA. For example, if $V_{SEL0} = V_{SEL1} = 0V$, the low pass filter bandwidth is set to a minimum and CAGC capacitance is too small, TTGD will be longer than if CAGC capacitance is properly chosen. This is because when RF signal first appears, the fast discharge period will reduce V_{CAGC} very fast, lowering the gain of the mixer and IF amplifier. But since the low pass filter bandwidth is low, it takes too long for the AGC comparator to see a reduced level of the audio signal, so it can not stop the discharge current. This causes an undershoot in CAGC voltage and a corresponding overshoot in RSSI voltage. Once CAGC undershoots, it takes a long time for it to charge back up because the current available is only 1.5µA.

Table 3 lists the recommended CAGC values for different SEL0 and SEL1 settings.

V_{SEL1}	V_{SEL0}	CAGC value
0V	0V	4.7µF
0V	V_{DD}	2.2µF
V_{DD}	0V	1µF
V_{DD}	V_{DD}	0.47µF

Table 3. Minimum Suggested CAGC Values

Figure 3 illustrates what occurs if CAGC capacitance is too small for a given SEL1, SEL0 setting. Here, $V_{SEL1} = 0V$, $V_{SEL0} = V_{DD}$, the capacitance on CAGC pin is 0.47µF, and the RF input level is stepped from no signal to –100dBm. RSSI voltage is shown instead of CAGC voltage because RSSI is a buffered version of CAGC (with an inversion and amplification). Probing CAGC directly can affect the loop dynamics through resistive loading from a scope probe, especially in the state where only 1.5µA is available, whereas probing RSSI does not. When RF signal is first applied, RSSI voltage overshoots due to the fast discharge current on CAGC, and the loop is too slow to stop this fast discharge current in time. Since the voltage on CAGC is too low, the audio signal level is lower than the slicing threshold (voltage on CTH), and DO pin is low. Once the fast discharge current stops, only the small 1.5µA charge current is available in settling the AGC loop to the correct level, causing the recovery from CAGC undershoot/RSSI overshoot condition to be slow. As a result, TTGD is about 9.1ms.

Figure 3. RSSI Overshoot and Slow TTGD (9.1ms)

Figure 4 shows the behavior with a larger capacitor on CAGC pin (2.2µF), $V_{SEL1} = 0V$, and $V_{SEL0} = V_{DD}$. In this case, V_{CAGC} does not undershoot (RSSI does not overshoot), and TTGD is relatively short at 1ms.

Figure 4. Proper TTGD (1ms) with Sufficient CAGC

Reference Oscillator

The reference oscillator in the MICRF220 (Figure 5) uses a basic Pierce crystal oscillator configuration with MOS transconductor to provide negative resistance. Though the MICRF220 has built-in load capacitors for the crystal oscillator, the external load capacitors are still required for tuning it to the right frequency. RO1 and RO2 are external pins of the MICRF220 to connect the crystal to the reference oscillator.

Application Information

Figure 8. MICRF220 EV Board Application Example

Supply Voltage Ramping

When supply voltage is initially applied, it should rise monotonically from 0V to 3.3V to ensure proper startup of the crystal oscillator and the PLL. It should not have multiple bounces across 2.6V, which is the threshold of the undervoltage lockout (UVLO) circuit inside MICRF220.

Antenna and RF Port Connections

Figure 8 shows the schematic of the MICRF220 Evaluation Board. Figures 9 thru 11 depict PCB images. This evaluation board is a good starting point for the prototyping of most applications. The evaluation board offers two options of injecting the RF input signal: through a PCB antenna or through a 50Ω SMA connector. The SMA connection allows for conductive testing, or an external antenna.

Low-Noise Amplifier Input Matching

Capacitor C3 and inductor L2 form the "L" shape input matching network to the SMA connector. The capacitor cancels out the inductive portion of the net impedance after the shunt inductor, and provides additional attenuation for low-frequency outside band noise. The inductor is chosen to over resonate the net capacitance at the pin, leaving a net-positive reactance and increasing the real part of the impedance. It also provides additional ESD protection for the antenna pin. The input impedance of the device is listed in Table 6 to aid calculation of matching values. Note that the net impedance at the pin is easily affected by component pads parasitic due to the high input impedance of the device. The numbers in Table 6 does NOT include trace and component pad parasitic capacitance, which total about 0.75pF on the evaluation board.

The matching components to the PCB antenna (L3 and C9) were empirically derived for best over-the-air reception range.

Frequency (MHz)	Z Device (Ω)
315	23 – j290
390	14 – j230
418	17 – j216
433.92	12 – j209

Table 6. Input Impedance for the Most Used Frequencies

Crystal Selection

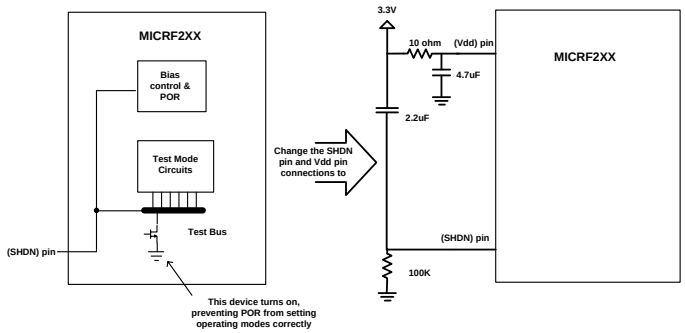
The crystal resonator provides a reference clock for all the device internal circuits. Crystal tolerance needs to be chosen such that the down-converted signal is always inside the IF bandwidth of MICRF220. From this consideration, the tolerance should be ±50ppm on both the transmitter and the MICRF220 side. ESR should be less than 300Ω, and the temperature range of the crystal should match the range required by the application. With the Abracon crystal listed in the Bill of Materials, a typical MICRF220 crystal oscillator still starts up at 105ºC with additional 400Ω series resistance.

The oscillator of the MICRF220 is a Pierce-type oscillator. Good care must be taken when laying out the printed circuit board. Avoid long traces and place the ground plane on the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and the crystals used are not verified, the oscillator may not start or takes longer to start. Time-to-good-data will be longer as well.

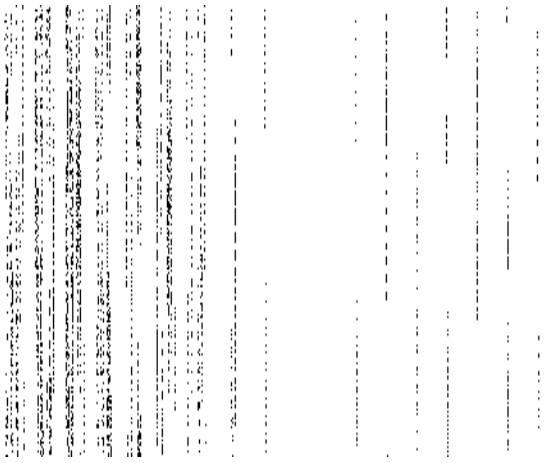
Important Note

A few customers have reported that some MICRF220eceiver do not start up correctly. When the issue occurs, DO either chatters or stays at low voltage level. An unusual operating current is observed and the part cannot receive or demodulate data even when a strong OOK signal is present.

Micrel has confirmed that this is the symptom of incorrect power on reset (POR) of internal register bits. The MICRF220 is designed to start up in shutdown mode (SHDN pin must be in logic high during Vdd ramp up). When the SHDN pin is tied to GND, and if the supply is ramped up slowly, a "test bus pull down" circuit may be activated. Once the chip enters this mode, the POR does not have the chance to set register bits (and hence operating modes) correctly. The test bus pull down acts on the SHDN pin, and can be illustrated in the following diagram.



To prevent the erroneous startup, a simple RC network is recommended. The 10Ω resistor and the 4.7µF capacitor provide a delay of about 200µs between VDD and SHDN during the power up, thus ensuring the part enters shutdown stage before the part is actually turned on. The 2.2µF capacitor bootstraps the voltage on SHDN, ensuring that SHDN voltage leads the supply voltage on VDD during power up. This gives the POR circuit time to set internal register bits. The SHDN pin can be brought low to turn the chip on once the initialization is completed. The 2.2µF and 100kΩ network form an RC delay of about 200ms before the SHDN pin is brought to low again. The 100kΩ resistor discharges the SHDN pin to turn the chip on.

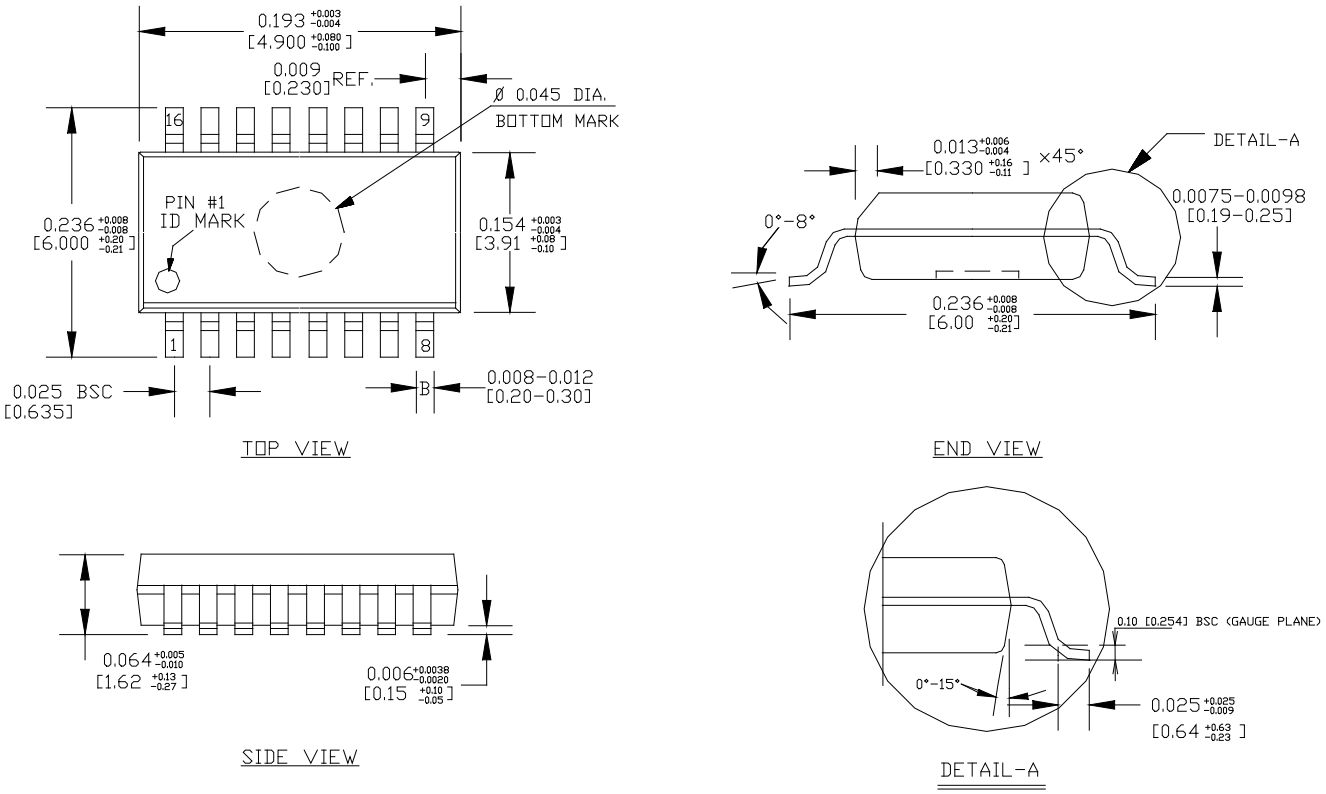


The suggestion provided above will generally serve to prevent the startup issue from happening to the MICRF220 series ASK receiver. However, exact values of the RC network depend on the ramp rate of the supply voltage, and should be determined on a case-by-case basis.

PCB Considerations and Layout

Figures 9 thru 11 illustrate the MICRF220 Evaluation Board layout. The Gerber files provided are downloadable from the Micrel website and contain the remaining layers needed to fabricate this board. When copying or making one's own boards, make the traces as short as possible. Long traces alter the matching network and the values suggested are no longer valid. Suggested matching values may vary due to PCB variations. A PCB trace 100 mils (2.5mm) long has about 1.1nH inductance. Optimization should always be done with exhaustive range tests. Make sure the individual ground connection has a dedicated via rather then sharing a few of ground points by a single via. Sharing ground via will increase the ground path inductance. Ground plane should be solid and with no sudden interruptions. Avoid using ground plane on top layer next to the matching elements. It normally adds additional stray capacitance which changes the matching. Do not use Phenolic materials as they are conductive above 200MHz. Typically, FR4 or better materials are recommended. The RF path should be as straight as possible to avoid loops and unnecessary turns. Separate ground and V_{DD} lines from other digital or switching power circuits (such microcontroller…etc). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid unnecessary wide traces which would add more distribution capacitance (between top trace to bottom GND plane) and alter the RF parameters.

Package Information and Recommended Land Pattern[1]



NOTE:
1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

QSOP16 Package Type (AQS16)

Note:

9. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

单击下面可查看定价，库存，交付和生命周期等信息

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