MIC33050

4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load®

Features

- Input Voltage: 2.7V to 5.5V
- 600 mA Output Current
- Fixed and Adjustable Output Voltage Options
- No External Inductor Required
- Ultra-Fast Transient Response
- 20 µA Quiescent Current
- 4 MHz Switching in PWM Mode
- Low Output Voltage Ripple
- >93% Peak Efficiency
- >85% Efficiency at 1 mA
- Micropower Shutdown
- 12-Pin 3 mm x 3 mm HDFN
- –40°C to +125°C Junction Temperature Range

Applications

- MPU Power
- Portable Instrumentation
- Wearable Devices
- Space-Constrained MCU Systems
- RF Modules
- USB-Powered Devices

General Description

The MIC33050 is a high-efficiency 600 mA PWM synchronous buck (step-down) regulator with internal inductor featuring HyperLight Load®, a switching scheme that offers best-in-class light load efficiency and transient performance while providing very small external components and low output ripple at all loads.

The MIC33050 also has a very low typical quiescent current of 20 µA and can achieve over 85% efficiency even at 1 mA.

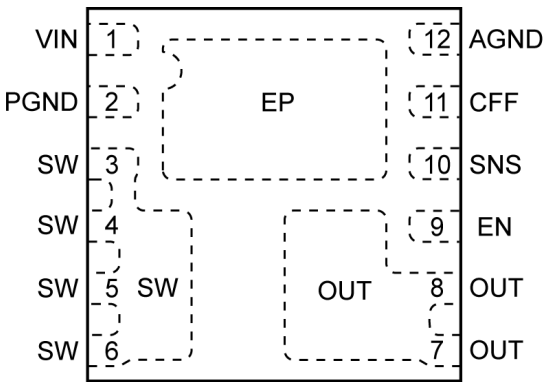
In contrast to traditional light load schemes, the HyperLight Load® architecture does not trade off control speed to obtain low standby currents and in doing so, the device only needs a small output capacitor to absorb the load transient as the powered device goes from light load to full load.

At higher loads, the MIC33050 provides a nearly constant switching frequency of greater than 4 MHz while providing peak efficiencies greater than 93%.

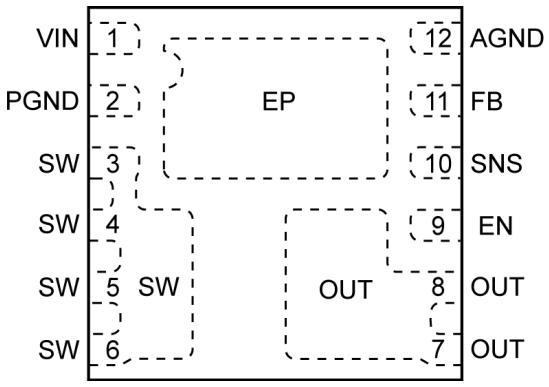
The MIC33050 is available in fixed and adjustable output voltages and comes in a 12-pin 3 mm x 3 mm HDFN with a operating junction temperature range of –40°C to +125°C.

Package Types

12-Pin 3 mm x 3 mm HDFN
Fixed (Top View)



12-Pin 3 mm x 3 mm HDFN
Adjustable (Top View)



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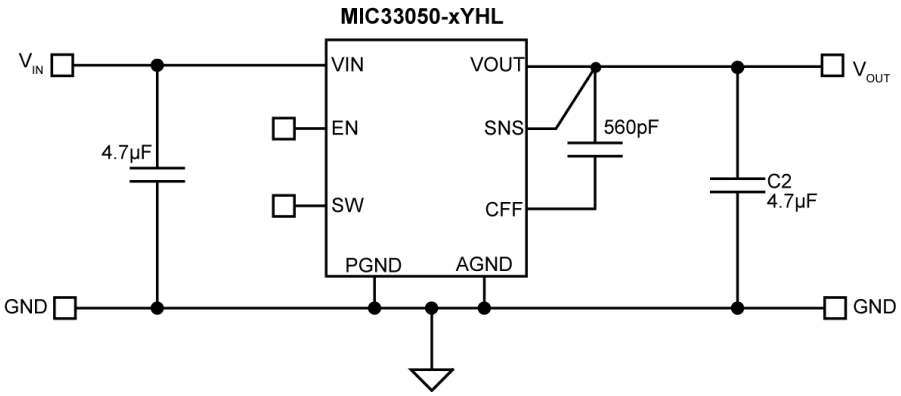
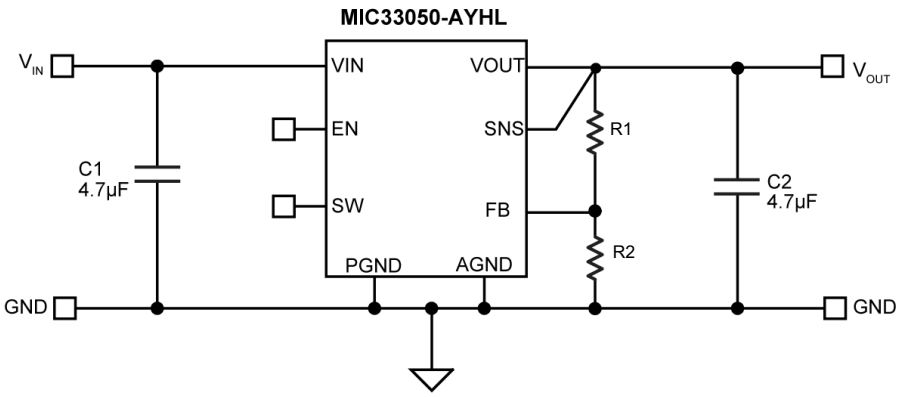
Typical Application Circuits

Fixed Output MIC33050



Adjustable Output MIC33050



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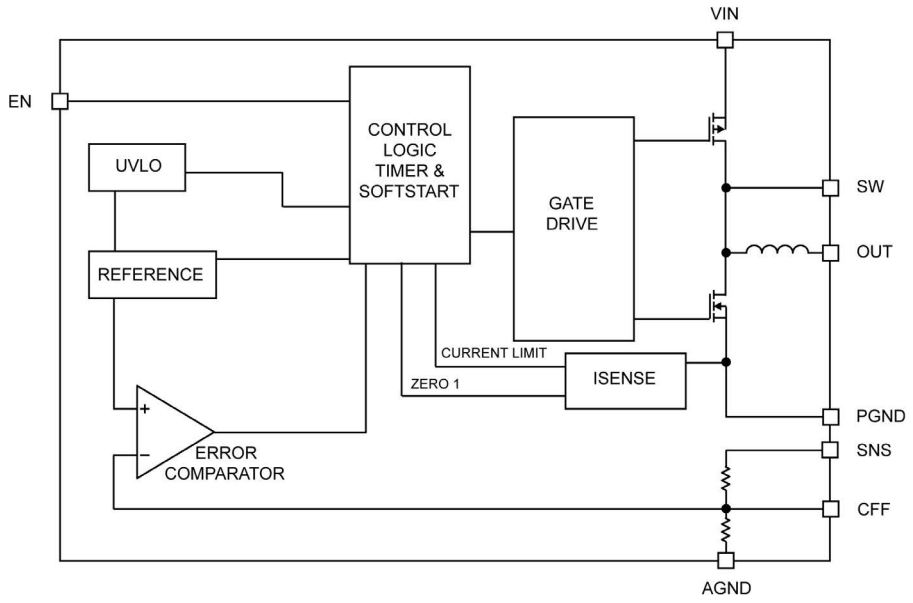
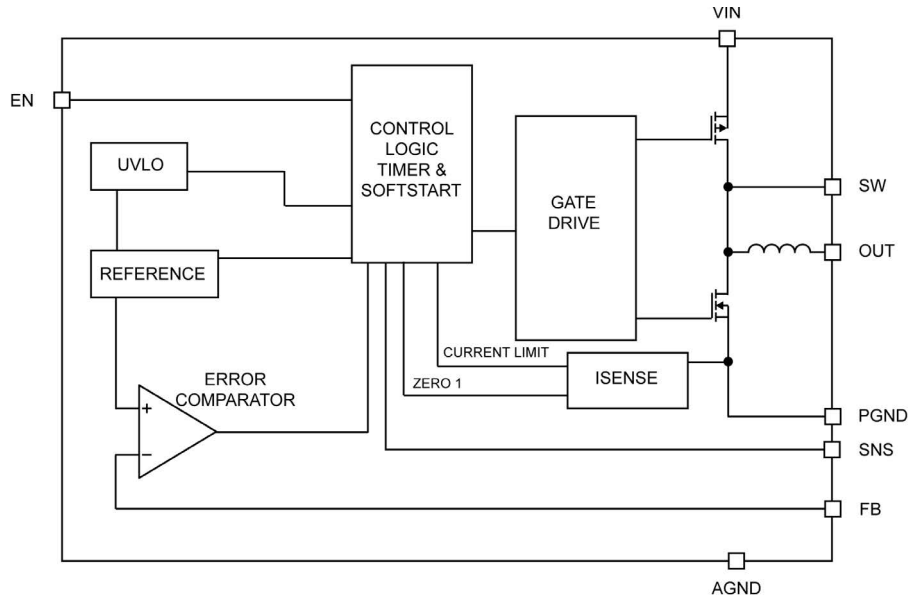
Functional Block Diagrams

Simplified MIC33050 Fixed Functional Block Diagram



Simplified MIC33050 Adjustable Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}).....+6V
Output Switch Voltage (V_{SW}).....+6V
Output Switch Current (I_{SW}).....2A
Logic Enable Input Voltage (V_{EN})..... –0.3V to V_{IN}
ESD Rating (Note 1)..... ESD Sensitive

Operating Ratings ‡

Supply Voltage (V_{IN})..... +2.7V to +5.5V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = 25°C, V_{IN} = V_{EN} = 3.6V; C_{FF} = 560 pF; C_{OUT} = 4.7µF; I_{OUT} = 20 mA unless otherwise specified. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. Specification for packaged product only.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	V_{IN}	2.7	—	5.5	V	—
Undervoltage Lockout Threshold	UVLO	2.45	2.55	2.65	V	Turn-On
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	—	100	—	mV	—
Quiescent Current	I_Q	—	20	**32**	µA	I_{OUT} = 0 mA, SNS > 1.2 * $V_{OUT(NOM)}$
Shutdown Current	I_{SHDN}	—	0.01	**4**	µA	V_{EN} = 0V; V_{IN} = 5.5V
Output Voltage Accuracy	ΔV_{OUT}	**–2.5**	—	**+2.5**	%	V_{IN} = 3.0V; I_{LOAD} = 20 mA
Current Limit in PWM Mode	I_{LIM}	**0.65**	1	**1.7**	A	V_{SNS} = 0.9*$V_{OUT(NOM)}$
Output Voltage Line Regulation	ΔV_{O_LINE}	—	0.5	—	%/V	V_{IN} = 3.0V to 5.5V, I_{LOAD} = 20 mA
Output Voltage Load Regulation	ΔV_{O_LOAD}	—	0.3	—	%	20 mA < I_{LOAD} < 500 mA
Feedback Voltage	V_{FB}	**390**	400	**410**	mV	V_{IN} = 3.0V; I_{OUT} = 20 mA
Maximum Duty Cycle	D_{MAX}	**80**	89	—	%	V_{SNS} ≤ $V_{OUT(NOM)}$
PWM Switch On-Resistance	$R_{DS(ON)P}$	—	0.45	—	Ω	I_{SW} = 100 mA PMOS
	$R_{DS(ON)N}$	—	0.5	—		I_{SW} = –100 mA NMOS
Switching Frequency	f_{SW}	—	4	—	MHz	I_{OUT} = 120 mA
Soft Start Time	t_{SS}	—	650	—	µs	V_{OUT} = 90% of $V_{OUT(NOM)}$
Enable Threshold	V_{ENTH}	**0.5**	0.8	**1.2**	V	Turn-On
Enable Hysteresis	V_{ENHYS}	—	35	—	mV	—
Enable Input Current	I_{EN}	—	0.1	**2**	µA	—
Overtemperature Shutdown	T_{SD}	—	165	—	°C	—
Overtemperature Shutdown Hysteresis	T_{SDHYS}	—	20	—	°C	—

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance 12-Pin HDFN 3 mm x 3 mm	θ_{JA}	—	60	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

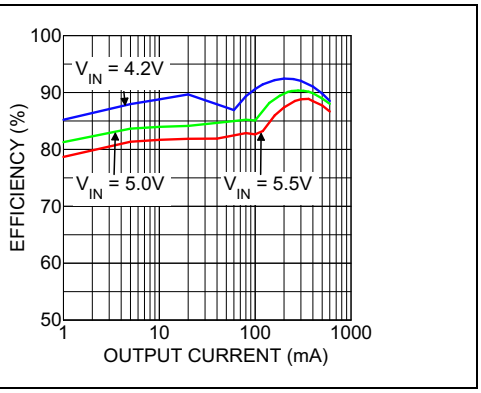

FIGURE 2-1: *Efficiency (V_{OUT} = 3.3V).*

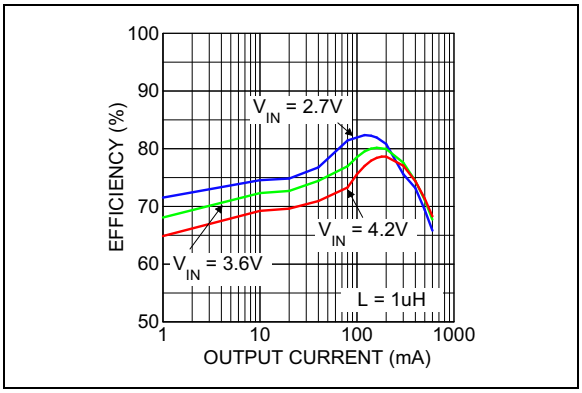

FIGURE 2-4: *Efficiency (V_{OUT} = 1.0V).*

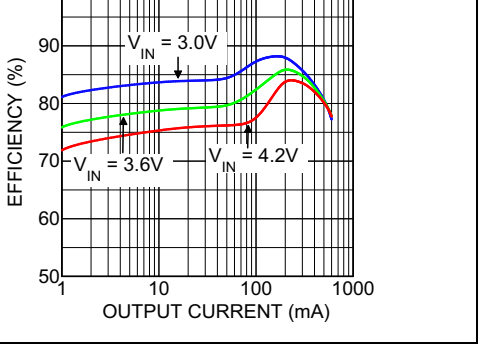

FIGURE 2-2: *Efficiency (V_{OUT} = 1.8V).*

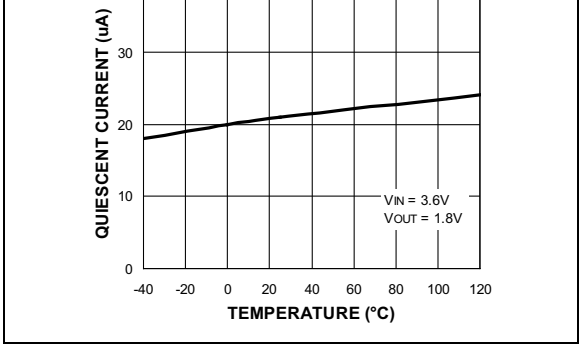

FIGURE 2-5: *Quiescent Current vs. Temperature.*

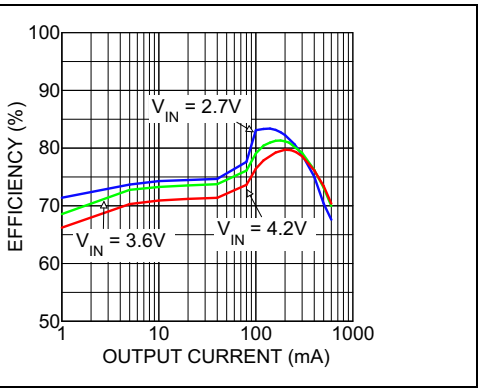

FIGURE 2-3: *Efficiency (V_{OUT} = 1.2V).*

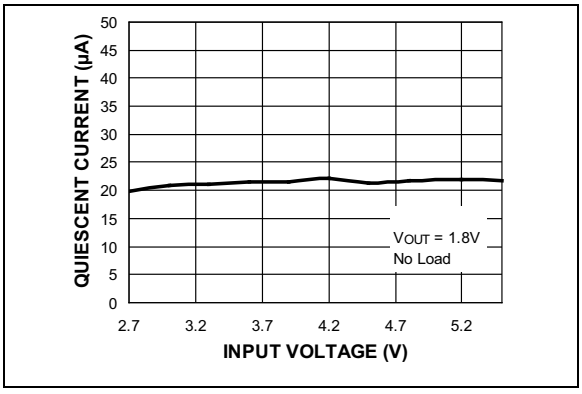

FIGURE 2-6: *Quiescent Current vs. Input Voltage.*

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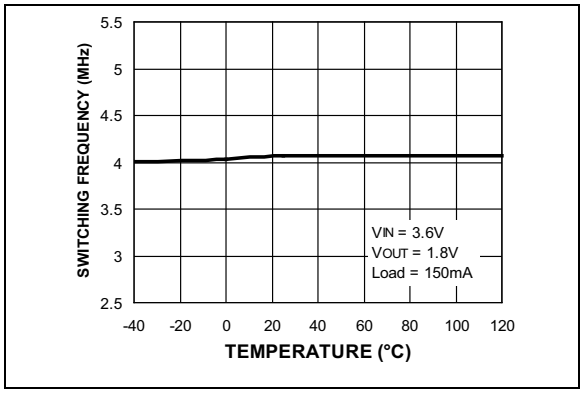

FIGURE 2-7: *Switching Frequency vs. Temperature.*

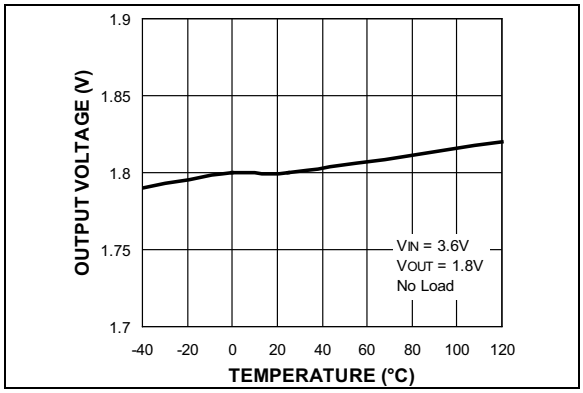

FIGURE 2-10: *Output Voltage vs. Temperature.*

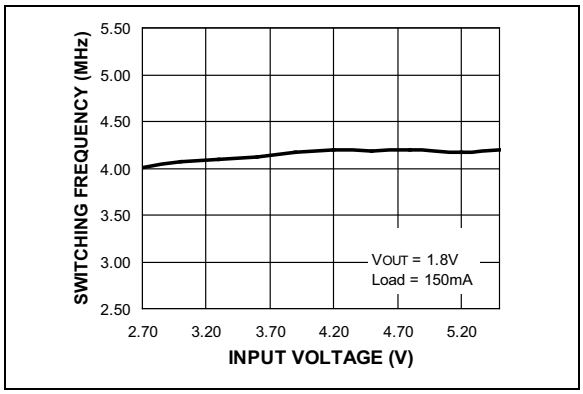

FIGURE 2-8: *Switching Frequency vs. Input Voltage.*

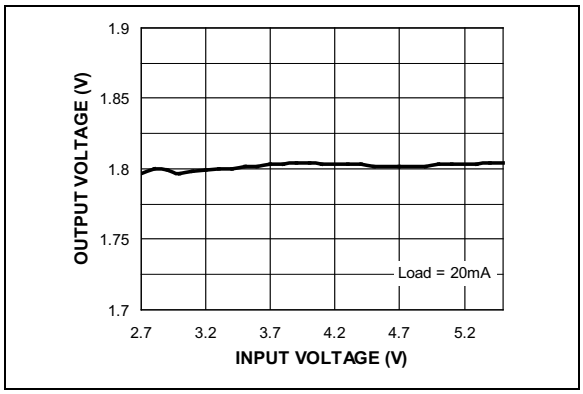

FIGURE 2-11: *Output Voltage vs. Input Voltage.*

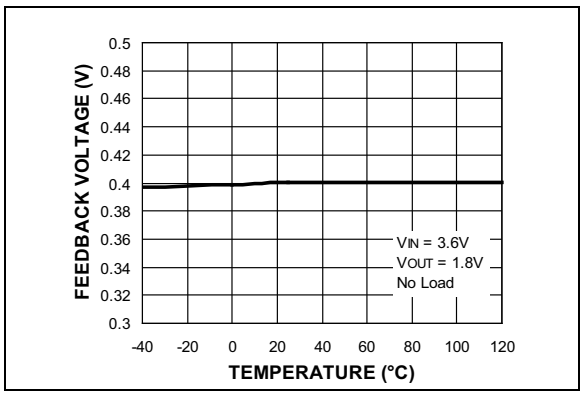

FIGURE 2-9: *Feedback Voltage vs. Temperature.*

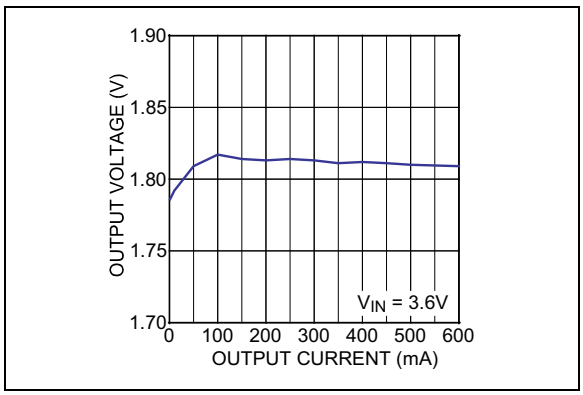

FIGURE 2-12: *Output Voltage vs. Output Current.*

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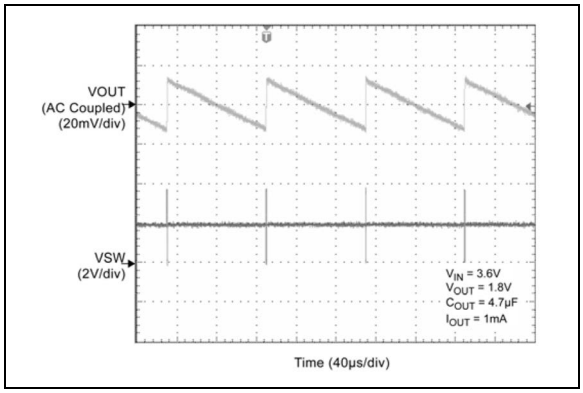

FIGURE 2-13: *Switching Waveforms, (I_{OUT} = 1 mA).*

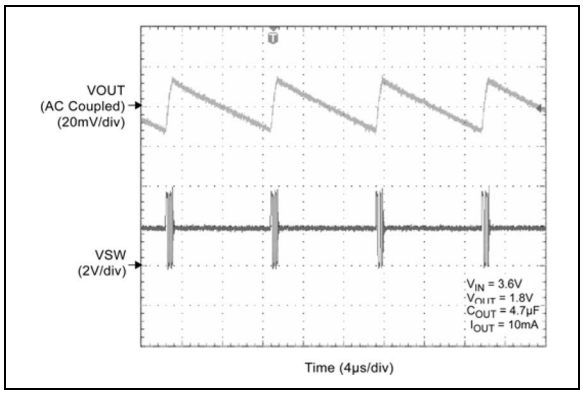

FIGURE 2-14: *Switching Waveforms, (I_{OUT} = 10 mA).*

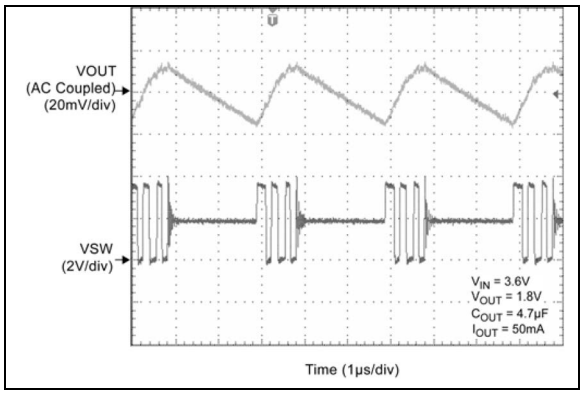

FIGURE 2-15: *Switching Waveforms, (I_{OUT} = 50 mA).*

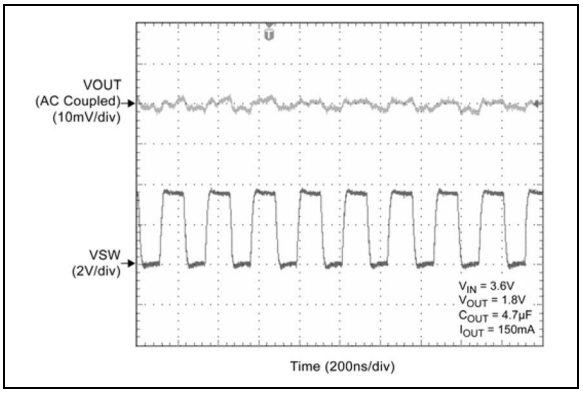

FIGURE 2-16: *Switching Waveforms, (I_{OUT} = 150 mA).*

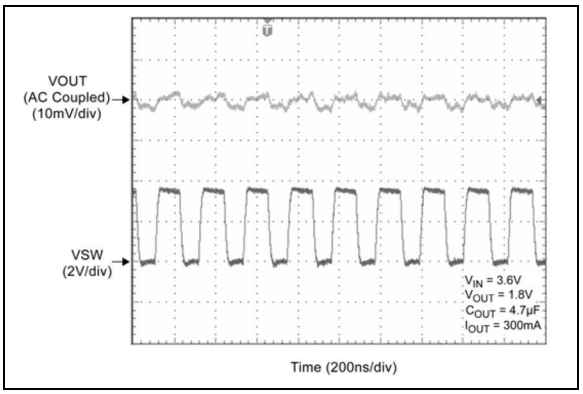

FIGURE 2-17: *Switching Waveforms, (I_{OUT} = 300 mA).*

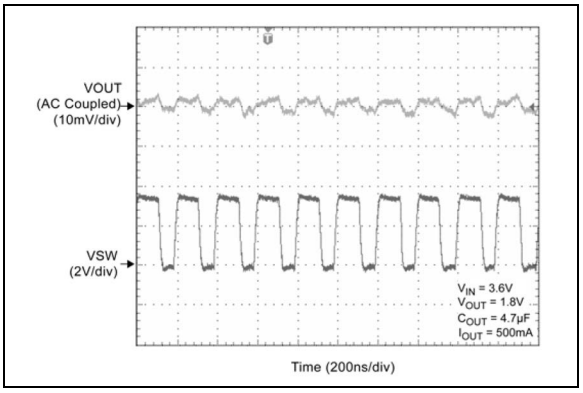

FIGURE 2-18: *Switching Waveforms, (I_{OUT} = 500 mA).*

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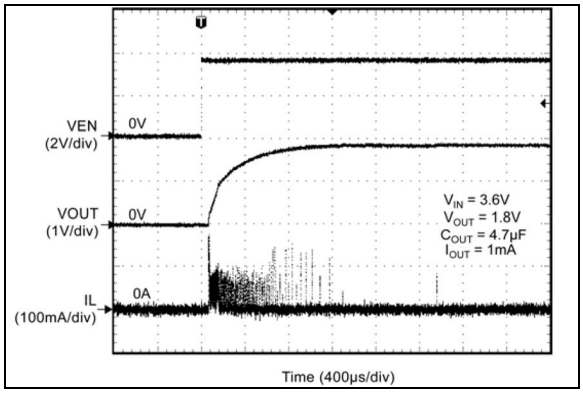

FIGURE 2-19: *Start-Up, (I_{OUT} = 1 mA).*

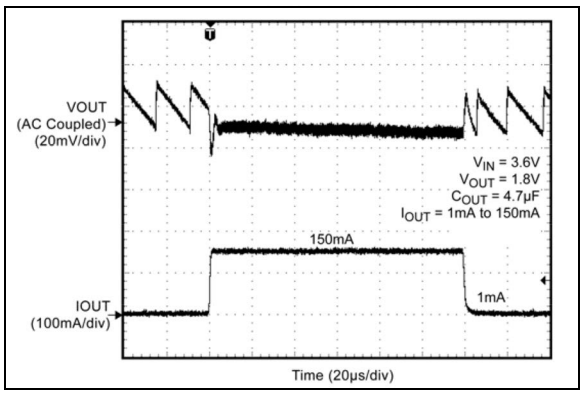

FIGURE 2-20: *Load Transient, (1 mA to 150 mA).*

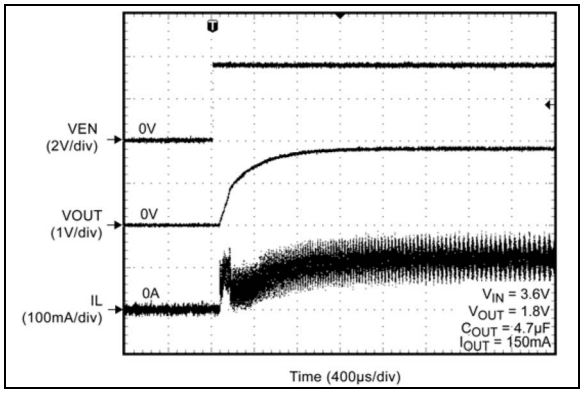

FIGURE 2-21: *Start-Up, (I_{OUT} = 150 mA).*

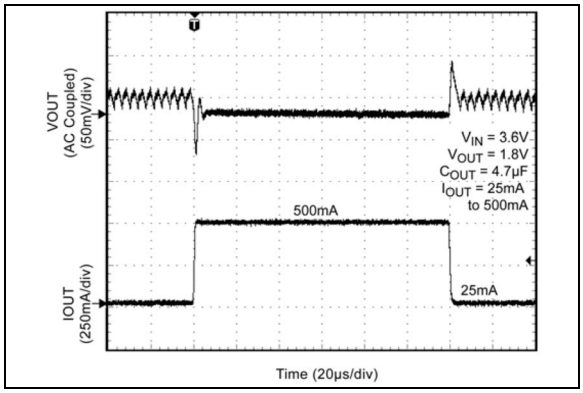

FIGURE 2-22: *Load Transient, (25 mA to 500 mA).*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number MIC33050 (Fixed Option)	Pin Number MIC33050 (Adj. Option)	Pin Name	Description
1	1	VIN	Supply Voltage (Input): Requires bypass capacitor to GND.
2	2	PGND	Power Ground.
3, 4, 5, 6	3, 4, 5, 6	SW	Switch (Output): Internal power MOSFET output switches.
7, 8	7, 8	OUT	Output after the internal inductor.
9	9	EN	Enable (Input): Logic low will shut down the device, reducing the quiescent current to less than 4 µA. Do not leave floating.
10	10	SNS	Input to the error amplifier. Connect to the external resistor divider network to see the output voltage. For fixed output voltages connect V_{OUT} (internal resistor network sets the output voltage).
11	—	CFF	Feed forward capacitor connected to out sense pin.
—	11	FB	Feedback voltage. Connect a resistor divider from output to ground to set the output voltage.
12	12	AGND	Analog ground.
ePAD	ePAD	ePAD	Exposed Heatsink Pad. Connect to power ground for best thermal performance.

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4.0 FUNCTIONAL DESCRIPTION

4.1 VIN

VIN provides power to the MOSFETs for the switch mode regulator section and to the analog supply circuitry. Due to the high switching speeds, it is recommended that a 2.2 µF or greater capacitor be placed close to VIN and the power ground (PGND) pin for bypassing.

4.2 EN

The enable pin, EN, controls the on and off state of the device. A high logic on the enable pin activates the regulator while a low logic deactivates it. MIC33050 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start-up. Do not leave floating.

4.3 SW

The pins at the switch node, SW, are connected directly to the internal inductor. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes such as the CFF and FB pins.

4.4 OUT

The OUT pin is for the output voltage following the internal inductor of the device. Connect an output filter capacitor equal to 2.2 µF or greater to this pin.

4.5 SNS

The sense pin, SNS, is needed to sense the output voltage at the output filter capacitor. In order for the control loop to monitor the output voltage accurately it is good practice to sense the output voltage at the positive side of the output filter capacitor where voltage ripple is smallest.

4.6 CFF

The CFF pin is connected to the SNS pin of MIC33050 with a feed-forward capacitor of 560 pF. The CFF pin itself is compared with the internal reference voltage (V_{REF}) of the device and provides the control path to control the output. V_{REF} is equal to 400 mV. The CFF pin is sensitive to noise and should be place away from the SW pin.

4.7 FB

The feedback pin is provided for the adjustable output version. An external resistor divider network is connected from the output and is compared to the internal 400 mV internal reference voltage within the control loop.

The output voltage, of the circuit in Figure 4-1, may be calculated via the equation below:

EQUATION 4-1:

$$V_{OUT} = 0.4V\left(1 + \frac{R1}{R2}\right)$$

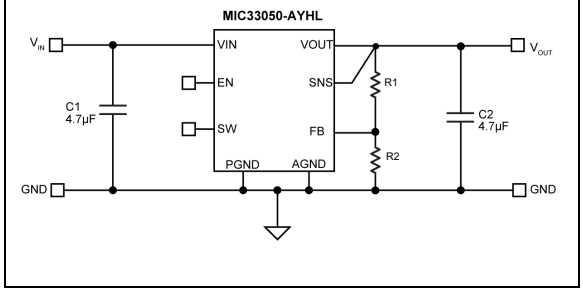

FIGURE 4-1: *MIC33050-AYHL Application Schematic.*

4.8 PGND

Power ground (PGND) is the ground path for high current. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop.

4.9 AGND

Signal ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the PGND loop.

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5.0 APPLICATIONS INFORMATION

5.1 Input Capacitor

A minimum of 2.2 µF ceramic capacitor should be placed close to the VIN pin and PGND pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

5.2 Output Capacitor

The MIC33050 was designed for use with a 2.2 µF or greater ceramic output capacitor. A low equivalent series resistance (ESR) ceramic output capacitor either X7R or X5R is recommended. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies.

5.3 Compensation

The MIC33050 is designed to be stable with an internal inductor with a minimum of 2.2 µF ceramic (X5R) output capacitor.

5.4 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

EQUATION 5-1:

$$\eta = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time which is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET $R_{DS(ON)}$ multiplied by the switch current squared. During the off cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required driving the gates on and off at a constant 4 MHz frequency and the switching transitions make up the switching losses.

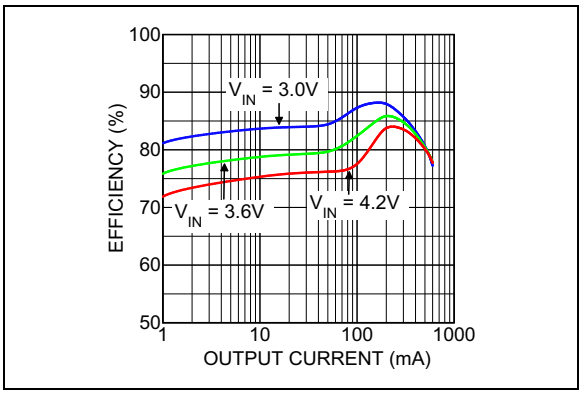

FIGURE 5-1: *Efficiency under Load.*

Figure 5-1 shows an efficiency curve. From 1 µA to 100 mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load® mode, the MIC33050 is able to maintain high efficiency at low output currents.

Over 100 mA, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor losses. Higher input supply voltages will increase the gate to source threshold on the internal MOSFETs, thereby reducing the internal $R_{DS(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant.

The DCR losses can be calculated by using Equation 5-2:

EQUATION 5-2:

$$P_{D(L)} \approx I_{OUT}^{2} \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated by using Equation 5-3:

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EQUATION 5-3:

$$EfficiencyLoss = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + P_{D(L)}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

5.5 HyperLight Load® Mode

The MIC33050 uses a minimum on and off time proprietary control loop. When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum on-time. When the output voltage is over the regulation threshold, the error comparator turns the PMOS off for a minimum off-time. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, MIC33050 works in pulse frequency modulation (PFM) to regulate the output. As the output current increases, the switching frequency increases. This improves the efficiency of the MIC33050 during light load currents. As the load current increases, the MIC33050 goes into continuous conduction mode (CCM) at a constant frequency of 4 MHz. The equation to calculate the load when the MIC33050 goes into continuous conduction mode may be approximated by the following Equation 5-4:

EQUATION 5-4:

$$I_{LOAD} = \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f}\right)$$

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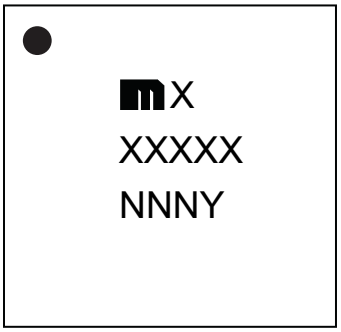
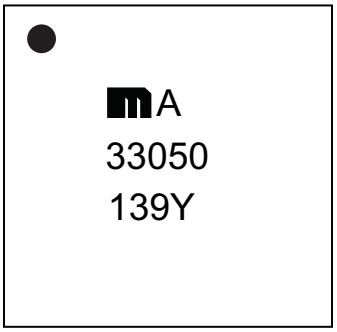
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

12-Lead HDFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

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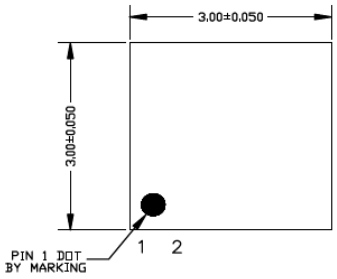
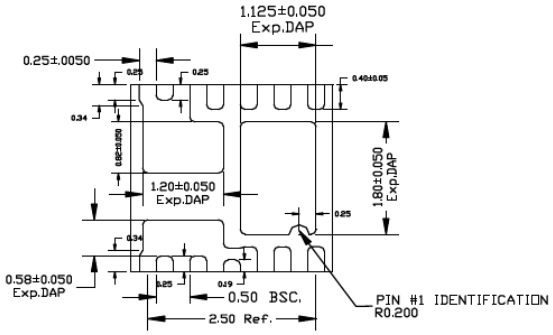
12-Lead HDFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

TITLE
12 LEAD HDFN 3x3 mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

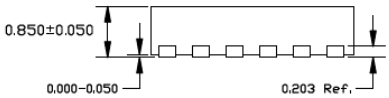
DRAWING #	HDFN33-12LD-PL-1	UNIT	MM



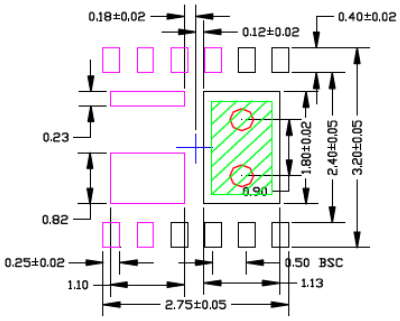
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5, 6

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30-0.35MM AND SHOULD BE CONNECTED TO GND FOR MAXIMUM PERFORMANCE
5. GREEN RECTANGLE REPRESENTS (OPTIONAL) SOLDER STENCIL OPENING. RECOMMENDED SIZE IS 0.90X1.50 MM.
6. PURPLE PADS REPRESENT DIFFERENT POTENTIAL. DO NOT CONNECT TO GND.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (November 2018)

- Converted Micrel document MIC33050 to Microchip data sheet DS20006120B.
- Minor text changes throughout.
- Deleted bullet: Up to 8 MHz PWM Operation in Continuous Mode from the Features, Updated Applications, removed the word patent-pending from General Description, Revised Figure 2-6 and Figure 2-8.

Revision B (March 2022)

- Corrected package marking drawings and added note below legend in Section 6.1, Package Marking Information.
- Minor formatting corrections throughout.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	-X	X	XX	–XX
Device	Output Voltage	Junction Temperature Range	Package Option	Media Type

Device:	MIC33050: 4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load	
Output Voltage:	C = 1.0V 4 = 1.2V G = 1.8V S = 3.3V A = Adjustable	
Junction Temperature Range:	Y =	–40°C to +125°C (Pb-Free, RoHS Compliant)
Package:	HL =	12-Lead 3 mm x 3 mm x 0.9 mm HDFN
Media Type:	T5 = TR =	500/Reel 5000/Reel

Note: Other output voltage options are available. Contact Factory for details.

Examples:

a) MIC33050-4YHL-TR: 4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load®, 1.2V Fixed Output Voltage, –40°C to +125°C Junction Temperature Range, Pb-Free, RoHS Compliant, 12-Lead HDFN Package, 5000/Reel

b) MIC33050-GYHL-TR: 4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load®, 1.8V Fixed Output Voltage, –40°C to +125°C Junction Temperature Range, Pb-Free, RoHS Compliant, 12-Lead HDFN Package, 5000/Reel

c) MIC33050-SYHL-TR: 4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load®, 3.3V Fixed Output Voltage, –40°C to +125°C Junction Temperature Range, Pb-Free, RoHS Compliant, 12-Lead HDFN Package, 5000/Reel

d) MIC33030-AYHL-T5: 4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load®, Adjustable Output Voltage, –40°C to +125°C Junction Temperature Range, Pb-Free, RoHS Compliant, 12-Lead HDFN Package, 500/Reel

e) MIC33030-AYHL-TR: 4 MHz Internal Inductor PWM Buck Power Module with HyperLight Load®, Adjustable Output Voltage, –40°C to +125°C Junction Temperature Range, Pb-Free, RoHS Compliant, 12-Lead HDFN Package, 5000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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