EMC2301/2/3/5

Single/Multiple RPM-Based PWM Fan Controller

Features

- Up To Five Programmable Fan Control Circuits:
  - 4-wire fan compatible
  - High-speed PWM (26 kHz)
  - Low-speed PWM (9.5 Hz-2240 Hz)
  - Optional detection of aging fans
  - Fan Spin Up Control and Ramp Rate Control
  - Alert on Fan Stall
  - Up to three selectable default fan speeds for the EMC2303/5
- Watchdog Timer
- RPM-Based Fan Control Algorithm:
  - 0.5% accuracy from 500 RPM to 16k RPM (external crystal oscillator)
  - 1% accuracy from 500 RPM to 16k RPM (internal clock)
- SMBus 2.0 Compliant:
  - Up to 6 selectable SMBus addresses for the EMC2303/5
  - SMBus Alert compatible
- CLK Pin Can Provide a Clock Source Output
- EMC2301 Available in an 8-Pin MSOP Lead-Free RoHS Compliant Package
- EMC2302 Available in a 10-Pin MSOP Lead-Free RoHS Compliant Package
- EMC2303 Available in a 12-Pin 4 mm x 4 mm QFN Lead-Free RoHS Compliant Package
- EMC2305 Available in a 16-Pin 4 mm x 4 mm QFN Lead-Free RoHS Compliant Package

General Description

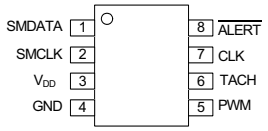
The EMC2301/2/3/5 family is an SMBus compliant fan controller with up to five independently controlled PWM fan drivers. Each fan driver is controlled by a programmable frequency PWM driver and Fan Speed Control algorithm that operates in either a closed loop fashion or as a directly PWM-controlled device.

Each closed loop Fan Speed Control (FSC) algorithm has the capability to detect aging fans and alert the system. It will likewise detect stalled or locked fans and trigger an interrupt.

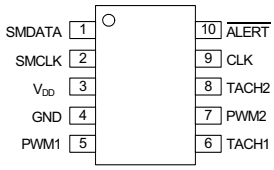
Additionally, the EMC2301/2/3/5 devices offer a clock output so that multiple devices may be chained as clients to the same clock source for optimal performance in large distributed systems.

Package Types

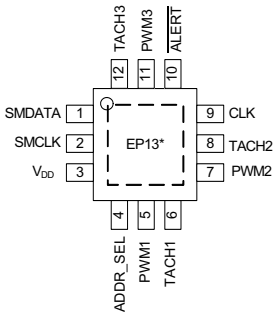
EMC2301 (MSOP-8)



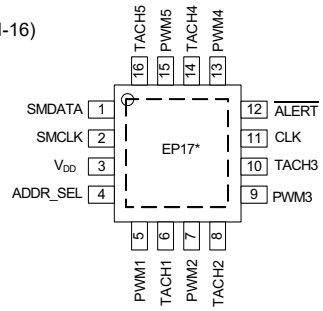
EMC2302 (MSOP-10)



EMC2303 (4 x 4 mmQFN-12)



EMC2305 (4 x 4 mm QFN-16)



* Includes Exposed Thermal Pad (see Table 3-1).

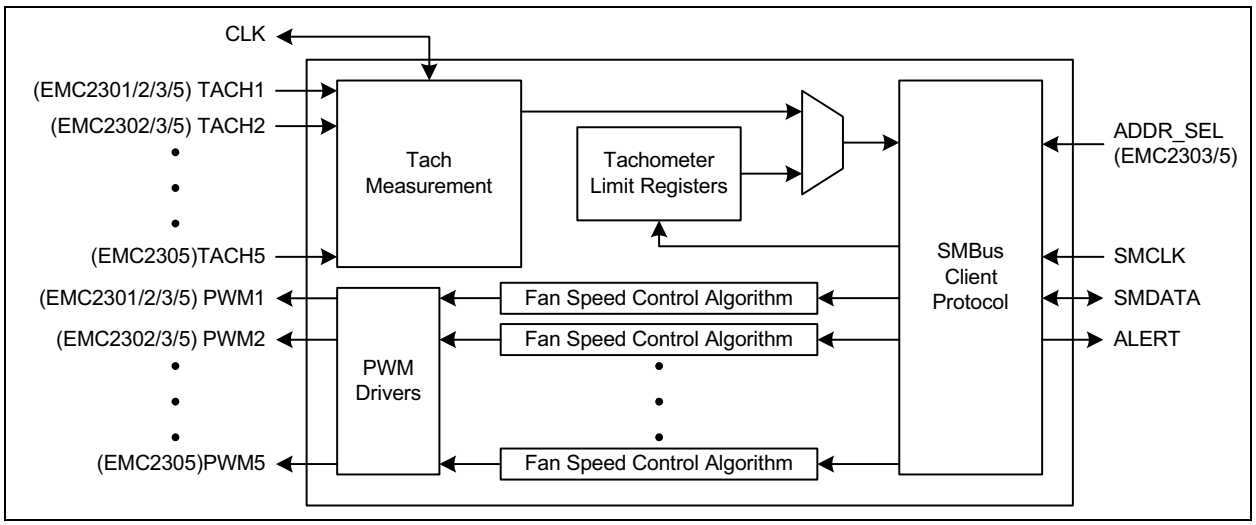
Device Features

Device	PWM Fan Control Channels	SMBus Address	Default Start-Up RPM Select
EMC2301	1	Fixed	No
EMC2302	2	Fixed	No
EMC2303	3	6 Selectable	Yes
EMC2305	5	6 Selectable	Yes

Applications

- Servers
- Projectors
- Industrial and Networking Equipment
- Notebook Computers

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings †

Ambient Temperature Under Bias ..... -40°C to +125°C
Storage Temperature ..... -55°C to +150°C
Voltage on V_{DD} with respect to GND ..... -0.3V to 4V
Voltage on 5V tolerant pins ($|V_{5VT\_pin} - V_{DD}|$ with respect to GND) (see Note 1) ..... 0V to 3.6V
Voltage on 5V tolerant pins with respect to GND ..... -0.3V to 5.5V
Voltage on any other pin with respect to GND ..... -0.3V to V_{DD} +0.3V
Package Thermal Resistance - Junction to Ambient (θ_{JA}) for QFN-16 ..... 40°C/W
Package Thermal Resistance - Junction to Ambient (θ_{JA}) for QFN-12 ..... 50°C/W
Package Thermal Resistance - Junction to Ambient (θ_{JA}) for MSOP-10 ..... 132°C/W
Package Thermal Resistance - Junction to Ambient (θ_{JA}) for MSOP-8 ..... 141°C/W
ESD Rating, All Pins, HBM ..... 2 kV

Note 1: For the 5V tolerant pins that have a pull-up resistor (SMCLK, SMDATA, TACH and $\overline{\text{ALERT}}$), the pull-up voltage must not exceed 3.6V when the device is unpowered.

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.2 DC Characteristics

Electrical Specifications: Unless otherwise indicated, V_{DD} = 3.0V to 3.6V, all typical values at T_A = +27°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DC Power						
Supply Voltage	V_{DD}	3	3.3	3.6	V	
Supply Current	I_{DD}	—	350	475	µA	EMC2301, channel active
		—	400	550		EMC2302, all channels active
		—	475	600		EMC2303, all channels active
		—	625	800		EMC2305, all channels active
PWM Fan Driver						
PWM Resolution	PWM	—	256	—	Steps	
PWM Duty Cycle	DUTY	0	—	100	%	
RPM-Based Fan Controller						
Tachometer Range	TACH	480	—	16000	RPM	
Tachometer Setting Accuracy	Δ_{TACH}	—	±0.5	±1	%	External oscillator 32.768kHz
		—	±1	±2		Internal oscillator
Input High Voltage	V_{IH}	2.0	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	
Output High Voltage	V_{OH}	V_{DD} - 0.4	—	—	V	8 mA current drive
Output Low Voltage	V_{OL}	—	—	0.4	V	8 mA current sink
Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$ pin powered and unpowered 0°C < T_A < 85°C Pull-up voltage ≤ 3.6V

1.3 SMBus Module DC Characteristics

Operating Conditions: Unless otherwise indicated, V_{DD} = 3V to 3.6V, T_A = -40°C to +125°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
SMBus Interface						
Input High Voltage	V_{IH}	2.0	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	
Output High Voltage	V_{OH}	V_{DD} - 0.4	—	—	V	
Output Low Voltage	V_{OL}	—	—	0.4	V	4 mA current sink
Input High/Low Current	I_{IH}/I_{IL}	—	—	±5	µA	Powered and unpowered 0°C < T_A < 85°C
Input Capacitance	C_{IN}	—	5	—	pF	
SMBus Timing						
Clock Frequency	f_{SMB}	10	—	400	kHz	
Spike Suppression	t_{SP}	—	—	50	ns	
Bus free time Start to Stop	t_{BUF}	1.3	—	—	µs	
Setup Time: Start	$t_{SU:STA}$	0.6	—	—	µs	
Setup Time: Stop	$t_{SU:STP}$	0.6	—	—	µs	
Data Hold Time	$t_{HD:DAT}$	0	—	—	µs	
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	µs	
Clock Low Period	t_{LOW}	1.3	—	—	µs	
Clock High Period	t_{HIGH}	0.6	—	—	µs	
Clock/Data Fall Time	t_{FALL}	—	—	300	ns	Min. = 20 + 0.1C_{LOAD} ns

1.3 SMBus Module DC Characteristics (Continued)

Operating Conditions: Unless otherwise indicated, V_{DD} = 3V to 3.6V, T_A = -40°C to +125°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Clock/Data Rise Time	t_{RISE}	—	—	300	ns	Min. = 20 + 0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}	—	—	400	pF	Per bus line

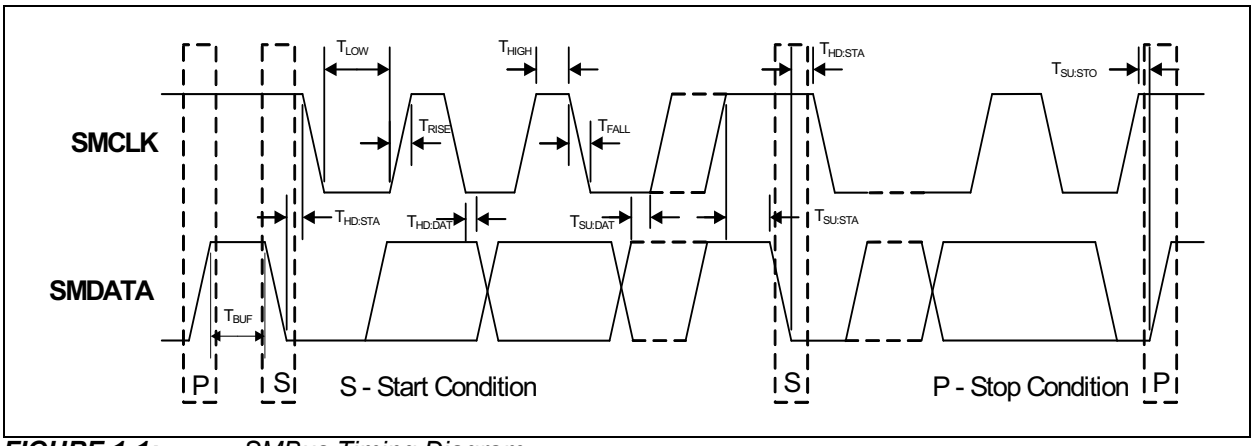


FIGURE 1-1: *SMBus Timing Diagram.*

NOTES:

2.0 TYPICAL OPERATING CURVES

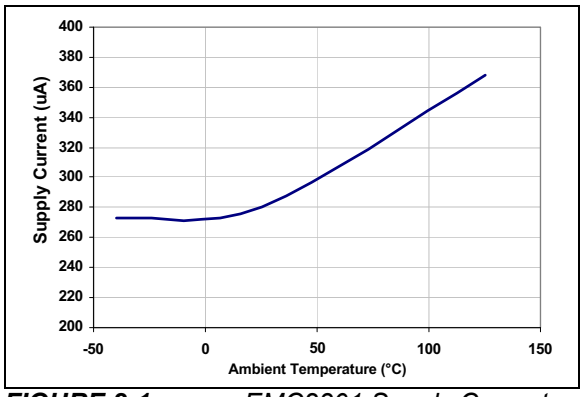


FIGURE 2-1: *EMC2301 Supply Current vs. Ambient Temperature.*

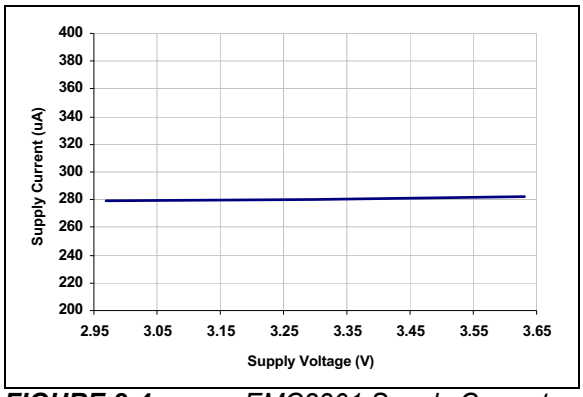


FIGURE 2-4: *EMC2301 Supply Current vs. Supply Voltage.*

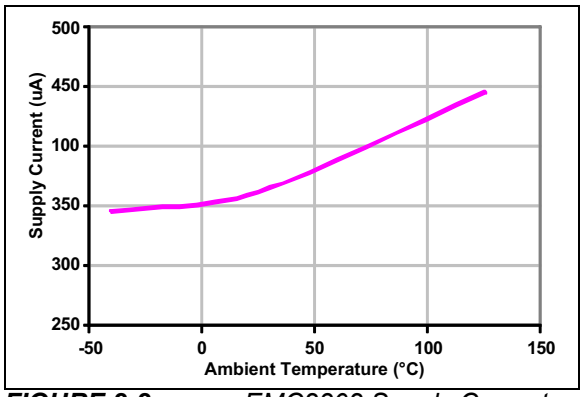


FIGURE 2-2: *EMC2302 Supply Current vs. Ambient Temperature.*

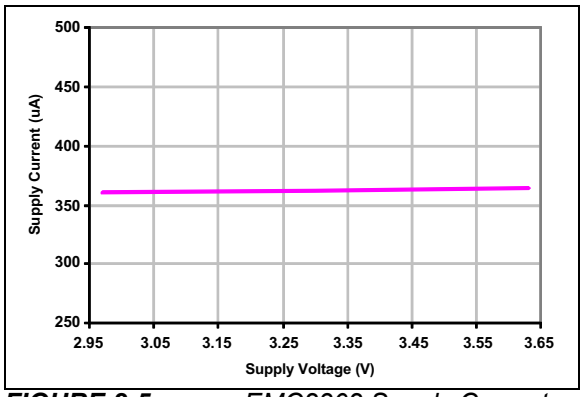


FIGURE 2-5: *EMC2302 Supply Current vs. Supply Voltage.*

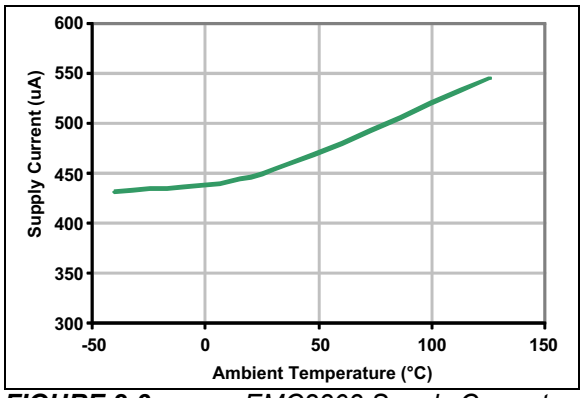


FIGURE 2-3: *EMC2303 Supply Current vs. Ambient Temperature.*

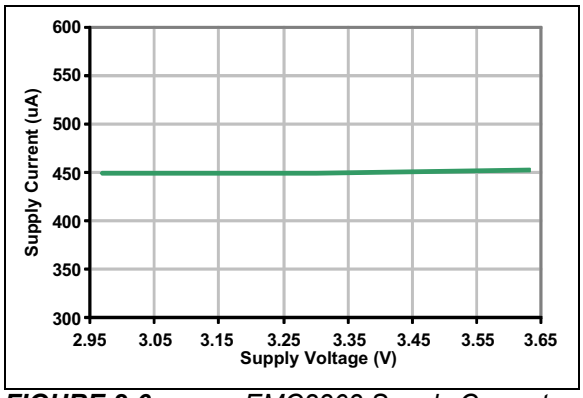


FIGURE 2-6: *EMC2303 Supply Current vs. Supply Voltage.*

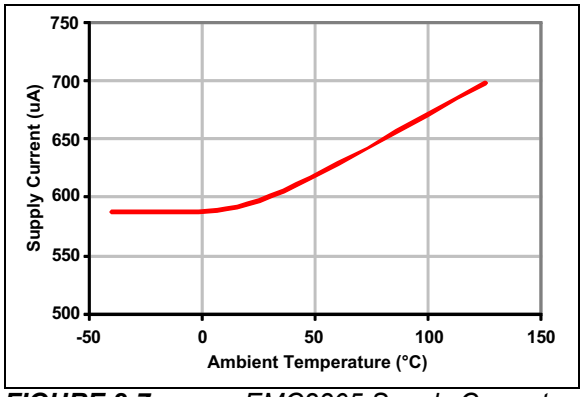


FIGURE 2-7: *EMC2305 Supply Current vs. Ambient Temperature.*

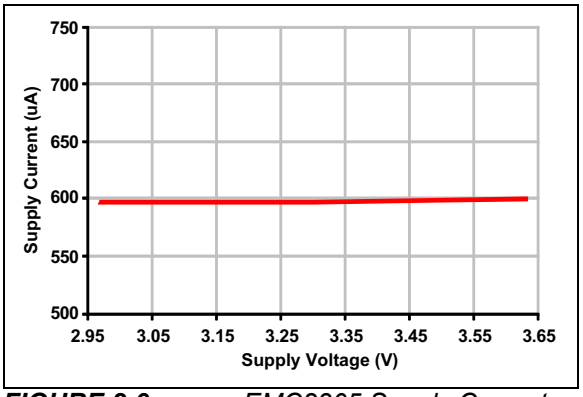


FIGURE 2-9: *EMC2305 Supply Current vs. Supply Voltage.*

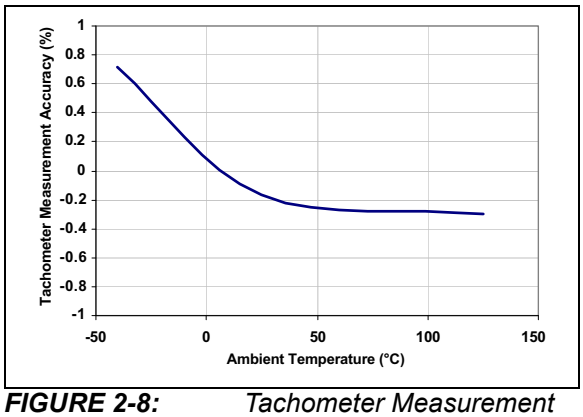


FIGURE 2-8: *Tachometer Measurement Accuracy vs. Ambient Temperature.*

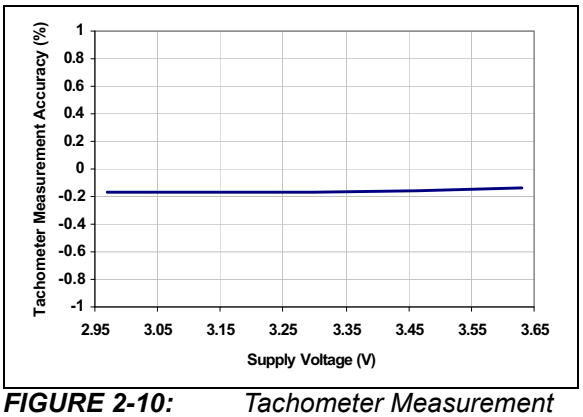


FIGURE 2-10: *Tachometer Measurement Accuracy vs. Supply Voltage.*

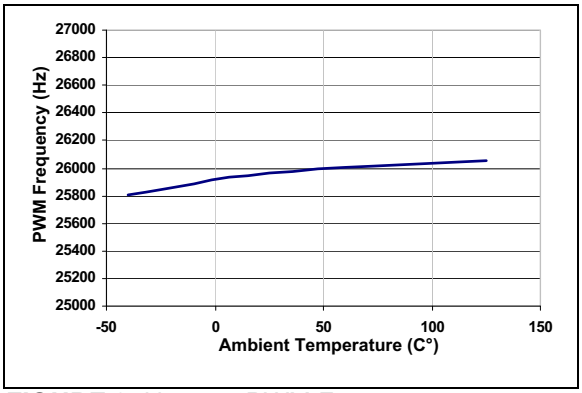


FIGURE 2-11: *PWM Frequency vs. Ambient Temperature V_{DD} = 3.3V, Base Frequency = 26 kHz.*

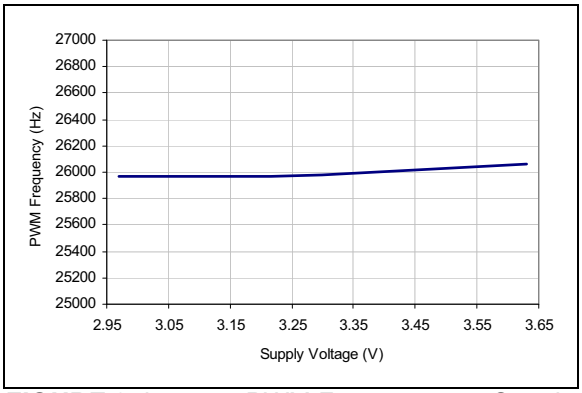


FIGURE 2-14: *PWM Frequency vs. Supply Voltage T_A = 25°C, Base Frequency = 26 kHz.*

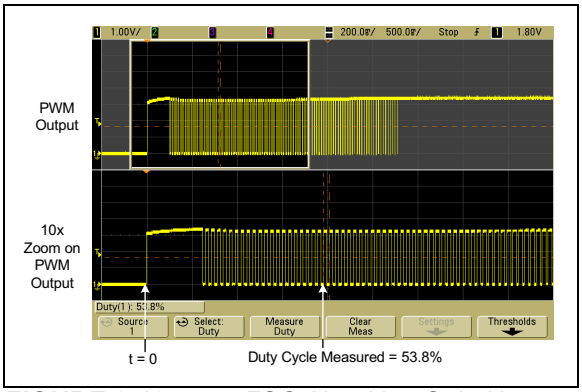


FIGURE 2-12: *FSC Algorithm Spin Up Routine. Spin Time = 1.0s; Spin Level = 55%; Updated Time = 200 ms. RPM Target from 0 RPM -> 8000 RPM @ time t = 0.*

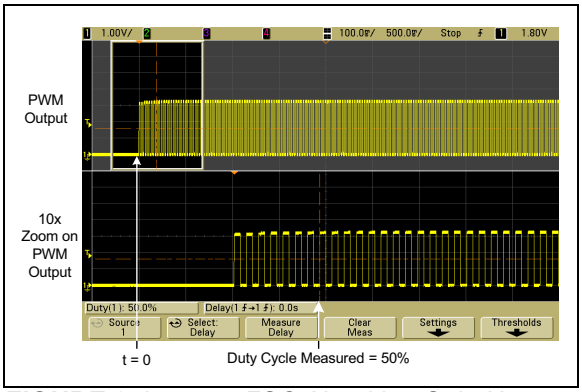


FIGURE 2-15: *FSC Algorithm Spin Up Routine – NoKick. Spin Time = 1.0s; Spin Level = 50%; UpdateTime = 200 ms. RPM Target from 0 RPM -> 8000 RPM @ time t = 0.*

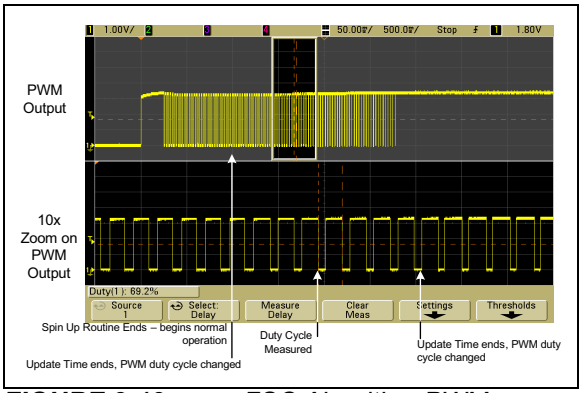


FIGURE 2-13: *FSC Algorithm PWM Ramping. Update Time = 200 ms; Max Step = 16 PWM counts.*
RPM Target from 0 RPM -> 8000 RPM @ time t = 0.

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1. The pin types are described in Table 3-2.

TABLE 3-1: PIN FUNCTION TABLE

EMC2305 (QFN-16)	EMC2303 (QFN-12)	EMC2302 (MSOP-10)	EMC2301 (MSOP-8)	Symbol	Pin Type	Description
1	1	1	1	SMDATA	DIOD	SMBus Data
2	2	2	2	SMCLK	DI	SMBus Clock
3	3	3	3	V_{DD}	Power	Power Supply
4	4	—	—	ADDR_SEL	AIO	Address Selection Input
5	5	5	5	PWM1	DO/OD	PWM1 Output
6	6	6	6	TACH1	DI	Tach 1 Input
7	7	7	—	PWM2	DO/OD	PWM2 Output
8	8	8	—	TACH2	DI	Tach 2 Input
9	11	—	—	PWM3	DO/OD	PWM3 Output
10	12	—	—	TACH3	DI	Tach 3 Input
11	9	9	7	CLK	DI/DO	Ext. 32.768 kHz clock
12	10	10	8	$\overline{\text{ALERT}}$	OD	SMBus Alert Pin
13	—	—	—	PWM4	DO/OD	PWM4 Output
14	—	—	—	TACH4	DI	Tach 4 Input
15	—	—	—	PWM5	DO/OD	PWM5 Output
16	—	—	—	TACH5	DI	Tach 5 Input
EP17	EP13	4	4	GND	Power	GROUND

The pin types are described in detail in Table 3-2.

TABLE 3-2: PIN TYPES

Pin Type	Description
Power	This pin is used to supply power or ground to the device.
DI	Digital Input: this pin is used as a digital input. This pin is 5V tolerant.
DO	Push/Pull Digital Output: this pin is used as a digital output. It can both source and sink current.
DIOD	Digital Input/Open Drain Output: this pin is used as a digital I/O. When it is used as an output, it is open drain and requires a pull-up resistor. This pin is 5V tolerant.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
AIO	Analog input/output. This pin is used for analog signals.

3.1 Pin Configurations

The EMC2301/2/3/5 family has four (4) variants that include features unique to each device. Refer to Table 3-1 to determine applicability of the pin descriptions.

3.1.1 SMDATA - SMBUS DATA

This is the open drain, bidirectional data pin for SMBus communication. Requires external pull-up resistor.

3.1.2 SMCLK - SMBUS CLOCK

This is the input clock pin for SMBus communication. Requires external pull-up resistor.

3.1.3 V_{DD} - POWER SUPPLY

This pin is the input power supply for the device.

3.1.4 ADDR_SEL - ADDRESS SELECT

Available only on the EMC2303 and EMC2305, this pin allows user programmability of the SMBus address. Requires external pull-up resistor.

3.1.5 PWM1/2/3/4/5 - PULSE WIDTH MODULATED OUTPUT

This is the output control signal from the Fan Speed Control 1/2/3/4/5 algorithms. This can be configured as a push-pull PWM output or an open drain PWM output (see **Section 4.2 "PWM Fan Driver"**).

3.1.6 TACH1/2/3/4/5 - TACHOMETER INPUT

Open drain tachometer input to Fan Speed Control 1/2/3/4/5 algorithms for feedback. Requires external pull-up resistor.

3.1.7 CLK - EXT. CLOCK

This is the common 32.768 kHz clock for improved Tach accuracy and a push-pull clock output to other fan controllers to synchronize Fan Speed Control.

3.1.8 $\overline{\text{ALERT}}$ - SMBUS ALERT PIN

This pin indicates when an out of limits or other error condition has occurred. Active low interrupt - requires external pull-up resistor.

3.1.9 GND, EP13, EP17

The exposed (bottom) pad is ground for the device.

4.0 PRODUCT DESCRIPTION

The EMC2301/2/3/5 family is an SMBus compliant fan controller with up to five programmable frequency PWM fan drivers. The fan drivers can be operated using two modes: the RPM-based Fan Speed Control algorithm or the direct fan drive setting. Figure 4-1 shows a system diagram of the EMC2301/2/3/5 family.

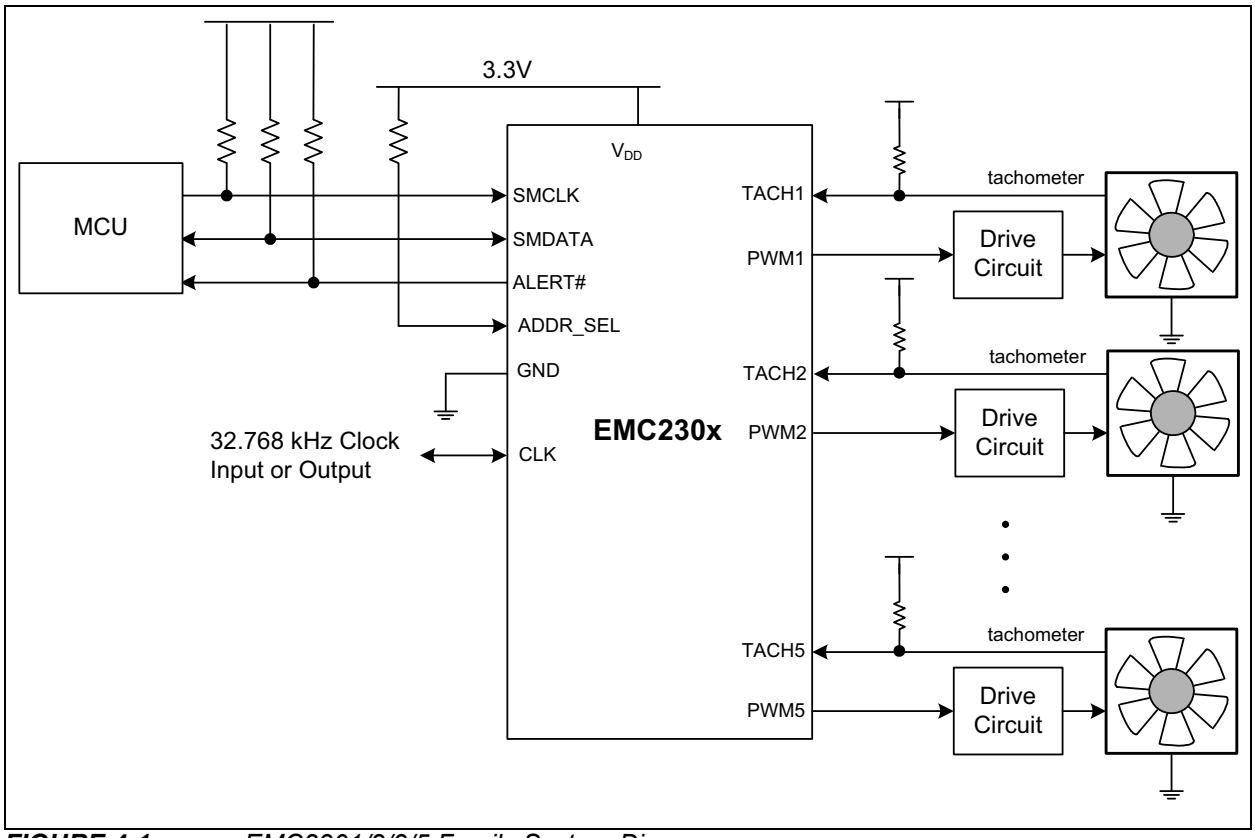


FIGURE 4-1: *EMC2301/2/3/5 Family System Diagram.*

4.1 Fan Control Modes of Operation

The EMC2301/2/3/5 has two modes of operation for each fan driver. Each mode of operation uses the Ramp Rate control and Spin Up Routine.

1. Direct Setting mode - in this mode of operation, the user directly controls the fan drive setting. Updating the Fan Driver Setting Register (see Register 6-11) will instantly update the PWM fan drive. Ramp rate control is optional and enabled via the ENRCx bits (see Register 6-14).

   Whenever the Direct Setting mode is enabled, the current drive will be changed to what was last written into the Fan Driver Setting Register. The conversion from register value to percent drive in shown in Equation 4-1.

EQUATION 4-1: REGISTER VALUE TO DRIVE

$$Drive = \left(\frac{VALUE}{255}\right) \times 100\%$$

2. Fan Speed Control (FSC) mode - in this mode of operation, the user determines a target tachometer count and the PWM drive setting is automatically updated to achieve this target speed.

   The algorithm uses the Spin Up Routine and has user-definable ramp rate controls.

   This mode is enabled setting the ENAGx bit in the Fan Configuration Register (see Register 6-13).

TABLE 4-1: FAN CONTROLS ACTIVE FOR OPERATING MODE

Direct Setting Mode	FSC Mode
Fan Driver Setting (Read/Write)	Fan Driver Setting (Read Only)
EDGES[1:0]	EDGES[1:0] (Fan Configuration)
—	RANGE[1:0] (Fan Configuration)
UPDATE[2:0] (Fan Configuration)	UPDATE[2:0] (Fan Configuration)
LEVEL (Spin Up Configuration)	LEVEL (Spin Up Configuration)
SPINUP_TIME[1:0] (Spin Up Configuration)	SPINUP_TIME[1:0] (Spin Up Configuration)
Fan Step	Fan Step
—	Fan Minimum Drive
Valid TACH Count	Valid TACH Count
—	TACH Target (Read/Write)
TACH Reading	TACH Reading
—	DRIVE_FAIL_CNT[1:0] and Drive Band Fail Registers

4.2 PWM Fan Driver

The EMC2301/2/3/5 supports up to five PWM output drivers. Each output driver can be configured to operate as an open-drain (default) or push-pull driver and can be configured with normal or inverse polarity (see Register 6-8).

Additionally, the PWM frequencies are independently programmable with ranges from 9.5 Hz to 26 kHz in four programmable frequency bands shown in Table 4-2 (see Register 6-9 and Register 6-10).

TABLE 4-2: PWM_BASEX BIT DECODE

PWM_BASEX[1:0]		Base Frequency
1	0	
0	0	26.00 kHz (default)
0	1	19.531 kHz
1	0	4.882 kHz
1	1	2.441 kHz

The frequency of the PWM drive can further be tuned through the PWM Frequency Divide Registers (see Register 6-12). The 8-bit value stored in this register divides the base frequency, allowing the 9.5 Hz PWM frequency to be generated from the 2441 Hz Base Frequency. A value of 00h or 01h in the PWM Frequency Divide Register is decoded as 01h.

4.3 RPM-Based Fan Speed Control Algorithm

The EMC2301/2/3/5 includes up to five RPM-based Fan Speed Control algorithms. Each algorithm operates independently and controls a separate fan driver. Each algorithm is controlled manually (by setting the target fan speed).

This fan control algorithm uses proportional, integral, and derivative terms to automatically approach and maintain the system's desired fan speed to an accuracy directly proportional to the accuracy of the clock source.

The desired tachometer count is set by the user inputting the desired number of 32.768 kHz cycles that occur per fan revolution. This is done by manually setting the TACH Target Register. The user may change the target count at any time. The user may also set the target count to FFh in order to disable the fan driver for lower current operation.

For example, if a desired RPM rate for a 2-pole fan is 3000 RPM, then the user would input the hexadecimal equivalent of 1296 (51h in the TACH Target Register). This number represents the number of 32.768 KHz cycles that would occur during the time it takes the fan to complete a single revolution when it is spinning at 3000 RPM.

The EMC2301/2/3/5's RPM-based Fan Speed Control algorithm has programmable configuration settings for parameters such as ramp-rate control and spin up conditions. The fan driver automatically detects and attempts to alleviate a Stalled/Stuck fan condition while also asserting the $\overline{\text{ALERT}}$ pin. The EMC2301/2/3/5 works with fans that operate up to 16000 RPM and provide a valid tachometer signal.

The fan controller will function either with an externally supplied 32.768 kHz clock source or with its own internal 32 kHz oscillator depending on the required accuracy. The EMC2301/2/3/5 offers a clock output that enables additional devices to be set as clients to the same clock source.

The update rate of the PID loop and Ramp Rate Control is controlled by the Fan Configuration 1 and 2 Registers settings (see Register 6-13 and Register 6-14). The values for the Update Time settings in the Fan Configuration 1 register are shown in Table 4-3.

TABLE 4-3: UPDATE TIME

UPDATEX[2:0]			Update Time
2	1	0	
0	0	0	100 ms
0	0	1	200 ms
0	1	0	300 ms
0	1	1	400 ms (default)
1	0	0	500 ms

TABLE 4-3: UPDATE TIME (CONTINUED)

UPDATEX[2:0]			Update Time
2	1	0	
1	0	1	800 ms
1	1	0	1200 ms
1	1	1	1600 ms

4.3.1 ERROR WINDOW

The FSC has a controllable error window, allowing the user to determine how close to the programmed RPM the fan needs to come before the FSC algorithm stops attempting to adjust fan speed (see Register 6-14). This feature helps prevent “motor-boating” when controlling difficult fans. The values for the error range is shown in Table 4-4.

TABLE 4-4: ERROR RANGE OPTIONS

ERGX[1:0]		Operation
1	0	
0	0	0 RPM (default)
0	1	50 RPM
1	0	100 RPM
1	1	200 RPM

4.3.2 PROGRAMMING THE RPM-BASED FAN SPEED CONTROL ALGORITHM

The RPM-based Fan Speed Control algorithm is disabled upon device power-up. The following registers control the algorithm. The EMC2301/2/3/5 fan control registers are preloaded with defaults that will work for a wide variety of fans so only the TACH Target Register is required to set a fan speed. The other fan control registers can be used to fine-tune the algorithm behavior based on application requirements.

Note that steps 1 to 6 below are optional and need only be performed if the default settings do not provide the desired fan response.

1. Set the Spin Up Configuration Register to the spin up level and spin time desired.
2. Set the Fan Step Register to the desired step size.
3. Set the Fan Minimum Drive Register to the minimum drive value that will maintain fan operation.
4. Set the Update Time and Edges options in the Fan Configuration Register.
5. Set the Valid TACH Count Register to the highest tach count that indicates the fan is spinning. Refer to AN17.4 RPM to TACH Counts Conversion for examples and tables for supported RPM ranges (500, 1k, 2k, 4k).
6. Set the TACH Target Register to the desired tachometer count.
7. Enable the RPM-based Fan Speed Control algorithm by setting the ENAG bit.

4.3.3 ADVANCED TOPICS USING THE FAN SPEED CONTROL ALGORITHM

In addition to the seven steps listed in this section, there are several other optional settings that may be used when attempting to control a fan that the previous steps failed to do.

4.3.3.1 Selecting the Derivative Options

The DPT bits in Register 6-14 allow the user to select the derivative response applied to the closed loop calculation. Table 4-5 shows the options available. A brief description is included in the table.

TABLE 4-5: DERIVATIVE OPTIONS

DPTX[1:0]		Name	Operation
1	0		
0	0	NONE	No derivative options used.
0	1	BASIC	The derivative of the current error, along with the Proportional and Integral values, are added to the iterative Fan Drive Register setting.
1	0	STEP	Same as the BASIC option, but the result is not limited by the MAX STEP SIZE register.
1	1	BOTH	Uses BASIC and STEP, effectively providing a gain of 2.

4.3.3.2 Setting the PID Gains

The Gain registers store the gain terms used by the proportional and integral portions of each of the RPM-based Fan Speed Control algorithms (see Register 6-15). These gain terms are used as the KD, KI, and KP gain terms in a classic PID control solution. The effective gains are shown in Table 4-6.

TABLE 4-6: GAIN DECODE

GAIND or GAINP or GAINI[1:0]		Respective Gain Factor
1	0	
0	0	1x
0	1	2x
1	0	4x (default)
1	1	8x

4.3.3.3 Fan Drive Max Step

The Fan Max Step registers (see Register 6-17), along with the Update Time in the Fan Configuration 1 Register, control the ramp rate of the fan driver response calculated by the RPM-based Fan Speed Control algorithm. The value of the register represents the maximum step size each fan driver will take between update times.

When the FSC algorithm is enabled, ramp rate control is automatically used. When the FSC is not active, then ramp rate control can be enabled by asserting the ENRCx bit (see Register 6-14).

The Update Time (UDT) bits and Fan Step Register settings operate independently of the RPM-based FSC algorithm and will always limit the fan drive setting.

That is, if the programmed fan drive setting (either as determined by the RPM-based FSC algorithm or by manual settings) exceeds the current fan drive setting by greater than the Fan Step Register setting, the EMC2301/2/3/5 will limit the fan drive change to the value of the Fan Step Register. It will use the Update Time to determine how often to update the drive settings.

If the Fan Speed Control Algorithm is used, the default settings in Register 6-14 will cause the maximum fan step settings to be ignored.

4.3.3.4 Minimum Drive Setting

The Fan Minimum Drive Register (see Register 6-18) stores the minimum drive setting for each RPM-based Fan Speed Control algorithm. The RPM-based Fan Speed Control algorithm will not drive the fan at a level lower than the minimum drive unless the target Fan Speed is set at FFh.

During normal operation, if the fan stops for any reason (including low drive), the RPM-based Fan Speed Control algorithm will attempt to restart the fan. Setting the Fan Minimum Drive Register to a setting that will maintain fan operation is a useful way to avoid potential fan oscillations as the control circuitry attempts to drive it at a level that cannot support fan operation.

4.4 Tachometer Measurement

The tachometer measurement circuitry is used in conjunction with the RPM-based Fan Speed Control Algorithm to update the fan driver output. Additionally, it can be used in Direct Setting mode as a diagnostic for host based fan control.

This method monitors the TACHx signal in real time. It constantly updates the tachometer measurement by reporting the number of clocks between a user programmed number of edges (EDGX bits in Register 6-13) on the TACHx signal (see Table 4-7).

Note:	The tachometer measurement method works independently of the drive settings. If the device is put into Direct Setting mode and the fan drive is set at a level that is lower than the fan can operate (including zero drive), then the tachometer measurement may signal a Stalled Fan condition and assert an interrupt.

TABLE 4-7: MINIMUM EDGES FOR FAN ROTATION

EDGX[1:0]		Minimum TACH Edges	Number of Fan Poles	Effective TACH Multiplier (Based on Two Pole Fans)
1	0			
0	0	3	1	0.5
0	1	5	2 (default)	1
1	0	7	3	1.5
1	1	9	4	2

The tachometer measurement provides fast response times for the RPM-based Fan Speed Control algorithm and the data is presented as a count value that represents the fan RPM period.

4.4.1 TACHOMETER COUNTS TO RPM

The TACH Reading Registers describe the current tachometer reading for each of the fans. By default, the data represents the fan speed as the number of 32 kHz clock periods that occur for a single revolution of the fan.

Equation 4-2 shows the detailed conversion from TACH measurement (COUNT) to RPM, while Equation 4-3 shows the simplified translation of TACH Reading Register count to RPM assuming a two-pole fan, measuring five edges, with a frequency of 32.768 kHz. These equations are solved and tabulated for ease of use in AN17.4 RPM to TACH Counts Conversion.

EQUATION 4-2: TACHOMETER COUNTS TO RPM

$$RPM = \frac{1}{(poles)} \times \frac{(n-1)}{COUNT \times \frac{1}{m}} \times f_{TACH} \times 60$$

Where:

- *poles* = number of poles on the fan (typically two)
- f_{TACH} = the tachometer measurement frequency (typically 32.768 kHz)
- *n* = number of edges measured (typically five for a two-pole fan)
- *m* = the multiplier defined by the RANGE bits
- *COUNT* = TACH Reading Register value (in decimal)

EQUATION 4-3: SIMPLIFIED TACH CONVERSION

$$RPM = \frac{3932160 \times m}{COUNT}$$

Where:

COUNT = TACH Reading Register value (in decimal)

4.4.2 VALID TACHOMETER READINGS

The Valid TACH Count registers store the maximum TACH Reading Register value to indicate that each fan is spinning properly. The value is referenced at the end of the Spin Up Routine to determine if the fan has started operating and decide if the device needs to retry. See **Section 4.4.1 "Tachometer Counts to RPM"** for translating the count to an RPM.

If the TACH Reading Register value exceeds the Valid TACH Count Register (indicating that the Fan RPM is below the threshold set by this count), then a Stalled Fan is detected. In this condition, the algorithm will automatically begin its Spin Up Routine.

If a TACH Target setting is set above the Valid TACH Count setting, then that setting will be ignored and the algorithm will use the current fan drive setting. The Valid Tach Count value is stored in Register 6-19.

4.4.3 STALLED FAN

A stalled fan is detected if the tach counter exceeds the user-programmable Valid TACH Count setting. If a stall is detected, the device will flag the fan as stalled and trigger an interrupt.

If the RPM-based Fan Speed Control algorithm is enabled, the algorithm will automatically attempt to restart the fan until it detects a valid tachometer level or is disabled.

The FNSTL status bit indicates that a stalled fan was detected (see Register 6-2). This bit is checked conditionally depending on the mode of operation.

- Whenever the Direct Setting mode or the Spin Up Routine is enabled, the FNSTL interrupt will be masked for the duration of the programmed Spin Up Time (see Table 4-11) to allow the fan to reach a valid speed without generating unnecessary interrupts.
- In Direct Setting mode, whenever the TACH Reading Register value exceeds the Valid TACH Count Register setting, the FNSTL status bit will be set.
- When using the RPM-based Fan Speed Control algorithm, the Stalled Fan condition is checked whenever the Update Time is met and the fan drive setting is updated. It is not a continuous check.

4.4.4 AGING FAN OR INVALID DRIVE DETECTION

This feature is useful to detect Aging Fan conditions (where the fan's natural maximum speed degrades over time) or a speed setting that is faster than the fan is capable of. The EMC2301/2/3/5 contains circuitry that detects if the programmed fan speed can be reached by the fan.

If the target fan speed cannot be reached within a user defined band of tach counts at maximum drive stored in Register 6-20 and Register 6-21, the DRVFx status bits (see Register 6-5) are set and the $\overline{\text{ALERT}}$ pin is asserted. Table 4-8 shows the decode based on DFC bits in Register 6-16. This setting determines how long the aging fan circuitry will interrogate the Tach Reading register before setting the status bits.

TABLE 4-8: DRIVE FAIL SAMPLE TIME

DFCX[1:0]		Number of Update Periods
1	0	
0	0	Disabled - the Drive Fail detection circuitry is disabled (default)
0	1	16 - the Drive Fail detection circuitry will count for 16 update periods
1	0	32 - the Drive Fail detection circuitry will count for 32 update periods
1	1	64 - the Drive Fail detection circuitry will count for 64 update periods

4.5 CLK Pin

The CLK pin has multiple functionality as determined by the pull-up decode of the ADDR_SEL pin and the settings of the Configuration register. The functionality associated with the CLK pin upon device power-up is independent of the CLK pin functionality after the device has been configured. The added functionality of the CLK pin is available only on the EMC2303/5.

4.6 Pull-Up Decode

The EMC2303/5 have the ability to program the SMBus address and default fan setting using a resistor pull-up on CLK. If additional functionality is enabled via the ADDR_SEL pin (see Table 5-1), then the CLK pin should be configured with a pull-up resistor to V_{DD} and should not be used. The value of the pull-up resistor on the CLK pin is used to determine the default drive state of all fan drivers as shown in Table 4-9.

TABLE 4-9: CLK PIN PULL-UP DECODE

Pull-Up Resistor	Fan Default Drive Setting
4.7k Ohm ±5%	0% - OFF
6.8k Ohm ±5%	30%
10k Ohm ±5%	50%
15k Ohm ±5%	75%
22k Ohm ±5%	100%
33k Ohm ±5%	0% - OFF

4.7 External Clock

The EMC2301/2/3/5 allows the user to choose between supplying an external 32.768 kHz clock or use of the internal 32 kHz oscillator to measure the tachometer signal. This clock source is used by the RPM-based Fan Speed Control algorithm to calculate the current fan speed. This fan controller accuracy is directly proportional to the accuracy of the clock source.

When this function is used, the external clock is driven into the device via the CLK pin.

4.7.1 INTERNAL CLOCK

Alternately, the EMC2301/2/3/5 may be configured to use its internal clock as a clock output to drive other fan driver devices. When configured to operate in this mode, the device uses its internal clock for tachometer reading and drives the CLK pin using a push-pull driver.

4.8 Spin Up Routine

The EMC2301/2/3/5 also contains programmable circuitry to control the spin up behavior of the fan driver to ensure proper fan operation. This circuitry is controlled though the Spin-Up Configuration register (see Register 6-16).

The Spin Up Routine is initiated in the Direct Setting mode when the setting value changes from 00h to anything else.

When the Fan Speed Control algorithm is enabled, the Spin Up Routine is initiated under the following conditions:

1. The TACH Target Register value changes from a value of FFh to a value that is less than the Valid TACH Count (see Register 6-19).
2. The RPM-based Fan Speed Control algorithm's measured TACH Reading Register value is greater than the Valid TACH Count setting.

When the Spin Up Routine is operating, the fan driver is set to full scale (optional) for one quarter of the total user defined spin up time. For the remaining spin up time, the fan driver output is set at a user-defined level as shown in Table 4-10.

TABLE 4-10: SPIN LEVEL

SPLVX[2:0]			Spin Up Drive Level
2	1	0	
0	0	0	30%
0	0	1	35%
0	1	0	40%
0	1	1	45%
1	0	0	50%
1	0	1	55%
1	1	0	60% (default)
1	1	1	65%

The amount of time allocated to the Spin Up Routine is also selectable using the SPT bits within Register 6-16. The times available are shown in Table 4-11.

TABLE 4-11: SPIN TIME

SPTX[1:0]		Total Spin Up Time
1	0	
0	0	250 ms
0	1	500 ms (default)
1	0	1 sec
1	1	2 sec

After the Spin Up Routine has finished, the EMC2301/2/3/5 measures the TACHx signal. If the measured TACH Reading Register value is higher than the Valid TACH Count Register setting, the FNSPIN status bit (see Register 6-2) is set and the Spin Up Routine will automatically attempt to restart the fan.

Figure 4-2 shows an example of the Spin Up Routine in response to a programmed fan speed change based on the first condition above.

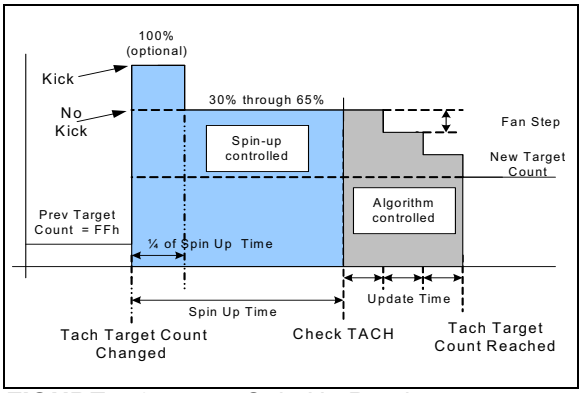


FIGURE 4-2: *Spin Up Routine.*

4.9 Power-Up Options

The EMC2303/5 allows for one of four fan speed options upon device power-up depending on the status of the pull-up resistor on the ADDR_SEL pin and the CLK pin. If the ADDR_SEL pin decode enables the CLK pin (see Table 5-1), then the value of the pull-up resistor on the CLK pin is used to determine the default fan drive setting (see **Section 4.6 "Pull-Up Decode"**).

If the Fan Drive setting is set at a non-zero value (as determined by the CLK pin), then the drive setting will be set to the desired setting. The Spin Up Routine will not be activated. This function does not disable the Watchdog timer which will continue to function normally. See **Section 4.11 "Watchdog Timer"**.

4.10 Ramp Rate Control

The Fan Driver can be configured with automatic ramp rate control. Ramp rate control is accomplished by adjusting the drive output settings based on the Maximum Fan Step Register settings and the Update Time settings.

If the RPM-based Fan Speed Control algorithm is used, then this ramp rate control is automatically used. The user programs a maximum step size for the fan drive setting and an update time. The update time varies from 100 ms to 1.6s while the fan drive maximum step can vary from 1 count to 31 counts, and can be set in Register 6-17.

When a new fan drive setting is entered, the delta from the next fan drive setting and the previous fan drive setting is determined. If this delta is greater than the Max Step settings, then the fan drive setting is incrementally adjusted every 100 ms to 1.6s as determined by the Update Time until the target fan drive setting is reached. See Table 4-3.

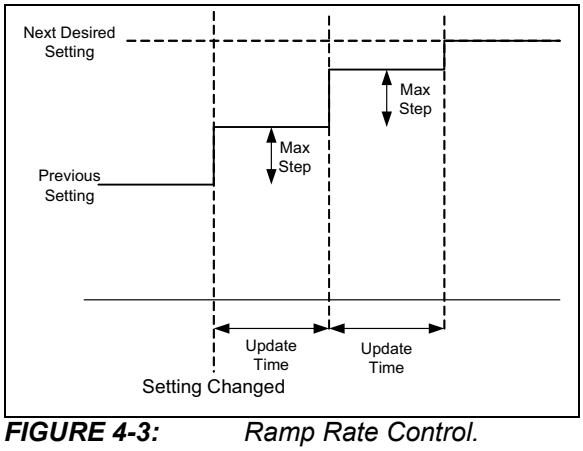


FIGURE 4-3: *Ramp Rate Control.*

4.11 Watchdog Timer

The EMC2301/2/3/5 contains an internal Watchdog Timer for all fan drivers. The Watchdog Timer monitors the SMBus traffic for signs of activity and works in two different modes based upon device operation. These modes are Power-Up Operation and Continuous Operation as described below.

For either mode of operation, if four seconds elapse without activity detected by the host, then the Watchdog will be triggered and the following will occur:

1. The WATCH status bit will be set.
2. The fan driver will be set to full scale drive. It will remain at full scale drive until it is disabled.
3. The $\overline{\text{ALERT}}$ pin will be asserted.

Note:	When the Watchdog timer is activated, the Fan Speed Control algorithm is automatically disabled. Disabling the Watchdog will not automatically set the fan drive nor re-activate the Fan Speed Control algorithm. This must be done manually.

4.11.1 POWER-UP OPERATION

The Watchdog Timer only starts immediately after power-up. Once it has been triggered or deactivated, it will not restart although it can be configured to operate in Continuous operation. While the Watchdog timer is active, the device will not check for a Stalled Fan condition.

During the Power-Up Operation, the Watchdog Timer is disabled by any of the following actions:

1. Writing the Fan Setting Register will disable the Watchdog Timer.
2. Enabling the RPM-based Fan Speed Control algorithm by setting the ENAGx bit will disable the Watchdog Timer. The fan driver will be set based on the RPM-based Fan Speed Control algorithm.

Writing any other configuration registers will not disable the Watchdog Timer upon power-up.

4.11.2 CONTINUOUS OPERATION

When configured to operate in Continuous Operation, the Watchdog Timer will start immediately (see WD_EN bits in Register 6-2). The timer will be reset by any access (read or write) to the SMBus register set. The four second Watchdog Timer will restart upon completion of SMBus activity.

NOTES:

5.0 SYSTEM MANAGEMENT BUS PROTOCOL

The EMC2301/2/3/5 communicates with a host controller through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 5-1. Stretching of the SMCLK signal is supported; however, the EMC2301/2/3/5 will not stretch the clock signal.

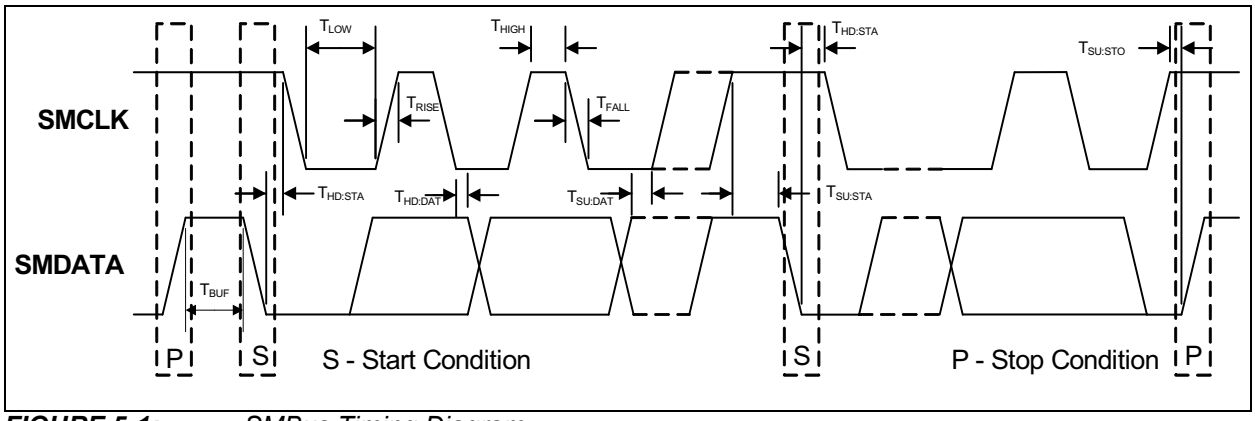


FIGURE 5-1: *SMBus Timing Diagram.*

5.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

5.2 SMBus Address and RD/$\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by an RD/$\overline{WR}$ indicator bit. If this RD/$\overline{WR}$ bit is a logic '0', then the SMBus Host is writing data to the client device. If this RD/$\overline{WR}$ bit is a logic '1', then the SMBus Host is reading data from the client device.

The EMC2303 and EMC2305 will respond to one of multiple SMBus addresses determined by the pull-up resistor on the ADDR_SEL pin. The ADDR_SEL pin decodes one of six pull-up resistors upon device power-up. Depending on the resistor used, the CLK pin may also be used to select additional functionality. The resistor values for each address is shown in Table 5-1.

TABLE 5-1: ADDR_SEL PIN DECODE (EMC2303/5 ONLY)

Pull-Up Resistor	SMBus Address	Additional Functions
4.7 kΩ ± 5%	0101_110(r/w)	None - CLK pin used as clock input or output.
6.8 kΩ ± 5%	0101_111(r/w)	
10 kΩ ± 5%	0101_100(r/w)	
15 kΩ ± 5%	0101_101(r/w)	
22 kΩ ± 5%	1001_100(r/w)	
33 kΩ ± 5%	1001_101(r/w)	CLK pin used to determine default fan drive - see **Section 4.6 "Pull-Up Decode"**. The CLK pin cannot be used as a clock input or output

The EMC2302-1 SMBus address is set at 0101_110(r/w)b.

The EMC2302-2 SMBus address is set at 0101_111(r/w)b.

The EMC2301 SMBus address is set at 0101_111(r/w)b.

5.3 SMBus Data Bytes

All SMBus Data bytes are sent Most Significant bit first and composed of 8 bits of information.

5.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the $\overline{\text{ALERT}}$ pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the host will ACK each data byte that it receives except the last data byte.

5.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the EMC2301/2/3/5 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.6 SMBus Time-Out

The EMC2301/2/3/5 includes an SMBus timeout feature. Following a 30 ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The SMBus timeout feature is disabled by default and can be enabled via clearing the DIS_TO bit in the Configuration register (see Register 6-1).

5.7 SMBus and I²C Compliance

The major difference between SMBus and I²C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10 kHz (I²C has no minimum frequency).
2. The client protocol will reset if the clock is held low for longer than 30 ms (I²C has no timeout).
3. The client protocol will reset if both the clock and data lines are held high for longer than 150 µs.
4. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).
5. The Block Read and Block Write protocols are only compliant with I²C data formatting. They do not support SMBus formatting for Block Read and Block Write protocols.

5.8 SMBus Protocols

The EMC2301/2/3/5 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Block Read and Receive Byte as valid protocols as shown below. The EMC2301/2/3/5 also supports the I²C Block Read and Block Write protocols. The device supports Write Byte, Read Byte, and Block Read/Block Write. All of the below protocols use the convention in Table 5-2.

TABLE 5-2: SMBUS PROTOCOL

Data Sent to Device	Data Sent to the Host
# of bits sent	# of bits sent

5.9 SMBus Write Byte

The Write Byte is used to write one byte of data to the registers, as shown in Table 5-3.

TABLE 5-3: WRITE BYTE PROTOCOL

START	CLIENT ADDR.	WR	ACK	REG. ADDR.	ACK	REG. DATA	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

5.10 Block Write

The Block Write protocol is used to write multiple data bytes to a group of contiguous registers as shown in Table 5-4. It is an extension of the Write Byte protocol.

Note: When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

TABLE 5-4: BLOCK WRITE PROTOCOL

START	CLIENT ADDR.	WR	ACK	REG. ADDR.	ACK	REPEAT N TIMES		STOP
						REG. DATA	ACK	
1 → 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 → 1

Note: The Block Write and Block Read protocols require that the address pointer be automatically incremented. For a write command, the address pointer will be automatically incremented when the ACK is sent to the host. There are no over or under bound limit checking and the address pointer will wrap around from FFh to 00h if necessary.

5.11 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Table 5-5.

TABLE 5-5: READ BYTE PROTOCOL

START	CLIENT ADDR.	WR	ACK	REG. ADDR.	ACK	
1 → 0	YYYY_YYY	0	0	XXh	0	
START	**CLIENT ADDR.**	**RD**	**ACK**	**REG. DATA**	**NACK**	**STOP**
1 → 0	YYYY_YYYb	1	0	XXh	1	0 → 1

5.12 Block Read

The Block Read protocol is used to read multiple data bytes from a group of contiguous registers as shown in Table 5-6. It is an extension of the Read Byte Protocol.

Note: When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

TABLE 5-6: BLOCK READ PROTOCOL

START	CLIENT ADDR.	WR	ACK	REG. ADDR.	ACK			
1 → 0	YYYY_YYY	0	0	XXh	0			
START	**CLIENT ADDR.**	**RD**	**ACK**	**REG. DATA**	**ACK**	**REG. DATA**	**NACK**	**STOP**
1 → 0	YYYY_YYY	1	0	XXh	0	XXh	1	0 → 1

Note: The Block Write and Block Read protocols require that the address pointer be automatically incremented. For a read command, the address pointer will be automatically incremented when the ACK is sent by the host. There are no over or under bound limit checking and the address pointer will wrap around from FFh to 00h if necessary.

5.13 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 5-7.

TABLE 5-7: SEND BYTE PROTOCOL

START	CLIENT ADDR.	WR	ACK	REG. ADDR.	ACK	STOP
1 → 0	YYYY_YYY	0	0	XXh	0	0 → 1

5.14 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 5-8.

TABLE 5-8: RECEIVE BYTE PROTOCOL

START	CLIENT ADDR.	RD	ACK	REG. DATA	NACK	STOP
1 → 0	YYYY_YYY	1	0	XXh	1	0 → 1

5.15 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt. When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address as shown in Table 5-9.

TABLE 5-9: ALERT RESPONSE ADDRESS PROTOCOL

START	ALERT RESPONSE ADDR.	RD	ACK	DEVICE ADDR.	NACK	STOP
1 → 0	0001_100b	1	0	YYYY_YYYb	1	0 → 1

The EMC2301/2/3/5 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Client Address and verify that full client address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

NOTES:

6.0 REGISTERS

Table 6-1 shows the register map.

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Lock	POR Value
Configuration	20h	MASK	DIS_TO	WD_EN	—	—	—	DRECK	USECK	SWL	40h
Fan Status	24h	WATCH	—	—	—	—	DVFAIL	FNSPIN	FNSTL	No	00h
Fan Stall Status	25h	—	—	—	F5STL	F4STL	F3STL	F2STL	F1STL	No	00h
Fan Spin Status	26h	—	—	—	F5SPIN	F4SPIN	F3SPIN	F2SPIN	F1SPIN	No	00h
Drive Fail Status	27h	—	—	—	DRVF5	DRVF4	DRVF3	DRVF2	DRVF1	No	00h
Fan Interrupt Enable Register	29h	—	—	—	F5ITEN	F4ITEN	F3ITEN	F2ITEN	F1ITEN	No	00h
PWM Polarity Config	2Ah	—	—	—	PLRTY 5	PLRTY 4	PLRTY 3	PLRTY 2	PLRTY 1	No	00h
PWM Output Config	2Bh	—	—	—	PM5OT	PM4OT	PM3OT	PM2OT	PM1OT	No	00h
PWM BaseF45	2Ch	—	—	—	—	PMB51	PMB50	PMB41	PMB40	No	00h
PWM BaseF123	2Dh	—	—	PMB31	PMB30	PMB21	PMB20	PMB11	PMB10	No	00h
Fan 1 Setting	30h	F1SP7	F1SP6	F1SP5	F1SP4	F1SP3	F1SP2	F1SP1	F1SP0	No	00h
PWM 1 Divide	31h	PM1D7	PM1D6	PM1D5	PM1D4	PM1D3	PM1D2	PM1D1	PM1D0	No	01h
Fan 1 Configuration 1	32h	ENAG1	RNG11	RNG10	EDG11	EDG10	UDT12	UDT11	UDT10	No	2Bh
Fan 1 Configuration 2	33h	—	ENRC1	GHEN1	DPT11	DPT10	ERG11	ERG10	—	SWL	28h
Gain 1	35h	—	—	GDE11	GDE10	GIN11	GIN10	GPR11	GPR10	SWL	2Ah
Fan 1 Spin Up Configuration	36h	DFC11	DFC10	NKCK1	SPLV12	SPLV11	SPLV10	SPT11	SPT10	SWL	19h
Fan 1 Max Step	37h	—	—	F1MS5	F1MS4	F1MS3	F1MS2	F1MS1	F1MS0	SWL	10h
Fan 1 Minimum Drive	38h	F1MN7	F1MN6	F1MN5	F1MN4	F1MN3	F1MN2	F1MN1	F1MN0	SWL	66h (40%)
Fan 1 Valid TACH Count	39h	F1VT7	F1VT6	F1VT5	F1VT4	F1VT3	F1VT2	F1VT1	F1VT0	SWL	F5h
Fan 1 Drive Fail Band Low Byte	3Ah	F1DF4	F1DF3	F1DF2	F1DF1	F1DF0	—	—	—	SWL	00h
Fan 1 Drive Fail Band High Byte	3Bh	F1DF12	F1DF11	F1DF10	F1DF9	F1DF8	F1DF7	F1DF6	F1DF5	SWL	00h
TACH 1 Target Low Byte	3Ch	F1TT4	F1TT3	F1TT2	F1TT1	F1TT0	—	—	—	No	F8h
TACH 1 Target High Byte	3Dh	F1TT12	F1TT11	F1TT10	F1TT9	F1TT8	F1TT7	F1TT6	F1TT5	No	FFh
TACH 1 Reading High Byte	3Eh	F1TR12	F1TR11	F1TR10	F1TR9	F1TR8	F1TR7	F1TR6	F1TR5	No	FFh
TACH 1 Reading Low Byte	3Fh	F1TR4	F1TR3	F1TR2	F1TR1	F1TR0	—	—	—	No	F8h
Fan 2 Setting	40h	F2SP7	F2SP6	F2SP5	F2SP4	F2SP3	F2SP2	F2SP1	F2SP0	No	00h
PWM 2 Divide	41h	PM2D7	PM2D6	PM2D5	PM2D4	PM2D3	PM2D2	PM2D1	PM2D0	No	01h

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Lock	POR Value
Fan 2 Configuration 1	42h	ENAG2	RNG21	RNG20	EDG21	EDG20	UDT22	UDT21	UDT20	No	2Bh
Fan 2 Configuration 2	43h	—	ENRC2	GHEN2	DPT21	DPT20	ERG21	ERG20	—	SWL	28h
Gain 2	45h	—	—	GDE21	GDE20	GIN21	GIN20	GPR21	GPR20	SWL	2Ah
Fan 2 Spin Up Configuration	46h	DFC21	DFC20	NKCK2	SPLV22	SPLV21	SPLV20	SPT21	SPT20	SWL	19h
Fan 2 Max Step	47h	—	—	F2MS5	F2MS4	F2MS3	F2MS2	F2MS1	F2MS0	SWL	10h
Fan 2 Minimum Drive	48h	F2MN7	F2MN6	F2MN5	F2MN4	F2MN3	F2MN2	F2MN1	F2MN0	SWL	66h (40%)
Fan 2 Valid TACH Count	49h	F2VT7	F2VT6	F2VT5	F2VT4	F2VT3	F2VT2	F2VT1	F2VT0	SWL	F5h
Fan 2 Drive Fail Band Low Byte	4Ah	F2DF4	F2DF3	F2DF2	F2DF1	F2DF0	—	—	—	SWL	00h
Fan 2 Drive Fail Band High Byte	4Bh	F2DF12	F2DF11	F2DF10	F2DF9	F2DF8	F2DF7	F2DF6	F2DF5	SWL	00h
TACH 2 Target Low Byte	4Ch	F2TT4	F2TT3	F2TT2	F2TT1	F2TT0	—	—	—	No	F8
TACH 2 Target High Byte	4Dh	F2TT12	F2TT11	F2TT10	F2TT9	F2TT8	F2TT7	F2TT6	F2TT5	No	FFh
TACH 2 Reading High Byte	4Eh	F2TR12	F2TR11	F2TR10	F2TR9	F2TR8	F2TR7	F2TR6	F2TR5	No	FFh
TACH 2 Reading low Byte	4Fh	F2TR4	F2TR3	F2TR2	F2TR1	F2TR0	—	—	—	No	F8h
Fan 3 Setting	50h	F3SP7	F3SP6	F3SP5	F3SP4	F3SP3	F3SP2	F3SP1	F3SP0	No	00h
PWM 3 Divide	51h	PM3D7	PM3D6	PM3D5	PM3D4	PM3D3	PM3D2	PM3D1	PM3D0	No	01h
Fan 3 Configuration 1	52h	ENAG3	RNG31	RNG30	EDG31	EDG30	UDT32	UDT31	UDT30	No	2Bh
Fan 3 Configuration 2	53h	—	ENRC3	GHEN3	DPT34	DPT30	ERG31	ERG30	—	SWL	28h
Gain 3	55h	—	—	GDE31	GDE30	GIN31	GIN30	GPR31	GPR30	SWL	2Ah
Fan 3 Spin Up Configuration	56h	DFC31	DFC30	NKCK3	SPLV32	SPLV31	SPLV30	SPT31	SPT30	SWL	19h
Fan 3 Max Step	57h	—	—	F3MS5	F3MS4	F3MS3	F3MS2	F3MS1	F3MS0	SWL	10h
Fan 3 Minimum Drive	58h	F3MN7	F3MN6	F3MN5	F3MN4	F3MN3	F3MN2	F3MN1	F3MN0	SWL	66h (40%)
Fan 3 Valid TACH Count	59h	F3VT7	F3VT6	F3VT5	F3VT4	F3VT3	F3VT2	F3VT1	F3VT0	SWL	F5h
Fan 3 Drive Fail Band Low Byte	5Ah	F3DF4	F3DF3	F3DF2	F3DF1	F3DF0	—	—	—	SWL	00h
Fan 3 Drive Fail Band High Byte	5Bh	F3DF12	F3DF11	F3DF10	F3DF9	F3DF8	F3DF7	F3DF6	F3DF5	SWL	00h
TACH 3 Target Low Byte	5Ch	F3TT4	F3TT3	F3TT2	F3TT1	F3TT0	—	—	—	No	F8h
TACH 3 Target High Byte	5Dh	F3TT12	F3TT11	F3TT10	F3TT9	F3TT8	F3TT7	F3TT6	F3TT5	No	FFh

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Lock	POR Value
TACH 3 Reading High Byte	5Eh	F3TR12	F3TR11	F3TR10	F3TR9	F3TR8	F3TR7	F3TR6	F3TR5	No	FFh
TACH 3 Reading Low Byte	5Fh	F3TR4	F3TR3	F3TR2	F3TR1	F3TR0	—	—	—	No	F8h
Fan 4 Setting	60h	F4SP7	F4SP6	F4SP5	F4SP4	F4SP3	F4SP2	F4SP1	F4SP0	No	00h
PWM 4 Divide	61h	PM4D7	PM4D6	PM4D5	PM4D4	PM4D3	PM4D2	PM4D1	PM4D0	No	01h
Fan 4 Configuration 1	62h	ENAG4	RNG41	RNG40	EDG41	EDG40	UDT42	UDT41	UDT40	No	2Bh
Fan 4 Configuration 2	63h	—	ENRC4	GHEN4	DPT41	DPT40	ERG41	ERG40	—	SWL	28h
Gain 4	65h	—	—	GDE41	GDE40	GIN41	GIN40	GPR41	GPR40	SWL	2Ah
Fan 4 Spin Up Configuration	66h	DFC41	DFC40	NKCK4	SPLV42	SPLV41	SPLV40	SPT41	SPT40	SWL	19h
Fan 4 Max Step	67h	—	—	F4MS5	F4MS4	F4MS3	F4MS2	F4MS1	F4MS0	SWL	10h
Fan 4 Minimum Drive	68h	F4MN7	F4MN6	F4MN5	F4MN4	F4MN3	F4MN2	F4MN1	F4MN0	SWL	66h (40%)
Fan 4 Valid TACH Count	69h	F4VT7	F4VT6	F4VT5	F4VT4	F4VT3	F4VT2	F4VT1	F4VT0	SWL	F5h
Fan 4 Drive Fail Band Low Byte	6Ah	F4DF4	F4DF3	F4DF2	F4DF1	F4DF0	—	—	—	SWL	00h
Fan 4 Drive Fail Band High Byte	6Bh	F4DF12	F4DF11	F4DF10	F4DF9	F4DF8	F4DF7	F4DF6	F4DF5	SWL	00h
TACH 4 Target Low Byte	6Ch	F4TT4	F4TT3	F4TT2	F4TT1	F4TT0	—	—	—	No	F8h
TACH 4 Target High Byte	6Dh	F4TT12	F4TT11	F4TT10	F4TT9	F4TT8	F4TT7	F4TT6	F4TT5	No	FFh
TACH 4 Reading High Byte	6Eh	F4TR12	F4TR11	F4TR10	F4TR9	F4TR8	F4TR7	F4TR6	F4TR5	No	FFh
TACH 4 Reading Low Byte	6Fh	F4TR4	F4TR3	F4TR2	F4TR1	F4TR0	—	—	—	No	F8h
Fan 5 Setting	70h	F5SP7	F5SP6	F5SP5	F5SP4	F5SP3	F5SP2	F5SP1	F5SP0	No	00h
PWM 5 Divide	71h	PM5D7	PM5D6	PM5D5	PM5D4	PM5D3	PM5D2	PM5D1	PM5D0	No	01h
Fan 5 Configuration 1	72h	ENAG5	RNG51	RNG50	EDG51	EDG50	UDT52	UDT51	UDT50	No	2Bh
Fan 5 Configuration 2	73h	—	ENRC5	GHEN5	DPT51	DPT50	ERG51	ERG50	—	SWL	28h
Gain 5	75h	—	—	GDE51	GDE50	GIN51	GIN50	GPR51	GPR50	SWL	2Ah
Fan 5 Spin Up Configuration	76h	DFC51	DFC50	NKCK5	SPLV52	SPLV51	SPLV50	SPT51	SPT50	SWL	19h
Fan 5 Max Step	77h	—	—	F5MS5	F5MS4	F5MS3	F5MS2	F5MS1	F5MS0	SWL	10h
Fan 5 Minimum Drive	78h	F5MN7	F5MN6	F5MN5	F5MN4	F5MN3	F5MN2	F5MN1	F5MN0	SWL	66h (40%)
Fan 5 Valid TACH Count	79h	F5VT7	F5VT6	F5VT5	F5VT4	F5VT3	F5VT2	F5VT1	F5VT0	SWL	F5h

TABLE 6-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Lock	POR Value
Fan 5 Drive Fail Band Low Byte	7Ah	F5DF4	F5DF3	F5DF2	F5DF1	F5DF0	—	—	—	SWL	00h
Fan 5 Drive Fail Band High Byte	7Bh	F5DF12	F5DF11	F5DF10	F5DF9	F5DF8	F5DF7	F5DF6	F5DF5	SWL	00h
TACH 5 Target Low Byte	7Ch	F5TT4	F5TT3	F5TT2	F5TT1	F5TT0	—	—	—	No	F8h
TACH 5 Target High Byte	7Dh	F5TT12	F5TT11	F5TT10	F5TT9	F5TT8	F5TT7	F5TT6	F5TT5	No	FFh
TACH 5 Reading High Byte	7Eh	F5TR12	F5TR11	F5TR10	F5TR9	F5TR8	F5TR7	F5TR6	F5TR5	No	FFh
TACH 5 Reading Low Byte	7Fh	F5TR4	F5TR3	F5TR2	F5TR1	F5TR0	—	—	—	No	F8h
Software Lock	EFh	—	—	—	—	—	—	—	LOCK	No	F8h
Product Features (EMC2305 and EMC2303 only)	FCh	—	—	ADR2	ADR1	ADR0	FSP2	FSP1	FSP0	No	00h
Product ID (EMC2305)	FDh	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	No	34h
Product ID (EMC2303)	FDh	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	No	35h
Product ID (EMC2302)	FDh	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	No	36h
Product ID (EMC2301)	FDh	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0	No	37h
Manufacturer ID	FEh	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	No	5Dh
Revision	FFh	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	No	80h

6.1 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

During Power-on Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the V_{DD} supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

The Lock column in Table 6-1 describes the locking mechanism, if any, used for individual registers. All SWL registers are Software Locked and therefore made read-only when the LOCK bit is set.

6.2 Configuration Register

The Configuration register controls the basic functionality of the EMC2301/2/3/5. The Configuration Register is software locked.

REGISTER 6-1: CONFIG - CONFIGURATION REGISTER (ADDRESS 20H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MASK	DIS_TO	WD_EN	—	—	—	DRECK	USECK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MASK:** Blocks the $\overline{\text{ALERT}}$ pin from being asserted
- 1 = The $\overline{\text{ALERT}}$ pin is masked and will not be asserted.
- 0 = The $\overline{\text{ALERT}}$ pin is unmasked. If any bit in the status registers is set, the $\overline{\text{ALERT}}$ pin will be asserted (unless individually masked via the Fan Interrupt Enable Register).

bit 6 **DIS_TO:** Disables the SMBus Time-Out function for the SMBus client (if enabled)
- 1 = The SMBus Time-Out function is disabled, allowing the device to be fully I^2C compatible.
- 0 = The SMBus Time-Out function is enabled.

bit 5 **WD_EN:** Enables the Watchdog Timer (see **Section 4.11 "Watchdog Timer"**) to operate in Continuous Mode
- 1 = The Watchdog Timer operates continuously.
- 0 = The Watchdog Timer does not operate continuously. It will function upon power-up and at no other time.

bit 4-2 Unimplemented bits, read as '0'.

bit 1 **DRECK:** Enables the internal tachometer clock to be driven out on the CLK pin so that multiple devices can be synced to the same source
- 1 = The CLK pin acts as a clock output and is a push-pull driver.
- 0 = The CLK pin acts as a clock input.

bit 0 **USECK:** Enables the EMC2301/2/3/5 to use a clock present on the CLK pin as the tachometer clock. If the DR_EXT_CLK bit is set, then this bit is ignored and the device will use the internal oscillator.
- 1 = The EMC2301/2/3/5 will use the oscillator presented on the CLK pin for all tachometer measurements.
- 0 = The EMC2301/2/3/5 will use its internal oscillator for all tachometer measurements.

6.3 Fan Status Register

The Fan Status register indicates that the fan driver has stalled or failed or that the Watchdog Timer has expired (see **Section 4.11 "Watchdog Timer"**).

REGISTER 6-2: FAN STATUS - FAN STATUS REGISTER (ADDRESS 24H)

RC-0	U-0	U-0	U-0	U-0	RC-0	RC-0	RC-0
WATCH	—	—	—	—	DVFAIL	FNSPIN	FNSTL
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **WATCH:** Indicates that the Watchdog Timer has expired. When this bit is set, each fan is driven to 100% duty cycle and will remain at 100% duty cycle until they are programmed. This bit is cleared when it is read.
1 = Watchdog Timer has expired.
0 = Watchdog Timer has not expired.

bit 6-3 Unimplemented bits, read as '0'.

bit 2 **DVFAIL:** Indicates that one or more fan drivers cannot meet the programmed fan speed at maximum PWM duty cycle.
1 = Any bit in the Fan Drive Fail Status register (Register 6-5) is set
0 = All bits in Fan Drive Fail Status register are cleared.

bit 1 **FNSPIN:** Indicates that one or more fan drivers cannot spin up.
1 = This bit is set when any bit in the Fan Spin Status register (Register 6-4) is set.
0 = All bits in the Fan Spin Status register are cleared.

bit 0 **FNSTL:** Indicates that one or more fan drivers have stalled.
1 = Any bit in the Fan Stall Status register (Register 6-3) is set.
0 = All bits in the Fan Stall register are cleared.

6.4 Fan Stall Status Register

The Fan Stall Status register indicates which fan driver has detected a stalled condition (see **Section 4.4.3 "Stalled Fan"**). All bits are cleared upon a read if the Error condition has been removed.

REGISTER 6-3: FAN STALL STATUS - FAN STALL STATUS REGISTER (ADDRESS 25H)

U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0	RC-0
—	—	—	F5STL	F4STL	F3STL	F2STL	F1STL
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented bits, read as '0'.

bit 4 **F5STL:** Fan 5 Stall Status
1 = Fan 5 tachometer count has exceeded maximum valid TACH count, indicating stall.
0 = Fan 5 Stall has not been detected.

REGISTER 6-3: FAN STALL STATUS - FAN STALL STATUS REGISTER (ADDRESS 25H)

bit 3 **F4STL:** Fan 4 Stall Status
1 = Fan 4 tachometer count has exceeded maximum valid TACH count, indicating stall.
0 = Fan 4 Stall has not been detected.

bit 2 **F3STL:** Fan 3 Stall Status
1 = Fan 3 tachometer count has exceeded maximum valid TACH count, indicating stall.
0 = Fan 3 Stall has not been detected.

bit 1 **F2STL:** Fan 2 Stall Status
1 = Fan 2 tachometer count has exceeded maximum valid TACH count, indicating stall.
0 = Fan 2 Stall has not been detected.

bit 0 **F1STL:** Fan 1 Stall Status
1 = Fan 1 tachometer count has exceeded maximum valid TACH count, indicating stall.
0 = Fan 1 Stall has not been detected.

6.5 Fan Spin Status Register

The Fan Spin Status register indicates which fan driver has failed to spin-up (see **Section 4.8 "Spin Up Routine"**). All bits are cleared upon a read if the Error condition has been removed.

REGISTER 6-4: FAN SPIN STATUS - FAN SPIN-UP STATUS REGISTER (ADDRESS 26H)

U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0	RC-0
—	—	—	F5SPIN	F4SPIN	F3SPIN	F2SPIN	F1SPIN
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented bits, read as '0'.

bit 4 **F5SPIN:** Fan 5 Spin-Up Status
1 = Fan 5 spin-up routine failed to start the fan.
0 = Fan 5 spin-up routine successful.

bit 3 **F4SPIN:** Fan 4 Spin-Up Status
1 = Fan 4 spin-up routine failed to start the fan.
0 = Fan 4 spin-up routine successful.

bit 2 **F3SPIN:** Fan 3 Spin-Up Status
1 = Fan 3 spin-up routine failed to start the fan.
0 = Fan 3 spin-up routine successful.

bit 1 **F2SPIN:** Fan 2 Spin-Up Status
1 = Fan 2 spin-up routine failed to start the fan.
0 = Fan 2 spin-up routine successful.

bit 0 **F1SPIN:** Fan 1 Spin-Up Status
1 = Fan 1 spin-up routine failed to start the fan.
0 = Fan 1 spin-up routine successful.

6.6 Fan Drive Fail Status Register

The Fan Drive Fail Status register indicates which fan driver cannot drive to the programmed speed even at 100% duty cycle (see **Section 4.4.4 "Aging Fan or Invalid Drive Detection"** and Register 6-16). All bits are cleared upon a read if the Error condition has been removed.

REGISTER 6-5: DRIVE FAIL STATUS - FAN DRIVE FAIL STATUS REGISTER (ADDRESS 27H)

U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0	RC-0
—	—	—	DRVF5	DRVF4	DRVF3	DRVF2	DRVF1
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented bits, read as '0'.

bit 4 **DRVF5:** Drive Fail Fan 5 Status
1 = Fan 5 is unable to reach the commanded RPM with 100% PWM input.
0 = Fan 5 is within limits of commanded RPM.

bit 3 **DRVF4:** Drive Fail Fan 4 Status
1 = Fan 4 is unable to reach the commanded RPM with 100% PWM input.
0 = Fan 4 is within limits of commanded RPM.

bit 2 **DRVF3:** Drive Fail Fan 3 Status
1 = Fan 3 is unable to reach the commanded RPM with 100% PWM input.
0 = Fan 3 is within limits of commanded RPM.

bit 1 **DRVF2:** Drive Fail Fan 2 Status
1 = Fan 2 is unable to reach the commanded RPM with 100% PWM input.
0 = Fan 2 is within limits of commanded RPM.

bit 0 **DRVF1:** Drive Fail Fan 1 Status
1 = Fan 1 is unable to reach the commanded RPM with 100% PWM input.
0 = Fan 1 is within limits of commanded RPM.

6.7 Fan Interrupt Enable Register

The Fan Interrupt Enable register controls the masking for each fan channel. When a channel is enabled, it will cause the $\overline{\text{ALERT}}$ pin to be asserted when an Error condition is detected.

- '1' - An Error condition (Stall, Spin Up, Drive Fail) on fan X will cause the $\overline{\text{ALERT}}$ pin to be asserted.
- '0' (default) - An Error condition on fan X will not cause the $\overline{\text{ALERT}}$ pin to be asserted; however, the status registers will be updated normally.

REGISTER 6-6: FAN INTERRUPT ENABLE - FAN INTERRUPT ENABLE REGISTER (ADDRESS 29H)

U-0	U-0	U-0	RW-0	RW-0	RW-0	RW-0	RW-0
—	—	—	F5ITEN	F4ITEN	F3ITEN	F2ITEN	F1ITEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented bits, read as '0'.

bit 4 **F5ITEN:** Fan 5 Interrupt Enable. Allows Fan 5 to assert the $\overline{\text{ALERT}}$ pin if an error condition is detected
1 = Fan 5 has an Error condition.
0 = Fan 5 is operating within limits.

bit 3 **F4ITEN:** Fan 4 Interrupt Enable. Allows Fan 4 to assert the $\overline{\text{ALERT}}$ pin if an error condition is detected
1 = Fan 4 has an Error condition.
0 = Fan 4 is operating within limits.

bit 2 **F3ITEN:** Fan 3 Interrupt Enable. Allows Fan 3 to assert the $\overline{\text{ALERT}}$ pin if an error condition is detected
1 = Fan 3 has an Error condition.
0 = Fan 3 is operating within limits.

bit 1 **F2ITEN:** Fan 2 Interrupt Enable. Allows Fan 2 to assert the $\overline{\text{ALERT}}$ pin if an error condition is detected
1 = Fan 2 has an Error condition.
0 = Fan 2 is operating within limits.

bit 0 **F1ITEN:** Fan 1 Interrupt Enable. Allows Fan 1 to assert the $\overline{\text{ALERT}}$ pin if an error condition is detected
1 = Fan 1 has an Error condition.
0 = Fan 1 is operating within limits.

6.8 PWM Polarity Configuration Registers

The PWM Polarity Configuration registers control the output type and polarity of all PWM outputs.

REGISTER 6-7: PWM POLARITY CONFIG - PWM POLARITY CONFIGURATION REGISTER (ADDRESS 2AH)

U-0	U-0	U-0	RW-0	RW-0	RW-0	RW-0	RW-0
—	—	—	PLRITY5	PLRITY4	PLRITY3	PLRITY2	PLRITY1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented bits, read as '0'.

bit 4 **PLRITY5:** Sets the PWM output polarity
1 = PWM 5 drive setting of 00h produces 100% duty cycle, drive setting of FFh produces 0% duty cycle.
0 = PWM 5 drive setting of 00h produces 0% duty cycle, drive setting of FFh produces 100% duty cycle.

bit 3 **PLRITY4:** Sets the PWM output polarity
1 = PWM 4 drive setting of 00h produces 100% duty cycle, drive setting of FFh produces 0% duty cycle.
0 = PWM 4 drive setting of 00h produces 0% duty cycle, drive setting of FFh produces 100% duty cycle.

bit 2 **PLRITY3:** Sets the PWM output polarity
1 = PWM 3 drive setting of 00h produces 100% duty cycle, drive setting of FFh produces 0% duty cycle.
0 = PWM 3 drive setting of 00h produces 0% duty cycle, drive setting of FFh produces 100% duty cycle.

bit 1 **PLRITY2:** Sets the PWM output polarity
1 = PWM 2 drive setting of 00h produces 100% duty cycle, drive setting of FFh produces 0% duty cycle.
0 = PWM 2 drive setting of 00h produces 0% duty cycle, drive setting of FFh produces 100% duty cycle.

bit 0 **PLRITY1:** Sets the PWM output polarity
1 = PWM 1 drive setting of 00h produces 100% duty cycle, drive setting of FFh produces 0% duty cycle.
0 = PWM 1 drive setting of 00h produces 0% duty cycle, drive setting of FFh produces 100% duty cycle.

6.9 PWM Output Configuration Register

The PWM Output Configuration register controls the PWM output type as push-pull or open drain.

REGISTER 6-8: PWM OUTPUT CONFIG - PWM OUTPUT CONFIGURATION REGISTER (ADDRESS 2BH)

U-0	U-0	U-0	RW-0	RW-0	RW-0	RW-0	RW-0
—	—	—	PMOT5	PMOT4	PMOT3	PMOT2	PMOT1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented bits, read as '0'.

bit 4 **PMOT5:** Sets the PWM output type
1 = PWM 5 drive is push-pull type.
0 = PWM 5 drive is open drain type.

bit 3 **PMOT4:** Sets the PWM output type
1 = PWM 4 drive is push-pull type.
0 = PWM 4 drive is open drain type.

bit 2 **PMOT3:** Sets the PWM output type
1 = PWM 3 drive is push-pull type.
0 = PWM 3 drive is open drain type.

bit 1 **PMOT2:** Sets the PWM output type
1 = PWM 2 drive is push-pull type.
0 = PWM 2 drive is open drain type.

bit 0 **PMOT1:** Sets the PWM output type
1 = PWM 1 drive is push-pull type.
0 = PWM 1 drive is open drain type.

6.10 PWM BaseF45 Register

The PWM BASEF45 Register controls the base frequency of PWM drivers 4 and 5.

REGISTER 6-9: PWM BASEF45 - PWM 4 AND 5 BASE FREQUENCY CONFIGURATION REGISTER (ADDRESS 2CH)

U-0	U-0	U-0	U-0	RW-0	RW-0	RW-0	RW-0
—	—	—	—	PMB5[1:0]		PMB4[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 Unimplemented bits, read as '0'.

bit 3-2 **PMB5[1:0]:** Sets the PWM5 base frequency
11 = PWM 5 base is 2.441 kHz.
10 = PWM 5 base is 4.882 kHz.
01 = PWM 5 base is 19.53 kHz.
00 = PWM 5 base is 26.00 kHz.

bit 1-0 **PMB4[1:0]:** Sets the PWM4 base frequency
11 = PWM 4 base is 2.441 kHz.
10 = PWM 4 base is 4.882 kHz.
01 = PWM 4 base is 19.53 kHz.
00 = PWM 4 base is 26.00 kHz.

6.11 PWM BaseF123 Register

The PWM BaseF123 Register controls the base frequency of PWM drivers 1, 2 and 3.

REGISTER 6-10: PWM BASEF123 - PWM 1, 2 AND 3 BASE FREQUENCY CONFIGURATION REGISTER (ADDRESS 2DH)

U-0	U-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
—	—	PMB3[1:0]		PMB2[1:0]		PMB1[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented bits, read as '0'.

bit 5-4 **PMB3[1:0]:** Sets the PWM3 base frequency
11 = PWM 3 base is 2.441 kHz.
10 = PWM 3 base is 4.882 kHz.
01 = PWM 3 base is 19.53 kHz.
00 = PWM 3 base is 26.00 kHz.

bit 3-2 **PMB2[1:0]:** Sets the PWM2 base frequency
11 = PWM 2 base is 2.441 kHz.
10 = PWM 2 base is 4.882 kHz.
01 = PWM 2 base is 19.53 kHz.
00 = PWM 2 base is 26.00 kHz.

REGISTER 6-10: PWM BASEF123 - PWM 1, 2 AND 3 BASE FREQUENCY CONFIGURATION REGISTER (ADDRESS 2DH) (CONTINUED)

bit 1-0 **PMB1[1:0]:** Sets the PWM1 base frequency
11 = PWM 1 base is 2.441 kHz.
10 = PWM 1 base is 4.882 kHz.
01 = PWM 1 base is 19.53 kHz.
00 = PWM 1 base is 26.00 kHz.

6.12 Fan Drive Setting Register

The Fan Drive Setting register always displays the current setting of the respective fan driver. Reading from any of the registers will report the current fan speed setting of the appropriate fan driver regardless of the operating mode. Therefore it is possible that reading from this register will not report data that was previously written into this register.

While the RPM-based Fan Speed Control algorithm is active, this register is read-only. Writing to the register will have no effect and the data will not be stored. The contents of the register represent the weighting of each bit in determining the final output voltage.

REGISTER 6-11: FAN DRIVE SETTING - FAN DRIVE SETTING REGISTER (ADDRESSES 30H, 40H, 50H, 60H, 70H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
FxSP[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **FxSP]7:0]:** Fan Speed Setting, where "x" represents PWM1 through 5 based on device features. PWM duty cycle is calculated in Equation 4-1.

6.13 PWM Divide Registers

The PWM Divide registers determine the final frequency of the respective PWM Fan Driver. Each driver base frequency is divided by the value of the respective PWM Divide Register to determine the final frequency. The duty cycle settings are not affected by these settings, only the final frequency of the PWM driver. A value of 00h will be decoded as 01h. The contents of the register represent the weighting of each bit in determining the final output voltage.

REGISTER 6-12: PWM X DIVIDE - PWMX FREQUENCY DIVIDE REGISTER (ADDRESSES 31H, 41H, 51H, 61H, 71H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
PWMxD[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PWMxD]7:0]:** PWM Frequency Divide value, where "x" represents PWM1 through 5 based on device features.

6.14 Fan Configuration Registers

The Fan Configuration registers control the general operation of the RPM-based Fan Speed Control algorithm used for the respective Fan Driver (see **Section 4.3 "RPM-Based Fan Speed Control Algorithm"**).

REGISTER 6-13: FAN CONFIG - FAN CONFIGURATION REGISTERS (ADDRESSES 32H, 42H, 52H, 62H, 72H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
ENAGx	RNGx[1:0]		EDGx[1:0]		UDTx[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ENAGx:** Enable Closed Loop algorithm, where "x" is 1 to 5, depending on device features
1 = Closed Loop algorithm "x" is enabled. Changes to Fan Setting register are ignored.
0 = Closed Loop algorithm "x" is disabled, and device is placed in Direct Setting mode (see **Section 4.1 "Fan Control Modes of Operation"**). Changes to the Fan Setting register will change the PWM Duty Cycle.

bit 6-5 **RNGx[1:0]:** Range. Sets the minimum fan speed measured and reported, where "x" is 1 to 5, depending on device features.
11 = 4000 RPM minimum, TACH count multiplier = 8.
10 = 2000 RPM minimum, TACH count multiplier = 4.
01 = 1000 RPM minimum, TACH count multiplier = 2.
00 = 500 RPM minimum, TACH count multiplier = 1.

REGISTER 6-13: FAN CONFIG - FAN CONFIGURATION REGISTERS (ADDRESSES 32H, 42H, 52H, 62H, 72H) (CONTINUED)

bit 4-3 **EDGx[1:0]:** Edges. Sets the number of edges to sample when calculating RPM, where "x" is 1 to 5, depending on device features.
11 = 9 edges sampled (4 poles) - effective Tach multiplier is 2, based on two pole fans
10 = 7 edges sampled (3 poles) - effective Tach multiplier is 1.5, based on two pole fans
01 = 5 edges sampled (2 poles) - effective Tach multiplier is 1, based on two pole fans
00 = 3 edges sampled (1 pole) - effective Tach multiplier is 0.5, based on two pole fans

bit 2-0 **UDTx[2:0]:** Update Time. Sets the PID update rate for closed loop control, where "x" is 1 to 5, depending on device features. The Update Time, along with the Fan Step register, is used to control the ramp rate of the drive response to provide a cleaner transition of the actual fan operation as the desired fan speed changes.
111 = 1600 ms update interval
110 = 1200 ms update interval
101 = 800 ms update interval
100 = 500 ms update interval
011 = 400 ms update interval
010 = 300 ms update interval
001 = 200 ms update interval
000 = 100 ms update interval

Note: Increasing the number of edges measured with respect to the number of poles of the fan will cause the TACH Reading registers to indicate a fan speed that is higher or lower than the actual speed. In order for the FSC algorithm to operate correctly, the TACH Target must be updated by the user to accommodate this shift. The Effective Tach Multiplier is used as a direct multiplier term that is applied to the Actual RPM to achieve the Reported RPM. It should only be applied if the number of edges measured does not match the number of edges expected based on the number of poles of the fan (which is fixed for any given fan). Contact Microchip for recommended settings when using fans with more or fewer than two poles.

6.15 Fan Configuration 2 Registers

The Fan Configuration 2 registers control the tachometer measurement and advanced features of the RPM-based Fan Speed Control algorithm (see **Section 4.3 "RPM-Based Fan Speed Control Algorithm"**).

REGISTER 6-14: FAN CONFIG 2 - FAN CONFIGURATION 2 REGISTERS (ADDRESSES 33H, 43H, 53H, 63H, 73H)

U-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	U-0
—	ENRCx	GHENx	DPTx[1:0]		ERGx[1:0]		—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 Unimplemented bit, read as '0'.

bit 6 **ENRCx:** Enable Ramp Rate Control, where "x" is 1 to 5, depending on device features. This is available only when ENAGx = 0.
1 = Ramp Rate Control enabled.
0 = Ramp Rate Control disabled.

bit 5 **GHENx:** Glitch Filter Enable. Enables the noise filter that removes high-frequency noise injected on the TACHx pin, where "x" is 1 to 5, depending on device features.
1 = Glitch filter enabled.
0 = Glitch filter disabled.

REGISTER 6-14: FAN CONFIG 2 - FAN CONFIGURATION 2 REGISTERS (ADDRESSES 33H, 43H, 53H, 63H, 73H) (CONTINUED)

bit 4-3 **DPTx[1:0]:** Derivative Options. Determines what form of derivative will be used in the Fan Speed Setting calculation (see **Section 4.3.3.1 "Selecting the Derivative Options"**).
11 = BOTH
10 = STEP
01 = BASIC
00 = NONE

bit 2-1 **ERGx[1:0]:** Error Window. Determines the range of the error window. When the measured fan speed is within the programmed error window around the target speed, then the fan drive setting is not updated. The algorithm will continue to monitor the fan speed and calculate necessary drive setting changes base on the error; however, these changes are ignored (see **Section 4.3.1 "Error Window"**). "X" is 1 to 5, depending on device features.
11 = 200 RPM
10 = 100 RPM
01 = 50 RPM
00 = 0 RPM

bit 0 Unimplemented bit, read as '0'.

6.16 PID Gain Register

See **Section 4.3.3.2 "Setting the PID Gains"**.

REGISTER 6-15: GAIN - PIDX GAIN REGISTER (ADDRESSES 35H, 45H, 55H, 65H, 75H)

U-0	U-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
—	—	GDEx[1:0]		GINx[1:0]		GPRx[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented bits, read as '0'.

bit 5-4 **GDEx[1:0]:** Derivative Gain, where "x" is 1 to 5, depending on device features. The effective gain applied to the KD in the PID equation.
11 = 8x
10 = 4x
01 = 2x
00 = 1x

bit 3-2 **GINx[1:0]:** Integral Gain, where "x" is 1 to 5, depending on device features. The effective gain applied to the KI in the PID equation.
11 = 8x
10 = 4x
01 = 2x
00 = 1x

bit 1-0 **GPRx[1:0]:** Proportional Gain, where "x" is 1 to 5, depending on device features. The effective gain applied to the KP in the PID equation.
11 = 8x
10 = 4x
01 = 2x
00 = 1x

6.17 Fan Spin Up Configuration Registers

The Fan Spin Up Configuration registers control the settings of the Spin Up Routine. These registers are software locked (see **Section 4.8 "Spin Up Routine"**).

REGISTER 6-16: FAN SPIN - SPIN-UP CONFIGURATION REGISTER (ADDRESSES 36H, 46H, 56H, 66H, 76H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
DFCx[1:0]		NKCKx	SPLVx[2:0]			SPTx[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **DFCx[1:0]:** Drive Fail Count, where "x" is 1 to 5, depending on device features. Determines when an aging fan has been detected.
11 = 64 update periods
10 = 32 update periods
01 = 16 update periods
00 = Disabled

bit 5 **NKCKx:** No Kick, where "x" is 1 to 5, depending on device features. Kick refers to the 100% drive for 1/4 of the spin-up time.
1 = Spin-Up will not drive to 100% PWM
0 = Spin-Up will drive to 100% PWM

bit 4-2 **SPLVx[2:0]:** Spin-Up Level, where "x" is 1 to 5, depending on device features. This is the level the spin-up routine will use.
111 = 65%
110 = 60%
101 = 55%
100 = 50%
011 = 45%
010 = 40%
001 = 35%
000 = 30%

bit 1-0 **SPTx[1:0]:** Spin-Up Time, where "x" is 1 to 5, depending on device features. This determines how long the spin-up routine will run before releasing the drive.
11 = 2s
10 = 1s
01 = 500 ms
00 = 250 ms

6.18 Maximum Step Size Register

This register determines the maximum step size for the ramp rate control (see **Section 4.3.3.3 "Fan Drive Max Step"** and **Section 4.10 "Ramp Rate Control"**).

The contents of the register represent the weighting of each bit in determining the final maximum step size for the ramp rate control.

REGISTER 6-17: MAX STEP - MAXIMUM STEP SIZE REGISTER (ADDRESSES 37H, 47H, 57H, 67H, 77H)

U-0	U-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
—	—	FxMS[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented bits, read as '0'.

bit 5-0 **FxMS[5:0]:** Fan Drive Max Step size, where "x" represents 1 through 5 based on device features.

6.19 Fan Minimum Drive Register

The Fan Minimum Drive Register (see **Section 4.3.3.4 "Minimum Drive Setting"**) stores the minimum drive setting for each RPM-based Fan Speed Control algorithm. The contents of the register represent the weighting of each bit in determining the final minimum fan driver setting.

REGISTER 6-18: MIN DRIVE - FAN SETTING DRIVE MINIMUM VALUE REGISTER (ADDRESSES 38H, 48H, 58H, 68H, 78H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
FxMS[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **FxMS[7:0]:** Fan Drive Min Step size, where "x" represents 1 through 5 based on device features.

6.20 Valid TACH Count Registers

The Valid TACH Count registers store the maximum TACH Reading register value to indicate that each fan is spinning properly (see **Section 4.4.2 "Valid Tachometer Readings"**). The contents of the register represent the weighting of each bit in determining the final Valid Tach count.

REGISTER 6-19: VALID TACH - MAXIMUM VALID TACH COUNTS REGISTER (ADDRESSES 39H, 49H, 59H, 69H, 79H)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
FxVT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0	**FxVT[7:0]:** Fan Drive Max Tach Counts, where "x" represents 1 through 5 based on device features.
bit 7	4096
bit 6	2048
bit 5	1024
bit 4	512
bit 3	256
bit 2	128
bit 1	64
bit 0	32

6.21 Drive Fail Band Registers

The Drive Fail Band registers store the number of tach counts used by the Fan Drive Fail detection circuitry. This circuitry is activated when the fan drive setting high byte is at FFh. When it is enabled, the actual measured fan speed is compared against the target fan speed. These registers are only used when the FSC algorithm is active.

This circuitry is used to indicate that the target fan speed at full drive is higher than the fan is actually capable of reaching. If the measured fan speed does not exceed the target fan speed minus the Fan Drive Fail Band register settings for a period of time longer than set by the DFCx[1:0] bits, then the DRIVE_FAIL status bit will be set and an interrupt generated (see **Section 4.4.4 "Aging Fan or Invalid Drive Detection"**). The contents of Register 6-20 and Register 6-21 represent the weighting of each bit in determining the final number of tach counts used by the Fan Drive Fail detection circuitry.

REGISTER 6-20: DRIVE FAIL - DRIVE FAIL BAND HIGH BYTE REGISTER (ADDRESSES 3BH, 4BH, 5BH, 6BH, 7BH)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
FxDF[12:5]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0	**FxDF[12:5]:** Drive Fail Band High Byte, where "x" represents 1 through 5 based on device features.
bit 7	4096
bit 6	2048
bit 5	1024
bit 4	512
bit 3	256
bit 2	128
bit 1	64
bit 0	32

REGISTER 6-21: DRIVE FAIL - DRIVE FAIL BAND LOW BYTE REGISTER (ADDRESSES 3AH, 4AH, 5AH, 6AH, 7AH)

RW-0	RW-0	RW-0	RW-0	RW-0	U-0	U-0	U-0
FxDF[4:0]					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3	**FxDF[5:0]:** Drive Fail Band Low Byte, where "x" represents 1 through 5 based on device features.
bit 7	16
bit 6	8
bit 5	4
bit 4	2
bit 3	1
bit 2-0	Unimplemented bits, read as '0'.

6.22 TACH Target Registers

The TACH Target Registers hold the target tachometer value that is maintained by the RPM-based Fan Speed Control algorithm.

The value in the TACH Target Registers will always reflect the current TACH Target value.

If one of the algorithms is enabled, setting the TACH Target Register to FFh will disable the fan driver (set the fan drive setting to 0%). Setting the TACH Target to any other value (from a setting of FFh) will cause the algorithm to invoke the Spin Up Routine after which it will function normally.

The Tach Target is not applied until the high byte is written. Once the high byte is written, the current value of both high and low bytes will be used as the next Tach target (see **Section 4.4 "Tachometer Measurement"**). The contents of Register and Register 6-22 represent the weighting of each bit in determining the final target tachometer value that is maintained by the RPM-based FSC algorithm.

TACH TARGET - TACHOMETER CLOSED LOOP TARGET HIGH BYTE REGISTER (ADDRESSES 3DH, 4DH, 5DH, 6DH, 7DH)

RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0
FxTT[12:5]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **FxTT[12:5]:** Fan Drive Tach Target Counts, where "x" represents 1 through 5 based on device features.

bit 7	4096
bit 6	2048
bit 5	1024
bit 4	512
bit 3	256
bit 2	128
bit 1	64
bit 0	32

REGISTER 6-22: TACH TARGET - TACHOMETER CLOSED LOOP TARGET LOW BYTE REGISTER (ADDRESSES 3CH, 4CH, 5CH, 6CH, 7CH)

RW-0	RW-0	RW-0	RW-0	RW-0	U-0	U-0	U-0
FxTT[4:0]					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3	**FxTT[4:0]:** Fan Drive Tach Target Counts, where "x" represents 1 through 5 based on device features.
bit 7	16
bit 6	8
bit 5	4
bit 4	2
bit 3	1
bit 2-0	Unimplemented bits, read as '0'.

6.23 TACH Reading Registers

The TACH Reading Registers describe the current tachometer reading for each of the fans (see **Section 4.4 "Tachometer Measurement"**). The contents of Register 6-24 and Register 6-25 represent the weighting of each bit in determining the current tachometer reading for each of the fans.

REGISTER 6-23: TACH READING - TACHOMETER READING HIGH BYTE REGISTER (ADDRESSES 3EH, 4EH, 5EH, 6EH, 7EH)

RW-0	RW-0	RW-0	RW-0	RW-0	U-0	U-0	U-0
FxTR[12:5]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **FxTR[12:5]:** Fan Drive Tach Reading Counts, where "x" represents 1 through 5 based on device features.

bit 7 4096
bit 6 2048
bit 5 1024
bit 4 512
bit 3 256
bit 2 128
bit 1 64
bit 0 32

REGISTER 6-24: TACH READING - TACHOMETER READING LOW BYTE REGISTER (ADDRESSES 3FH, 4FH, 5FH, 6FH, 7FH)

RW-0	RW-0	RW-0	RW-0	RW-0	U-0	U-0	U-0
FxTR[4:0]					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-3 **FxTR[12:5]:** Fan Drive Tach Reading Counts, where "x" represents 1 through 5 based on device features.

bit 7 16
bit 6 8
bit 5 4
bit 4 2
bit 3 1
bit 2-0 Unimplemented bit, read as '0'.

REGISTER 6-25: SOFTWARE LOCK - SOFTWARE LOCK REGISTER (ADDRESS EFH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	RW-0
—	—	—	—	—	—	—	LOCK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 Unimplemented bit, read as '0'.

bit 0 **LOCK:** Enables the SWL function
1 = All SWL registers are locked and read-only. Unlock occurs on power cycle.
0 = All SWL registers are writable.

REGISTER 6-26: PROD FEAT - EMC2303/5 PRODUCT FEATURES REGISTER (ADDRESS FCH)

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	ADR[2:0]			FSP[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented bit, read as '0'.

bit 5-3 **ADR[2:0]:** SMBus address determined by the ADDR_SEL pin decode.
101 = 1001_101(r/w)
100 = 1001_100(r/w)
011 = 0101_101(r/w)
010 = 0101_100(r/w)
001 = 0101_111(r/w)
000 = 0101_110(r/w)

bit 2-0 **FSP[2:0]:** Default Fan Speed determined by the CLK pin decode. This is conditional on ADDR_SEL.
100 = 100% PWM
011 = 75% PWM
010 = 50% PWM
001 = 30% PWM
000 = 0% PWM

REGISTER 6-27: PRODUCT ID - PRODUCT IDENTIFICATION REGISTER (ADDRESS FDH)

R-1	R-0	R-1	R-1	R-0	R-1	R-0	R-0
PID[7:2]						PID[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **PID[7:2]:** Product Identification Register. Hard coded fixed value of 0011_01b.

bit 1-0 **PID[1:0]:** Product Identification Register. Device defines bit pattern.
11 = EMC2301
10 = EMC2302
01 = EMC2303
00 = EMC2305

REGISTER 6-28: MFG ID - MANUFACTURER IDENTIFICATION REGISTER (ADDRESS FEH)

R-0	R-1	R-0	R-1	R-1	R-1	R-0	R-1
MID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MID[7:0]:** Manufacturer Identification Register. Hard coded fixed value of 5Dh.

REGISTER 6-29: REV - SILICON REVISION REGISTER (ADDRESS FFH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
REV[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

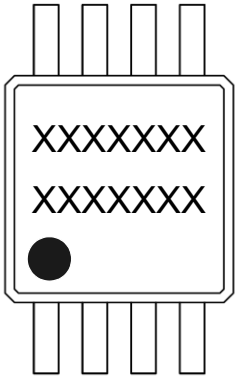
bit 7-0 **REV[7:0]:** Silicon Revision set to 80h.

7.0 PACKAGING SPECIFICATIONS

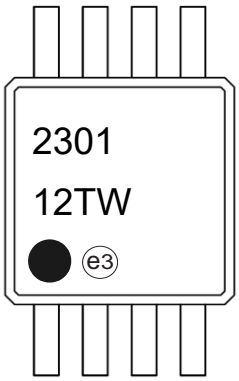
7.1 Package Marking Information

MSOP-8
(EMC2301)

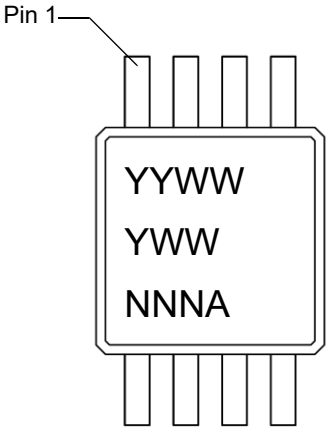
Front

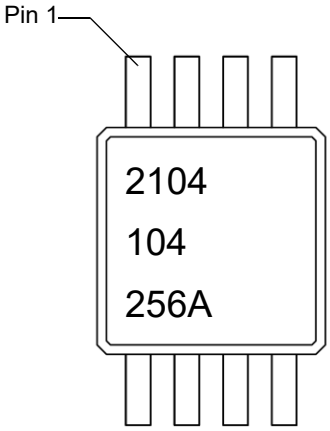


Example



Back





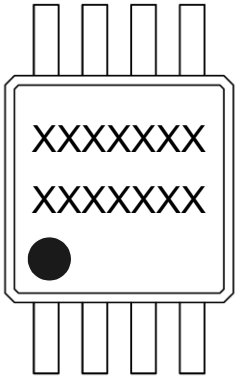
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

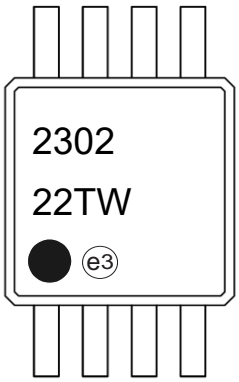
7.2 Package Marking Information (CONTINUED)

MSOP-10
(EMC2302)

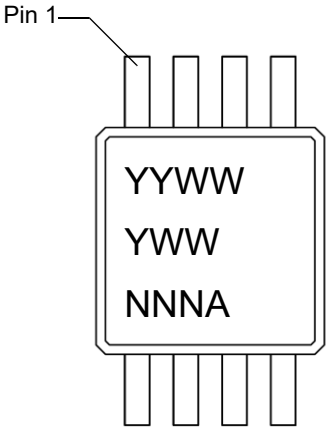
Front

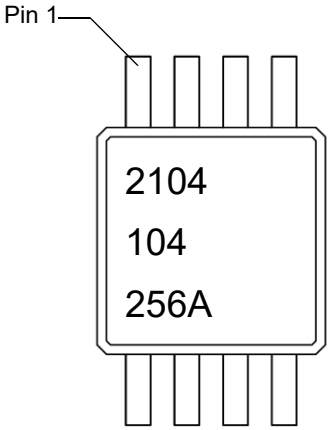


Example

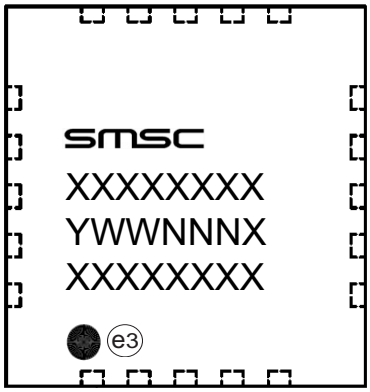


Back

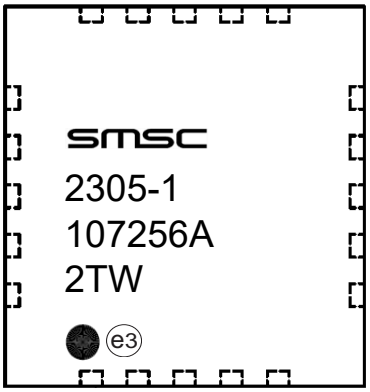




QFN-12 (EMC2303)
QFN-16 (EMC2305)

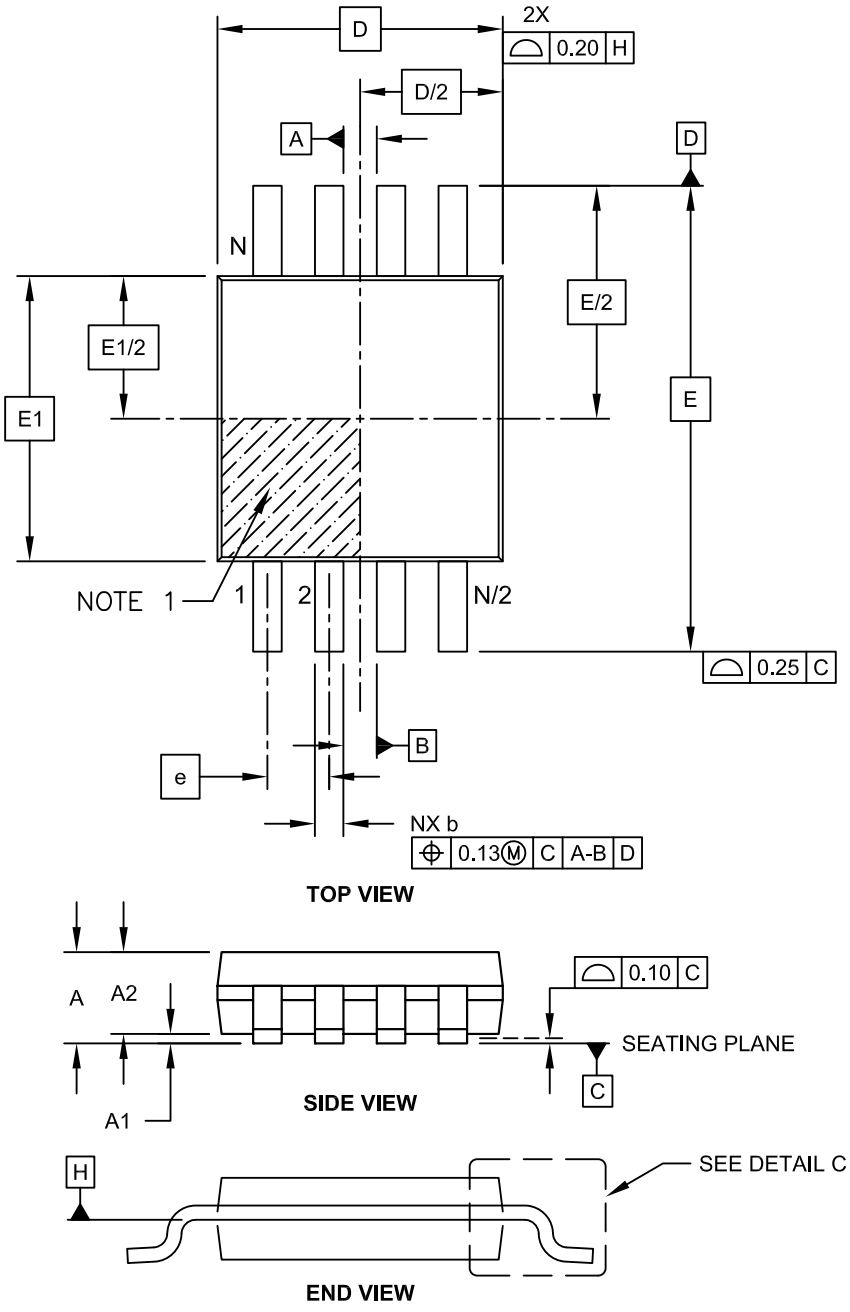


Example



8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

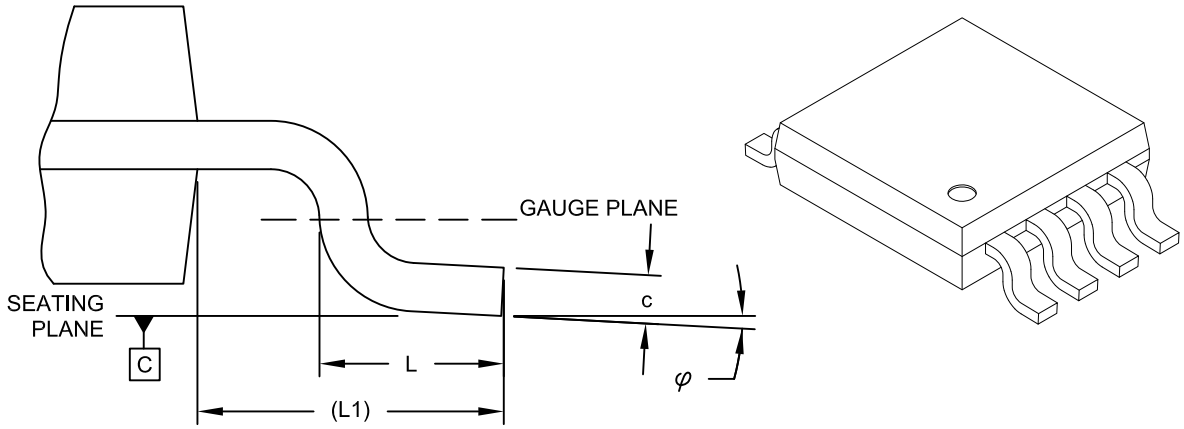
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

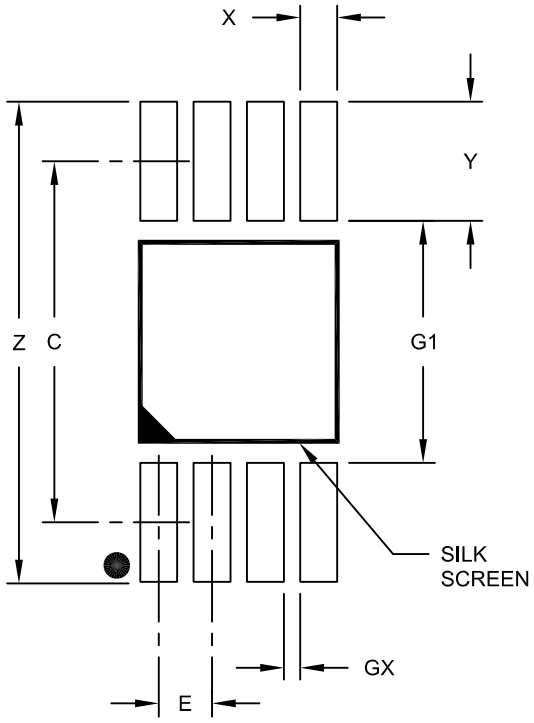
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (UA) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

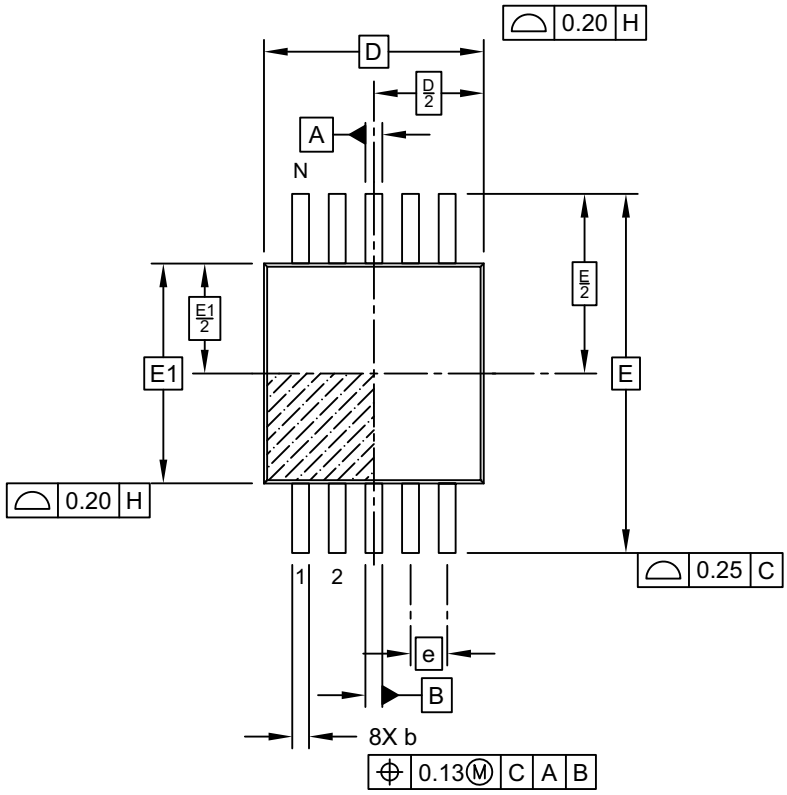
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

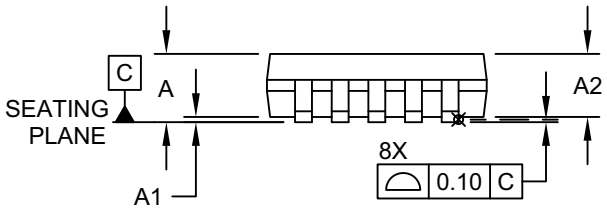
Microchip Technology Drawing No. C04-2111A

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

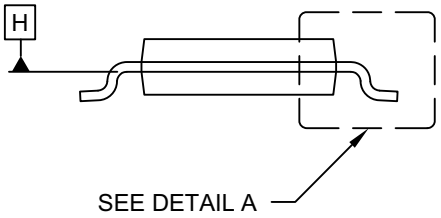
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

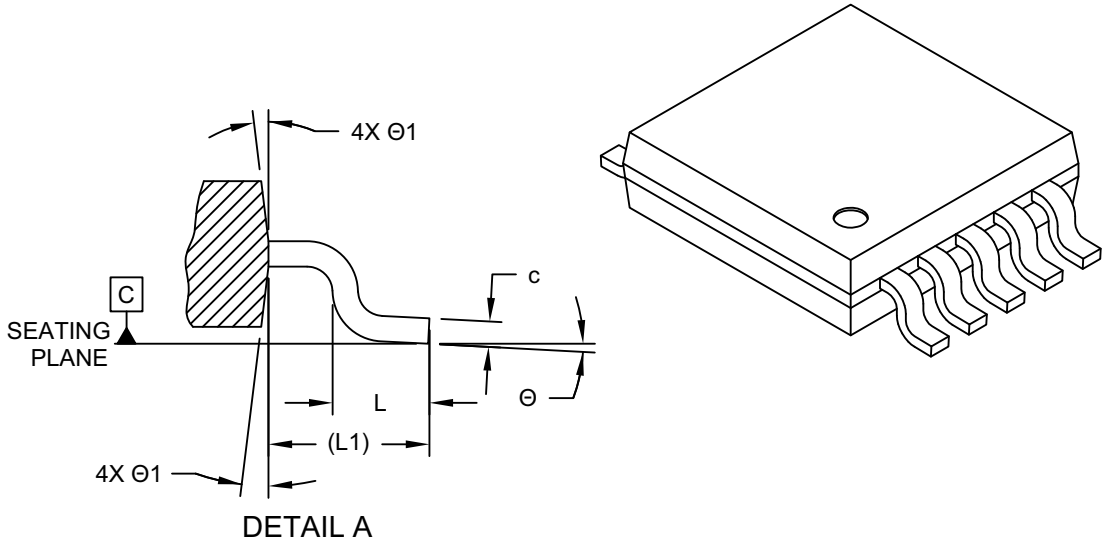


END VIEW

Microchip Technology Drawing C04-021D Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Mold Draft Angle	Θ	0°	-	8°
Foot Angle	Θ1	5°	-	15°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

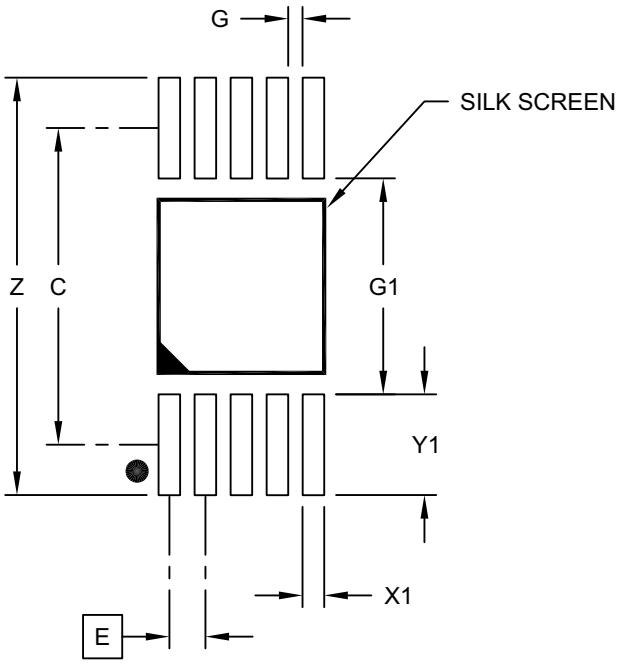
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021D Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

Notes:

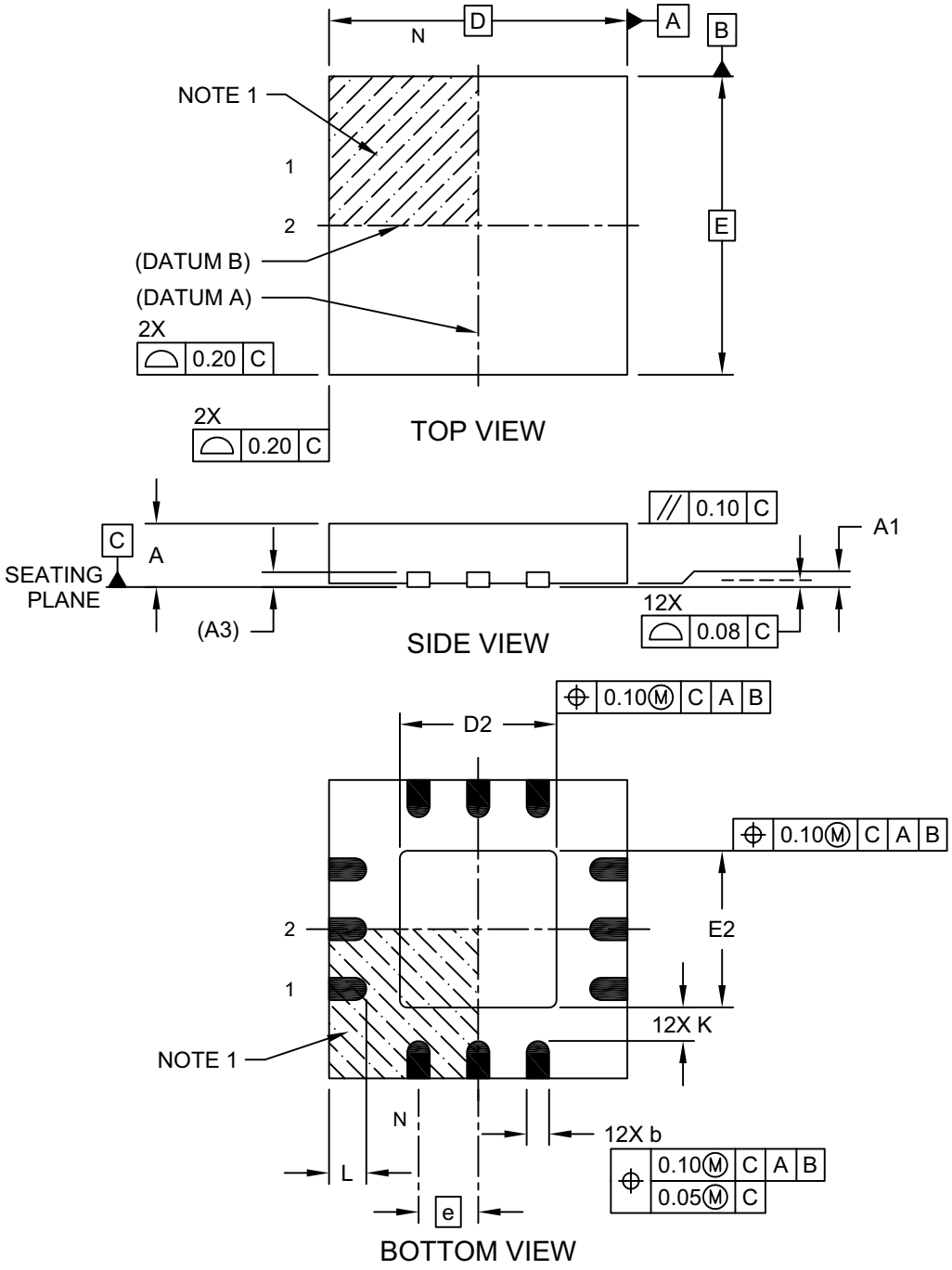
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021B

12-Lead Very Thin Plastic Quad Flat, No Lead Package (UL) - 4x4 mm Body [VQFN] SMSC Legacy KP [SQFN]

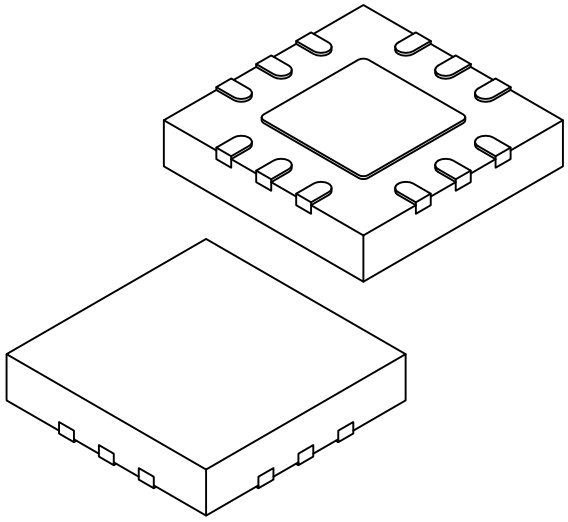
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-308A Sheet 1 of 2

12-Lead Very Thin Plastic Quad Flat, No Lead Package (UL) - 4x4 mm Body [VQFN] SMSC Legacy KP [SQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		12	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.00	2.10	2.20
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.00	2.10	2.20
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.40	0.50	0.60
Terminal-to-Exposed-Pad	K	0.35	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

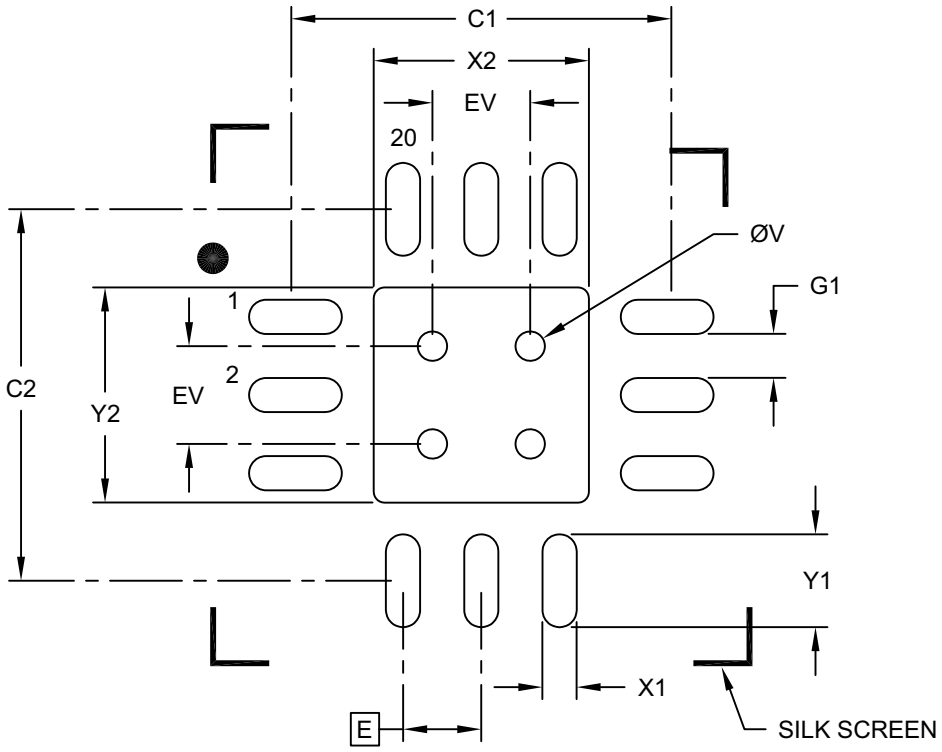
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-308A Sheet 2 of 2

12-Lead Very Thin Plastic Quad Flat, No Lead Package (UL) - 4x4 mm Body [VQFN] SMSC Legacy KP [SQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Optional Center Pad Width	X2			2.20
Optional Center Pad Length	Y2			2.20
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X12)	X1			0.37
Contact Pad Length (X12)	Y1			0.95
Contact Pad to Center Pad (X12)	G1	0.45		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

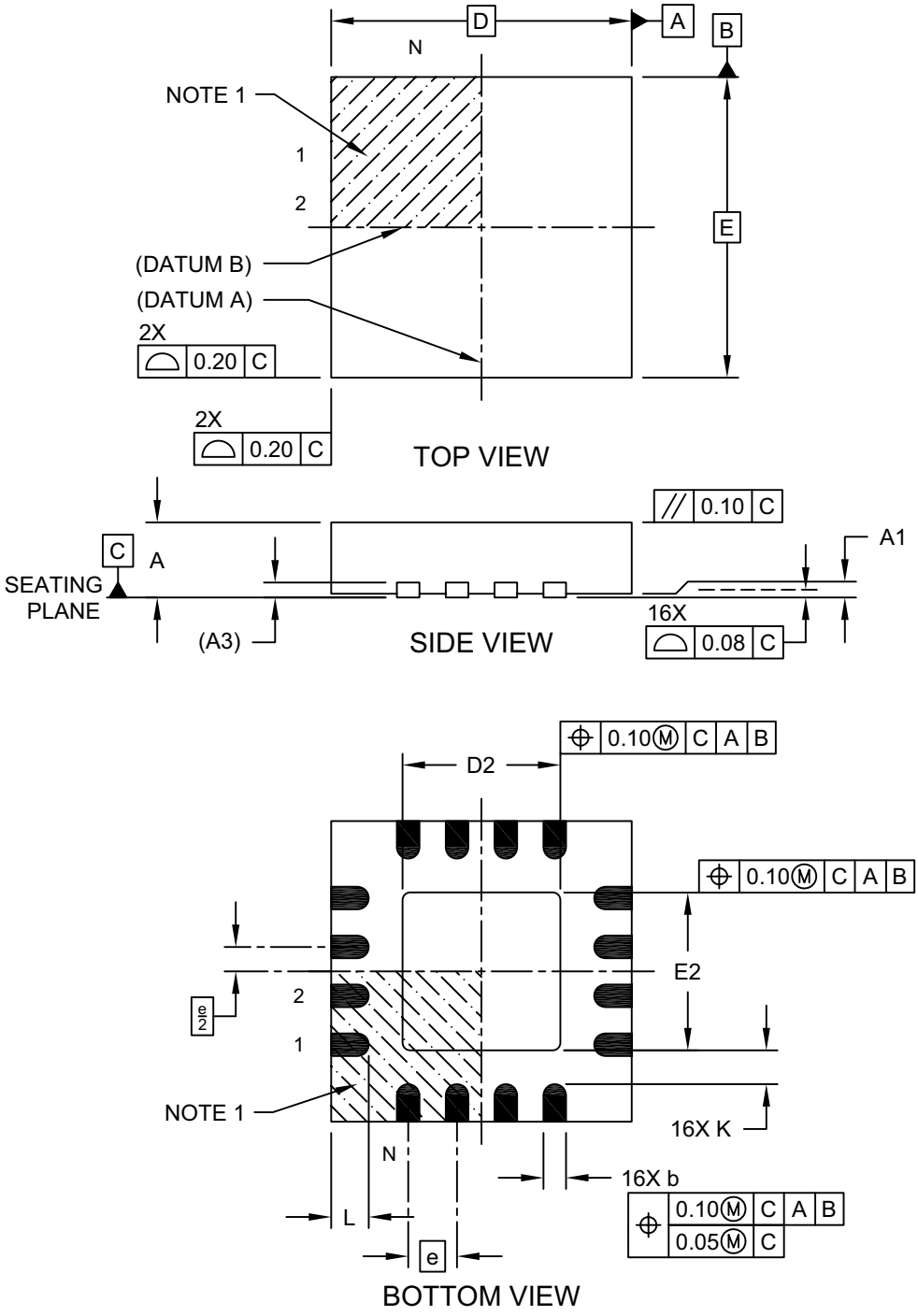
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2308A

16-Lead Very Thin Plastic Quad Flat, No Lead Package (AP) - 4x4 mm Body [VQFN] SMSC Legacy AP [SQFN]

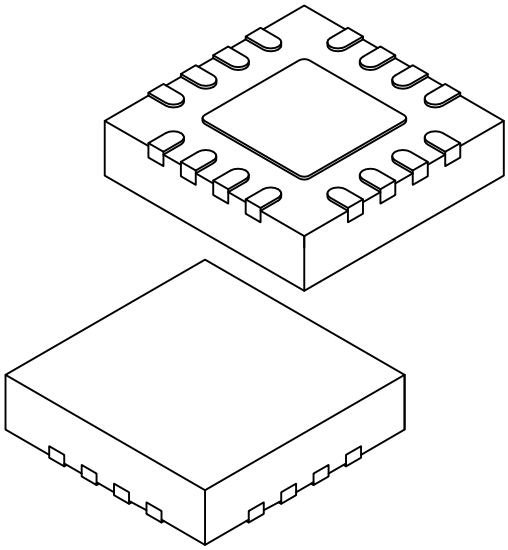
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-381A Sheet 1 of 2

16-Lead Very Thin Plastic Quad Flat, No Lead Package (AP) - 4x4 mm Body [VQFN] SMSC Legacy AP [SQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.00	2.10	2.20
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.00	2.10	2.20
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.40	0.50	0.60
Terminal-to-Exposed-Pad	K	0.35	-	-

Notes:

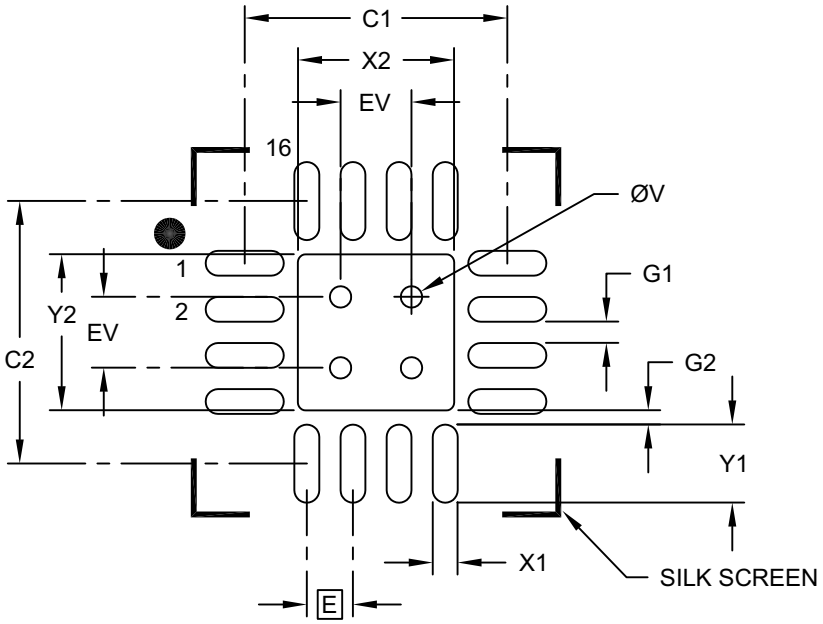
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-381A Sheet 2 of 2

16-Lead Very Thin Plastic Quad Flat, No Lead Package (AP) - 4x4 mm Body [VQFN] SMSC Legacy AP [SQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			2.20
Optional Center Pad Length	Y2			2.20
Contact Pad Spacing	C1		3.70	
Contact Pad Spacing	C2		3.70	
Contact Pad Width (X16)	X1			0.37
Contact Pad Length (X16)	Y1		0.79	1.10
Space Between Pads	G1	0.30		
Contact Pad to Center Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2381A

APPENDIX A: REVISION HISTORY

Revision A (April 2021)

- Original release of this document.
- This document replaces the following Data Sheets:
  - EMC2301 Data Sheet - *"RPM-Based PWM Fan Controller"* (SMSC EMC2301 Revision 1.3 (05-18-11)).
  - EMC2302 Data Sheet - *"Dual RPM-Based PWM Fan Controller"* (SMSC EMC2302 Revision 1.3 (05-18-11))
  - EMC2303 Data Sheet - *"Multiple RPM-Based PWM Fan Controller for Three Fans"* (SMSC EMC2303 Revision 1.3 (05-18-11))
  - EMC2305 Data Sheet - *"Multiple RPM-Based PWM Fan Controller for Five Fans"* (SMSC EMC2305 Revision 1.3 (05-18-11))
- The SMBus standard uses the terminology "slave". The equivalent Microchip terminology used in this document is "client".

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	-XX(/XXXX)	-XX
Device	SMBus Address	Package Type	Tape and Reel

Device:	EMC2301/2/3/5 - Single/Multiple RPM-Based PWM Fan Controller
SMBus Address	1 - SMBus address is set at 0101_111r/w (EMC2301 only). SMbus Address is set at 0101_110r/w (EMC2302 only). SMBus Address is selectable (EMC2303 and EMC2305 only). 2 - SMBus address is set at 0101_111r/w (EMC2302 only).
Package Type	ACZL = Plastic Micro Small Outline Package (8-Lead MSOP) AIZL = Plastic Micro Small Outline Package (10-Lead MSOP) KP = Very Thin Plastic Quad Flat, No Lead Package (12-Lead QFN) AP = Very Thin Plastic Quad Flat, No Lead Package (16-Lead QFN)
Tape and Reel	TR = Tape and Reel (**Note 1**)

Examples:

a) EMC2301-1-ACZL-TR = Single RPM-Based PWM Fan Controller, MSOP-8 Package

b) EMC2302-2-AIZL-TR = Dual RPM-Based PWM Fan Controller, MSOP-10 Package

c) EMC2303-1-KP-TR = Multiple RPM-Based PWM Fan Controller for Three Fans, QFN-12 Package

d) EMC2305-1-AP-TR = Multiple RPM-Based PWM Fan Controller for Five Fans, QFN-16 Package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is nto printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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