KSZ8041NL/RNL

10BASE-T/100BASE-TX Physical Layer Transceiver

Highlights

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- HP Auto-MDIX Support

Target Applications

- Printer
- LOM
- Game Console
- IPTV
- IP Phone
- IP Set-Top Box

Key Benefits

- Single-Chip 10BASE-T/100BASE-TX Physical Layer Solution
- Fully Compliant To IEEE 802.3u Standard
- Low Power CMOS Design, Power Consumption of <180 mW
- HP Auto MDI/MDI-X For Reliable Detection and Correction for Straight-Through and Crossover Cables with Disable and Enable Option
- Robust Operation Over Standard Cables
- Power Down and Power Saving Modes
- MII Interface Support (KSZ8041NL Only)
- RMII Interface Support with External 50-MHz System Clock (KSZ8041NL Only)
- RMII Interface Support with 25-MHz Crystal/Clock Input and 50-MHz Reference Clock Output to MAC (KSZ8041RNL Only)
- MIIM (MDC/MDIO) Management Bus to 6.25 MHz for Rapid PHY Register Configuration
- Interrupt Pin Option
- Programmable LED Outputs for Link, Activity and Speed
- ESD Rating (6 kV)
- Single Power Supply (3.3V)
- Built-in 1.8V Regulator for Core
- Available In 32-pin 5 mm × 5 mm QFN Package

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1.0 GENERAL DESCRIPTION

The KSZ8041NL is a single supply 10BASE-T/100BASE-TX physical layer transceiver, which provides MII/RMII interfaces to transmit and receive data. A unique mixed-signal design extends signaling distance while reducing power consumption.

HP Auto MDI/MDI-X provides the most robust solution for eliminating the need to differentiate between crossover and straight-through cables.

The KSZ8041NL represents a new level of features and performance and is an ideal choice of physical layer transceiver for 10BASE-T/100BASE-TX applications.

The KSZ8041RNL is an enhanced Reduced Media Independent Interface (RMII) version of the KSZ8041NL that does not require a 50-MHz system clock. It uses a 25-MHz crystal for its input reference clock and outputs a 50-MHz RMII reference clock to the media access control (MAC).

The KSZ8041NL and KSZ8041RNL are available in 32-pin, lead-free QFN packages (see Product Identification System).

FIGURE 1-1: KSZ8041NL FUNCTIONAL DIAGRAM

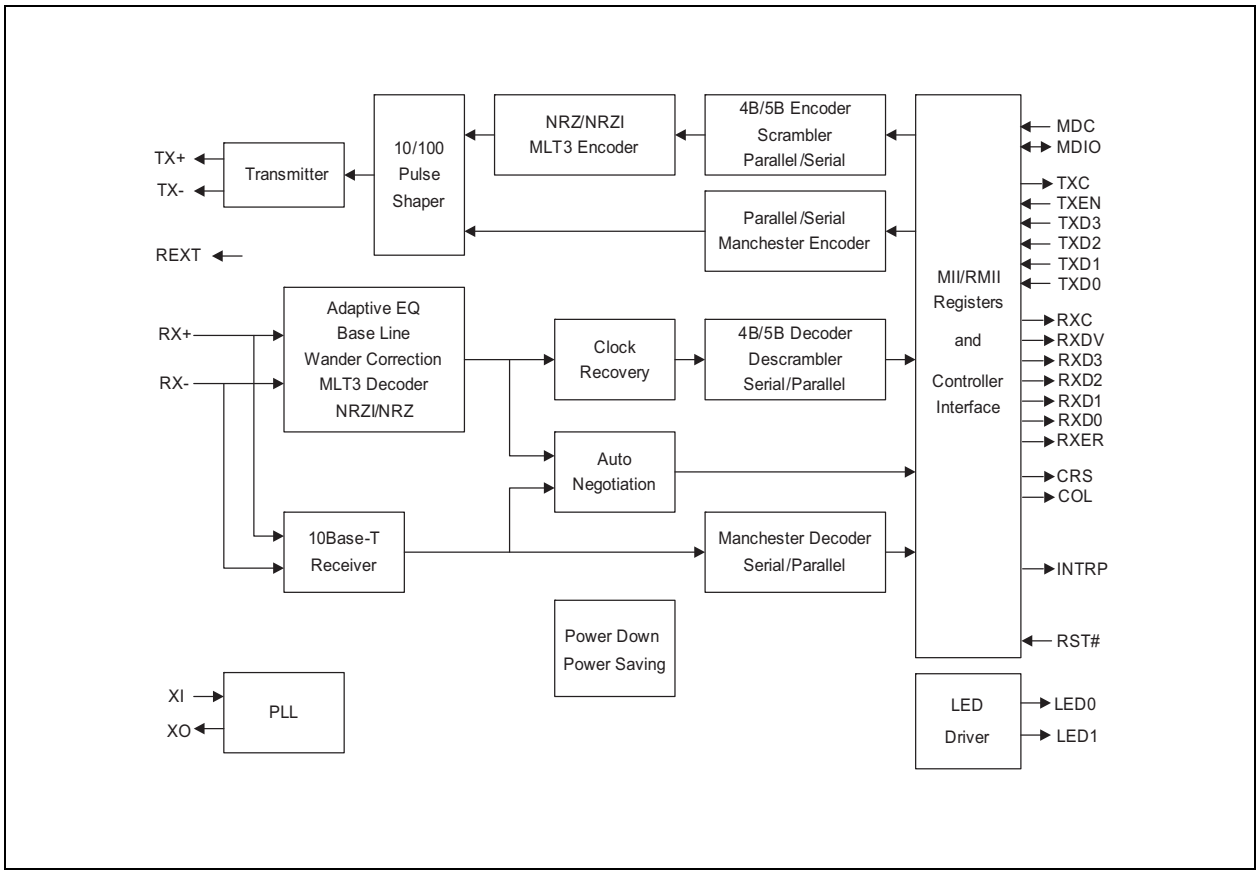
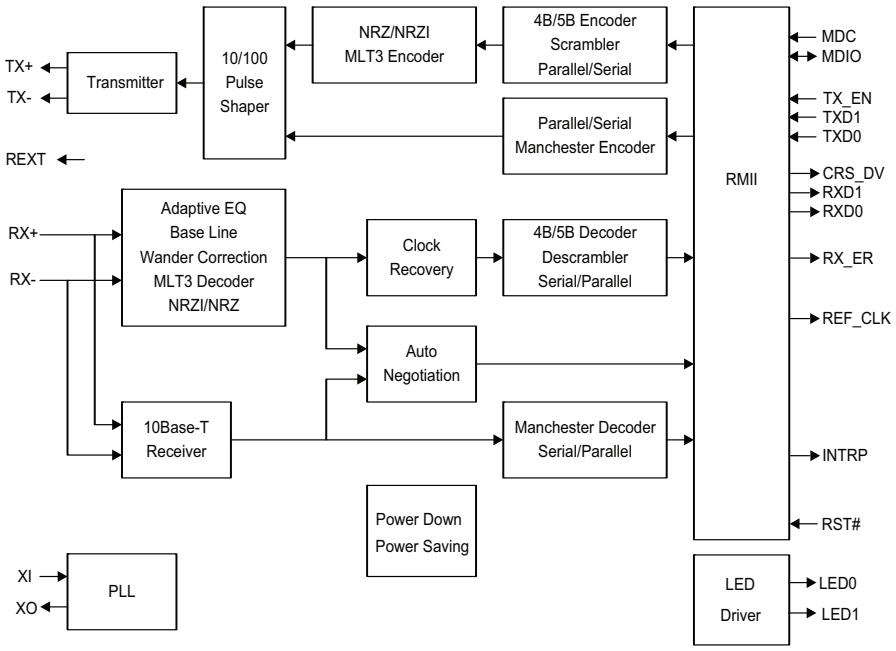


FIGURE 1-2: KSZ8041RNL FUNCTIONAL DIAGRAM



2.0 PIN DESCRIPTION AND CONFIGURATION

2.1 KSZ8041NL Pin Description and Configuration

FIGURE 2-1: KSZ8041NL 32-QFN PIN ASSIGNMENT (TOP VIEW)

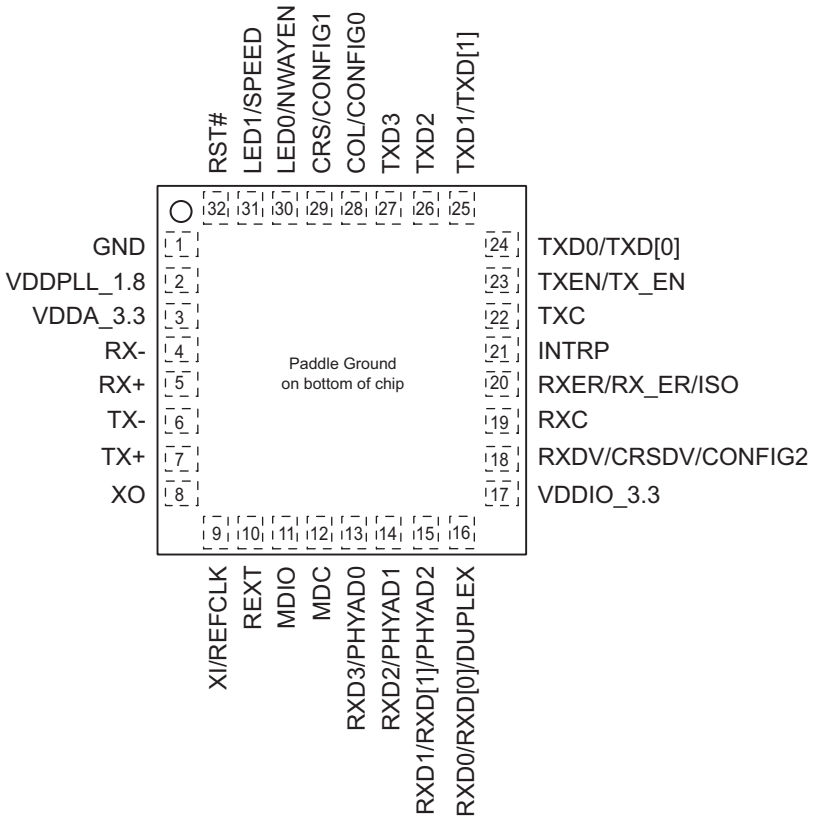


TABLE 2-1: KSZ8041NL PIN DESCRIPTION

Pin Number	Symbol	Buffer Type (Note 2-1)	Description
1	GND	Gnd	Ground
2	VDDPLL_1.8	P	1.8V Analog V_{DD} Decouple with 1.0-µF and 0.1-µF capacitors to ground.
3	VDDA_3.3	P	3.3V Analog V_{DD}
4	RX-	I/O	Physical receive or transmit signal (- differential)
5	RX+	I/O	Physical receive or transmit signal (+ differential)
6	TX-	I/O	Physical transmit or receive signal (- differential)

TABLE 2-1: KSZ8041NL PIN DESCRIPTION (CONTINUED)

Pin Number	Symbol	Buffer Type (Note 2-1)	Description
7	TX+	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal Feedback. This pin is used only in MII mode when a 25-MHz crystal is used. This pin is a no connect if an oscillator or an external clock source is used, or if RMII mode is selected.
9	XI / REFCLK	I	Crystal/Oscillator/External Clock Input: MII mode: 25 MHz ±50 ppm (crystal, oscillator, or external clock) RMII mode: 50 MHz ±50 ppm (oscillator or external clock only)
10	REXT	I/O	Set physical transmit output current. Connect a 6.49-KΩ resistor in parallel with a 100-pF capacitor to ground on this pin.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7-KΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	RXD3 / PHYAD0	Ipu/O	MII mode: Receive Data Output[3] (Note 2-2) Config mode: The pull-up/pull-down value is latched as PHY-ADDR[0] during power-up or reset. See "Strap-In option – KSZ8041NL" for details.
14	RXD2 / PHYAD1	Ipd/O	MII mode: Receive Data Output[2] (Note 2-2) Config mode: The pull-up/pull-down value is latched as PHY-ADDR[1] during power-up or reset. See "Strap-In option – KSZ8041NL" for details.
15	RXD1 / RXD[1] / PHYAD2	Ipd/O	MII mode: Receive Data Output[1] (Note 2-2) RMII mode: Receive Data Output[1] (Note 2-3) Config mode: The pull-up/pull-down value is latched as PHY-ADDR[2] during power-up or reset. See "Strap-In option – KSZ8041NL" for details.
16	RXD0 / RXD[0] / DUPLEX	Ipu/O	MII mode: Receive Data Output[0] (Note 2-2). RMII mode: Receive Data Output[0] (Note 2-3). Config mode: Latched as DUPLEX (register 0h, bit 8) during power-up or reset. See "Strap-In option – KSZ8041NL" for details.
17	VDDIO_3.3	P	3.3V Digital V_{DD}
18	RXDV / CRSDV / CONFIG2	Ipd/O	MII mode: Receive Data Valid Output RMII mode: Carrier Sense/Receive Data Valid Output Config mode: The pull-up/pull-down value is latched as CONFIG2 during power-up or reset. See "Strap-In option – KSZ8041NL" for details.
19	RXC	O	MII mode: Receive Clock Output
20	RXER / RX_ER / ISO	Ipd/O	MII mode: Receive Error Output RMII mode: Receive Error Output Config mode: The pull-up/pull-down value is latched as ISOLATE during power-up or reset. See "Strap-In option – KSZ8041NL" for details.

TABLE 2-1: KSZ8041NL PIN DESCRIPTION (CONTINUED)

Pin Number	Symbol	Buffer Type (Note 2-1)	Description
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	TXC	O	MII mode: Transmit Clock Output
23	TXEN / TX_EN	I	MII mode: Transmit Enable Input RMII mode: Transmit Enable Input
24	TXD0 / TXD[0]	I	MII mode: Transmit Data Input[0] (Note 2-4) RMII mode: Transmit Data Input[0] (Note 2-5)
25	TXD1 / TXD[1]	I	MII mode: Transmit Data Input[1] (Note 2-4) RMII mode: Transmit Data Input[1] (Note 2-5)
26	TXD2	I	MII mode: Transmit Data Input[2] (Note 2-4)
27	TXD3	I	MII mode: Transmit Data Input[3] (Note 2-4)
28	COL/CONFIG0	Ipd/O	MII mode: Collision Detect Output Config mode: The pull-up/pull-down value is latched as CONFIG0 during power-up or reset. See “Strap-In option – KSZ8041NL” for details.
29	CRS/CONFIG1	Ipd/O	MII mode: Collision Sense Output Config mode: The pull-up/pull-down value is latched as CONFIG1 during power-up or reset. See “Strap-In option – KSZ8041NL” for details.

TABLE 2-1: KSZ8041NL PIN DESCRIPTION (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Buffer Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>30</td><td>LED0 / NWAYEN</td><td>Ipu/O</td><td>
LED Output: Programmable LED0 Output
Config ode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up or reset. See Strap-In option – KSZ8041NL for details.
The LED0 pin is programmable via register 1Eh bits [15:14] and is defined as follows:

LED Mode = [00]
<table>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
<tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr>
</table>
LED Mode = [01]
<table>
<tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No Link</td><td>H</td><td>OFF</td></tr>
<tr><td>Link</td><td>L</td><td>ON</td></tr>
</table>
<u>LED Mode = [10]</u>
Reserved

<u>LED Mode = [11]</u>
Reserved
</td></tr>
</table>

TABLE 2-1: KSZ8041NL PIN DESCRIPTION (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Buffer Type (Note 2-1)</th><th>Description</th></tr>
<tr><td>31</td><td>LED1 / SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output
Config mode: Latched as SPEED (register 0h, bit 13) during power-up or reset. See Strap-In option – KSZ8041NL for details.
The LED1 pin is programmable via register 1Eh bits [15:14] and is defined as follows:

LED Mode = [00]
<table><tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>10BT</td><td>H</td><td>OFF</td></tr><tr><td>100BT</td><td>L</td><td>ON</td></tr></table>
LED Mode = [01]
<table><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Activity</td><td>H</td><td>OFF</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
<u>LED Mode = [10]</u>
Reserved

<u>LED Mode = [11]</u>
Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low)</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground</td></tr>
</table>

Note 2-1 P = Power supply
Gnd = Ground
I = Input
O = Output
I/O = Bi-directional
Ipd = Input with internal pull-down (40K ±30%)
Ipu = Input with internal pull-up (40K ±30%)
Opu = Output with internal pull-up (40K ±30%)
Ipu/O = Input with internal pull-up (40K ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40K ±30%) during power-up/reset; output pin otherwise.

Note 2-2 MII Rx mode: The RXD[3:0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3:0] presents a valid data to the MAC through the MII. RXD[3:0] is invalid when RXDV is deasserted.

Note 2-3 RMII Rx mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.

Note 2-4 MII Tx mode: The TXD[3:0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3:0] presents a valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is deasserted.

Note 2-5 RMII Tx mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

2.2 STRAP-IN OPTION – KSZ8041NL

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap in to ISOLATE mode, or is not configured with an incorrect PHY Address.

TABLE 2-2: STRAP-IN OPTION – KSZ8041NL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Pin Function</th></tr>
<tr><td>15</td><td>PHYAD2</td><td>Ipd/O</td><td rowspan="3">The PHY Address is latched at power-up or reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>14</td><td>PHYAD1</td><td>Ipd/O</td></tr>
<tr><td>13</td><td>PHYAD0</td><td>Ipu/O</td></tr>
<tr><td>18</td><td>CONFIG2</td><td>Ipd/O</td><td rowspan="3">The CONFIG[2:0] strap-in pins are latched at power-up or reset and are defined as follows:

<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>Reserved - not used</td></tr><tr><td>011</td><td>Reserved - not used</td></tr><tr><td>100</td><td>MII 100 Mbps Preamble Restore</td></tr><tr><td>101</td><td>Reserved - not used</td></tr><tr><td>110</td><td>Reserved - not used</td></tr><tr><td>111</td><td>Reserved - not used</td></tr></table></td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>ISOLATE mode:
Pull-up = Enable
Pull-down (default) = Disable
During power-up or reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>SPEED mode:
Pull-up (default) = 100 Mbps
Pull-down = 10 Mbps
During power-up or reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>DUPLEX mode:
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up or reset, this pin value is latched into register 0h bit 8 as the Duplex mode.</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway Auto-Negotiation Enable:
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
During power-up or reset, this pin value is latched into register 0h bit 12.</td></tr>
</table>

Note 2-1 Ipu/O = Input with internal pull-up (40K ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40K ±30%) during power-up/reset; output pin otherwise.

2.3 KSZ8041RNL Pin Description and Configuration

FIGURE 2-2: KSZ8041RNL 32-QFN PIN ASSIGNMENT (TOP VIEW)

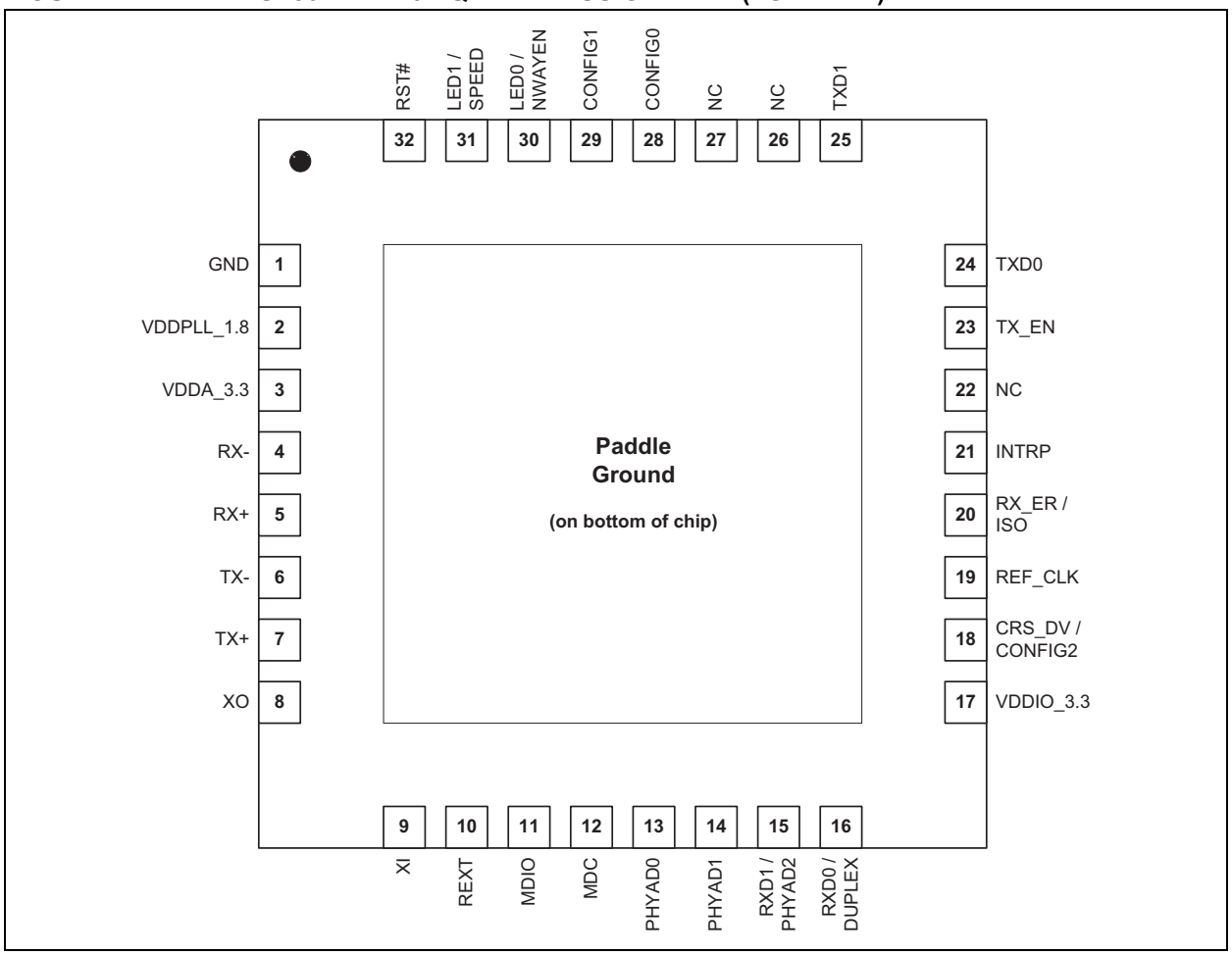


TABLE 2-3: KSZ8041RNL PIN DESCRIPTION

Pin Number	Pin Name	Type (Note 2-1)	Pin Function
1	GND	Gnd	Ground
2	VDDPLL_1.8	P	1.8V Analog V_{DD} Decouple with 1.0-µF and 0.1-µF capacitors to ground.
3	VDDA_3.3	P	3.3V Analog V_{DD}
4	RX-	I/O	Physical receive or transmit signal (- differential)
5	RX+	I/O	Physical receive or transmit signal (+ differential)
6	TX-	I/O	Physical transmit or receive signal (- differential)
7	TX+	I/O	Physical transmit or receive signal (+ differential)
8	XO	O	Crystal Feedback for 25-MHz Crystal This pin is a no connect if an oscillator or an external clock source is used.
9	XI	I	Crystal/Oscillator/External Clock Input 25 MHz ±50 ppm
10	REXT	I/O	Set physical transmit output current. Connect a 6.49-kΩ resistor in parallel with a 100-pF capacitor to ground on this pin. See KSZ8041RNL reference schematics.

TABLE 2-3: KSZ8041RNL PIN DESCRIPTION (CONTINUED)

Pin Number	Pin Name	Type (Note 2-1)	Pin Function
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7-kΩ pull-up resistor.
12	MDC	I	Management Interface (MII) Clock Input This pin is synchronous to the MDIO data interface.
13	PHYAD0	Ipu/O	The pull-up/pull-down value is latched as PHYADDR[0] during power-up or reset. See Strap-In option – KSZ8041RNL for details.
14	PHYAD1	Ipd/O	The pull-up/pull-down value is latched as PHYADDR[1] during power-up or reset. See Strap-In option – KSZ8041RNL for details.
15	RXD1 / PHYAD2	Ipd/O	RMII mode: RMII Receive Data Output[1] (Note 2-2) Config mode: The pull-up/pull-down value is latched as PHYADDR[2] during power-up or reset. See Strap-In option – KSZ8041RNL for details.
16	RXD0 / DUPLEX	Ipu/O	RMII mode: RMII Receive Data Output[0]] (Note 2-2) Config mode: Latched as DUPLEX (register 0h, bit 8) during power-up or reset. See Strap-In option – KSZ8041RNL for details.
17	VDDIO_3.3	P	3.3V Digital V_{DD}
18	CRSDV / CONFIG2	Ipd/O	RMII mode: Carrier Sense/Receive Data Valid Output Config mode: The pull-up/pull-down value is latched as CONFIG2 during power-up or reset. See Strap-In option – KSZ8041RNL for details.
19	REF_CLK	O	50 MHz Clock Output This pin provides the 50-MHz RMII reference clock output to the MAC.
20	RXER / RX_ER / ISO	Ipd/O	RMII mode: Receive Error Output. Config mode: The pull-up/pull-down value is latched as ISOLATE during power-up or reset. See Strap-In option – KSZ8041RNL for details.
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.
22	NC	O	No Connect
23	TX_EN	I	RMII Transmit Enable Input
24	TXD0	I	RMII Transmit Data Input[0] (Note 2-3)
25	TXD1	I	RMII Transmit Data Input[1] (Note 2-3)
26	NC	I	No Connect
27	NC	I	No Connect
28	CONFIG0	Ipd/O	The pull-up/pull-down value is latched as CONFIG0 during power-up or reset. See Strap-In option – KSZ8041RNL for details.
29	CONFIG1	Ipd/O	The pull-up/pull-down value is latched as CONFIG1 during power-up or reset. See Strap-In option – KSZ8041RNL for details.

TABLE 2-3: KSZ8041RNL PIN DESCRIPTION (CONTINUED)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Pin Function</th></tr>
<tr><td>30</td><td>LED0 /
NWAYEN</td><td>Ipu/O</td><td>LED Output: Programmable LED0 Output
Config mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up or reset. See Strap-In option – KSZ8041RNL for details.
The LED0 pin is programmable via register 1Eh bits [15:14] and is defined as follows:

LED Mode = [00]

<table><tr><th>Link/Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Link</td><td>H</td><td>OFF</td></tr><tr><td>Link</td><td>L</td><td>ON</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
LED Mode = [01]

<table><tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Link</td><td>H</td><td>OFF</td></tr><tr><td>Link</td><td>L</td><td>ON</td></tr></table>
<u>LED Mode = [10], [11]</u>
Reserved</td></tr>
<tr><td>31</td><td>LED1 /
SPEED</td><td>Ipu/O</td><td>LED Output: Programmable LED1 Output
Config mode: Latched as SPEED (register 0h, bit 13) during power-up or reset. See Strap-In option – KSZ8041RNL for details.
The LED1 pin is programmable via register 1Eh bits [15:14] and is defined as follows:

LED Mode = [00]

<table><tr><th>Speed</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>10BT</td><td>H</td><td>OFF</td></tr><tr><td>100BT</td><td>L</td><td>ON</td></tr></table>
LED Mode = [01]

<table><tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr><tr><td>No Activity</td><td>H</td><td>OFF</td></tr><tr><td>Activity</td><td>Toggle</td><td>Blinking</td></tr></table>
<u>LED Mode = [10], [11]</u>
Reserved</td></tr>
<tr><td>32</td><td>RST#</td><td>I</td><td>Chip Reset (active low)</td></tr>
<tr><td>PADDLE</td><td>GND</td><td>Gnd</td><td>Ground</td></tr>
</table>

Note 2-1 P = Power supply
Gnd = Ground
I = Input
O = Output
I/O = Bi-directional
Opu = Output with internal pull-up (40K ±30%)
Ipu/O = Input with internal pull-up (40K ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40K ±30%) during power-up/reset; output pin otherwise.

Note 2-2 RMII Rx mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.

Note 2-3 RMII Tx mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

2.4 STRAP-IN OPTION – KSZ8041RNL

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the RMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap in to ISOLATE mode, or is not configured with an incorrect PHY Address.

TABLE 2-4: STRAP-IN OPTION – KSZ8041RNL

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type (Note 2-1)</th><th>Pin Function</th></tr>
<tr><td>15</td><td>PHYAD2</td><td>Ipd/O</td><td rowspan="3">The PHY Address is latched at power-up or reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>14</td><td>PHYAD1</td><td>Ipd/O</td></tr>
<tr><td>13</td><td>PHYAD0</td><td>Ipu/O</td></tr>
<tr><td>18</td><td>CONFIG2</td><td>Ipd/O</td><td rowspan="3">The CONFIG[2:0] strap-in pins are latched at power-up or reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>Reserved - not used</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>Reserved - not used</td></tr><tr><td>011</td><td>Reserved - not used</td></tr><tr><td>100</td><td>Reserved - not used</td></tr><tr><td>101</td><td>Reserved - not used</td></tr><tr><td>110</td><td>Reserved - not used</td></tr><tr><td>111</td><td>Reserved - not used</td></tr></table></td></tr>
<tr><td>29</td><td>CONFIG1</td><td>Ipd/O</td></tr>
<tr><td>28</td><td>CONFIG0</td><td>Ipd/O</td></tr>
<tr><td>20</td><td>ISO</td><td>Ipd/O</td><td>ISOLATE mode:
Pull-up = Enable
Pull-down (default) = Disable
During power-up or reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>31</td><td>SPEED</td><td>Ipu/O</td><td>SPEED mode:
Pull-up (default) = 100 Mbps
Pull-down = 10 Mbps
During power-up or reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>16</td><td>DUPLEX</td><td>Ipu/O</td><td>DUPLEX mode:
Pull-up (default) = Half Duplex
Pull-down = Full Duplex
During power-up or reset, this pin value is latched into register 0h bit 8 as the Duplex mode.</td></tr>
<tr><td>30</td><td>NWAYEN</td><td>Ipu/O</td><td>Nway Auto-Negotiation Enable:
Pull-up (default) = Enable Auto-Negotiation
Pull-down = Disable Auto-Negotiation
During power-up or reset, this pin value is latched into register 0h bit 12.</td></tr>
</table>

Note 2-1 Ipu/O = Input with internal pull-up (40K ±30%) during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down (40K ±30%) during power-up/reset; output pin otherwise.

3.0 FUNCTIONAL DESCRIPTION

The KSZ8041NL is a single 3.3V supply Fast Ethernet transceiver. It is fully compliant with the IEEE 802.3u specification.

On the media side, the KSZ8041NL supports 10BASE-T and 100BASE-TX with HP auto MDI/MDI-X for reliable detection of and correction for straight-through and crossover cables.

The KSZ8041NL offers a choice of MII or RMII data interface connection with the MAC processor. The MII management bus option gives the MAC processor complete access to the KSZ8041NL control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll for PHY status change.

Physical signal transmission and reception are enhanced through the use of patented analog circuitries that make the design more efficient and allow for lower power consumption and smaller chip die size.

The KSZ8041RNL is an enhanced RMII version of the KSZ8041NL that does not require a 50-MHz system clock. It uses a 25-MHz crystal for its input reference clock and outputs a 50-MHz RMII reference clock to the MAC.

3.1 100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125-MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output.

The output current is set by an external 6.49-kΩ 1% resistor for the 1:1 transformer ratio. It has typical rise or fall times of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output drivers are also incorporated into the 100BASE-TX drivers.

3.2 100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, descrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are functions of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, and then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and to improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125-MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the descrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

3.3 PLL Clock Synthesizer

The KSZ8041NL/RNL generates 125-MHz, 25-MHz, and 20-MHz clocks for system timing. Internal clocks are generated from an external 25-MHz crystal or oscillator. For the KSZ8041NL in RMII mode, these internal clocks are generated from an external 50-MHz oscillator or system clock.

3.4 Scrambler/Descrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce EMI and baseline wander.

3.5 10BASE-T Transmit

The 10BASE-T drivers are incorporated with the 100BASE-TX drivers to allow for transmission using the same magnetic. The drivers also perform internal wave-shaping and pre-emphasize, and output 10BASE-T signals with a typical amplitude of 2.5V peak. The 10BASE-T signals have harmonic contents that are at least 27 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

3.6 10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL performs the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400 mV or with short pulse widths to prevent noise at the RX+ and RX- inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8041NL/RNL decodes a data frame. The receive clock is kept active during idle periods in between data reception.

3.7 SQE and Jabber Function (10BASE-T only)

In 10BASE-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10BASE-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10BASE-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10BASE-T transmitter is re-enabled and COL is deasserted (returns to low).

3.8 Auto-Negotiation

The KSZ8041NL/RNL conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Auto-negotiation is enabled by either hardware pin strapping (pin 30) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation.

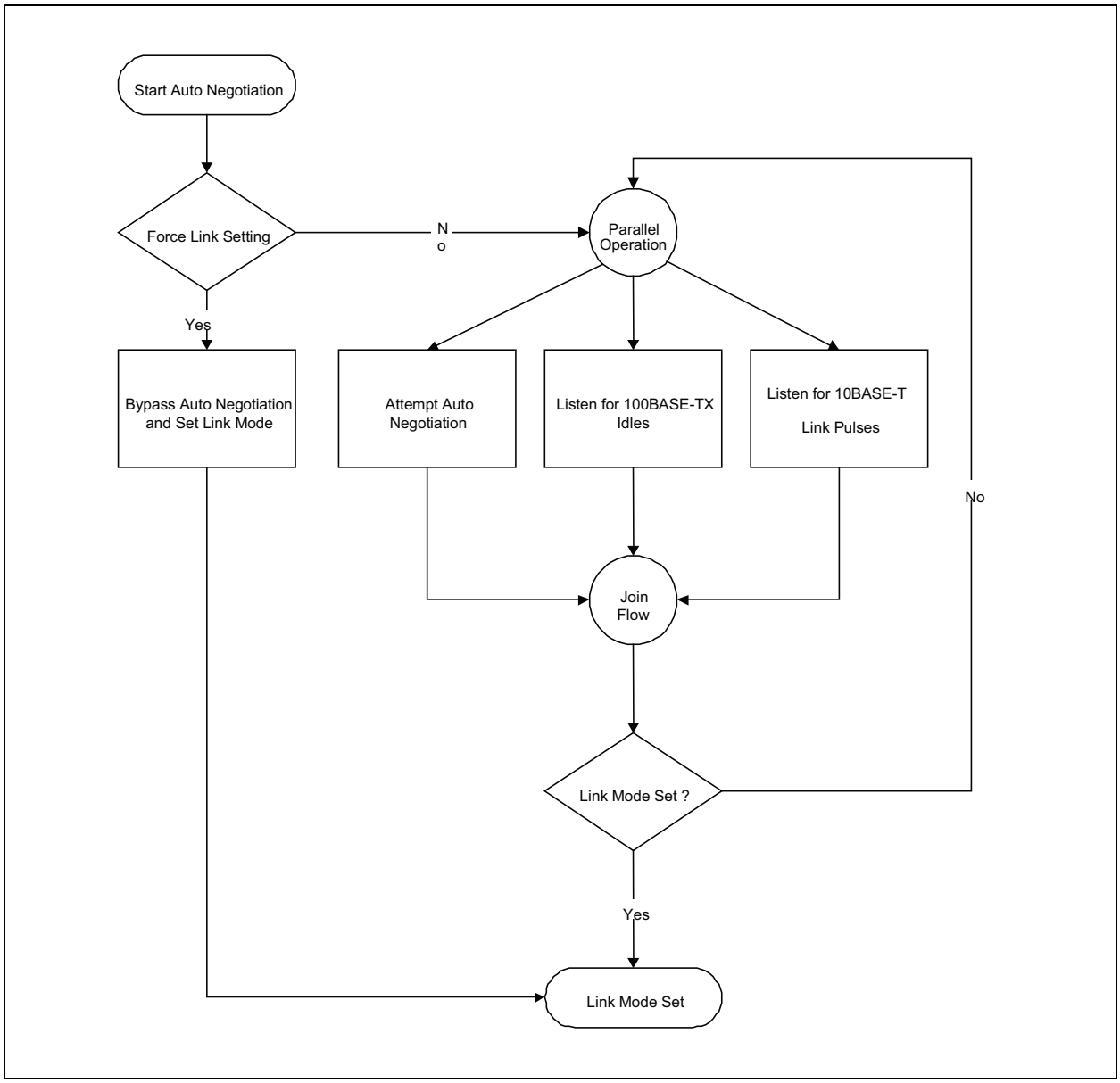
The following list shows the speed and duplex operation mode from highest to lowest:

- Priority 1: 100BASE-TX, full-duplex
- Priority 2: 100BASE-TX, half-duplex
- Priority 3: 10BASE-T, full-duplex
- Priority 4: 10BASE-T, half-duplex

If auto-negotiation is not supported or the KSZ8041NL/RNL link partner is forced to bypass auto-negotiation, the KSZ8041NL/RNL sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and this allows the KSZ8041NL/RNL to establish a link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in the flow chart illustrated as Figure 3-1.

FIGURE 3-1: AUTO-NEGOTIATION FLOW CHART



3.9 MII Management (MIIM) Interface

The KSZ8041NL/RNL supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input or Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the KSZ8041NL/RNL. An external device with MIIM capability is used to read the PHY status or to configure the PHY settings or both. Further details on the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with one or more PHY devices. Each KSZ8041NL/RNL device is assigned a unique PHY address between 1 and 7 by its PHYAD[2:0] strapping pins. Additionally, every KSZ8041NL/RNL device supports the broadcast PHY address 0, as defined per the IEEE 802.3 specification, which can be used to read or write to a single KSZ8041NL/RNL device, or write to multiple KSZ8041NL/RNL devices simultaneously.
- A set of 16-bit MDIO registers. Registers [0:6] are required, and their functions are defined per the IEEE 802.3 specification. The additional registers are provided for expanded functionality.

Table 3-1 shows the MII Management frame format for the KSZ8041NL/RNL.

TABLE 3-1: MII MANAGEMENT FRAME FORMAT

	Preamble	Start of Frame	Read/ Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

3.10 Interrupt (INTRP)

INTRP (pin 21) is an optional interrupt signal that is used to inform the external controller that there has been a status update to the KSZ8041NL/RNL PHY register. Bits[15:8] of register 1Bh are the interrupt control bits and are used to enable and disable the conditions for asserting the INTRP signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh.

Bit 9 of register 1Fh sets the interrupt level to active high or active low.

3.11 MII Data Interface (KSZ8041NL only)

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3 specification. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10 Mbps and 100 Mbps data rates
- Uses a 25-MHz reference clock, sourced by the PHY
- Provides independent 4-bit wide (nibble) transmit and receive data paths
- Contains two distinct groups of signals: one for transmission and the other for reception

By default, the KSZ8041NL is configured to MII mode after it is powered up or reset with the following:

- A 25-MHz crystal connected to XI, XO (pins 9, 8), or an external 25-MHz clock source (oscillator) connected to XI
- CONFIG[2:0] (pins 18, 29, 28) set to '000' (default setting)

3.12 MII Signal Definition (KSZ8041NL only)

Table 3-2 describes the MII signals. Refer to Clause 22 of the IEEE 802.3 specification for detailed information.

TABLE 3-2: MII SIGNAL DEFINITION

MII Signal Name	Direction (with respect to PHY, KSZ8041NL signal)	Direction (with respect to MAC)	Description
TXC	Output	Input	Transmit Clock (2.5 MHz for 10 Mbps, 25 MHz for 100 Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXC	Output	Input	Receive Clock (2.5 MHz for 10 Mbps, 25 MHz for 100 Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

3.12.1 TRANSMIT CLOCK (TXC)

TXC is sourced by the PHY. It is a continuous clock that provides the timing reference for Transmit Enable (TXEN) and Transmit Data [3:0] (TXD[3:0]).

TXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.12.2 TRANSMIT ENABLE (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXC following the final nibble of a frame.

TXEN transitions synchronously with respect to TXC.

3.12.3 TRANSMIT DATA [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXC. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is “00” to indicate idle when TXEN is deasserted. Values other than “00” on TXD[3:0] while TXEN is deasserted are ignored by the PHY.

3.12.4 RECEIVE CLOCK (RXC)

RXC provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10 Mbps mode, RXC is recovered from the line while the carrier is active. RXC is derived from the PHY’s reference clock when the line is idle or the link is down.
- In 100 Mbps mode, RXC is continuously recovered from the line. If the link is down, RXC is derived from the PHY’s reference clock.

RXC is 2.5 MHz for 10 Mbps operation and 25 MHz for 100 Mbps operation.

3.12.5 RECEIVE DATA VALID (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10 Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), “5D”, and remains asserted until the end of the frame.
- In 100 Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXC.

3.12.6 RECEIVE DATA [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

3.12.7 RECEIVE ERROR (RXER)

RXER is asserted for one or more RXC periods to indicate that a Symbol Error (for example, a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RXER transitions synchronously with respect to RXC. While RXDV is deasserted, RXER has no effect on the MAC.

3.12.8 CARRIER SENSE (CRS)

CRS is asserted and deasserted as follows:

- In 10 Mbps mode, CRS assertion is based on the reception of valid preambles. CRS deassertion is based on the reception of an end-of-frame (EOF) marker.
- In 100 Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is deasserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer deasserts CRS if IDLE symbols are received without /T/R.

3.12.9 COLLISION (COL)

COL is asserted in half-duplex mode whenever the transmitter and the receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXC and RXC.

3.13 Reduced MII (RMII) Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count MII. It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10 Mbps and 100 Mbps data rates
- Uses a 50-MHz reference clock
- Provides independent 2-bit wide (di-bit) transmit and receive data paths
- Contains two distinct groups of signals: one for transmission and the other for reception

The KSZ8041NL is configured in RMII mode after it is powered up or reset with the following:

- A 500MHz reference clock connected to REFCLK (pin 9)
- CONFIG[2:0] (pins 18, 29, 28) set to '001'

The KSZ8041RNL is configured in RMII mode and outputs the 50-MHz RMII reference clock to the MAC on REF_CLK (pin 19) after it is powered up or reset with the following:

- A 25-MHz crystal connected to XI (pin 9) and XO (pin 8), or a 25-MHz reference clock connected to XI (pin 9)
- CONFIG[2:0] (pins 18, 29, 28) set to '001'

In RMII mode, unused MII signals, TXD[3:2] (pins 27, 26), are tied to ground.

3.14 RMII Signal Definition

Table 3-3 and Table 3-4 describe the RMII signals for KSZ8041NL and KSZ8041RNL. Refer to RMII specification for detailed information.

TABLE 3-3: RMII SIGNAL DESCRIPTION – KSZ8041NL

RMII Signal Name	Direction (with respect to PHY, KSZ8041NL signal)	Direction (with respect to MAC)	Description
REF_CLK	Input	Input or Output	Synchronous 50-MHz clock reference for receive, transmit, and control interface
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RX_ER	Output	Input, or (not required)	Receive Error

TABLE 3-4: RMII SIGNAL DESCRIPTION – KSZ8041RNL

RMII Signal Name	Direction (with respect to PHY, KSZ8041RNL signal)	Direction (with respect to MAC)	Description
REF_CLK	Output	Input	Synchronous 50-MHz clock reference for receive, transmit, and control interface
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RX_ER	Output	Input, or (not required)	Receive Error

3.14.1 REFERENCE CLOCK (REF_CLK)

REF_CLK is a continuous 50-MHz clock that provides the timing reference for TX_EN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

The KSZ8041NL inputs the 50-MHz REF_CLK from the MAC or system board.

The KSZ8041RNL generates the 50MHz RMII REF_CLK and outputs it to the MAC.

3.14.2 TRANSMIT ENABLE (TX_EN)

TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII, and is negated prior to the first REF_CLK following the final di-bit of a frame.

TX_EN transitions synchronously with respect to REF_CLK.

3.14.3 TRANSMIT DATA [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] is accepted for transmission by the PHY. TXD[1:0] is “00” to indicate idle when TX_EN is deasserted. Values other than “00” on TXD[1:0] while TX_EN is deasserted are ignored by the PHY.

3.14.4 CARRIER SENSE/RECEIVE DATA VALID (CRS_DV)

CRS_DV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of a carrier. This is when a squelch is passed in 10 Mbps mode, and when two non-contiguous zeros in 10 bits are detected in 100 Mbps mode. Loss of carrier results in the deassertion of CRS_DV.

As long as carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit, and it is negated prior to the first REF_CLK that follows the final di-bit. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is “00” until proper receive signal decoding takes place.

3.14.5 RECEIVE DATA [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. RXD[1:0] is “00” to indicate idle when CRS_DV is deasserted. Values other than “00” on RXD[1:0] while CRS_DV is deasserted are ignored by the MAC.

3.14.6 RECEIVE ERROR (RX_ER)

RX_ER is asserted for one or more REF_CLK periods to indicate that a Symbol Error (for example,. a coding error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY.

RX_ER transitions synchronously with respect to REF_CLK. While CRS_DV is deasserted, RX_ER has no effect on the MAC.

3.14.7 COLLISION DETECTION

The MAC regenerates the COL signal of the MII from TX_EN and CRS_DV.

3.15 RMII Signal Diagram

The KSZ8041NL RMII pin connections to the MAC are shown in Figure 3-2.

FIGURE 3-2: KSZ8041NL RMII INTERFACE

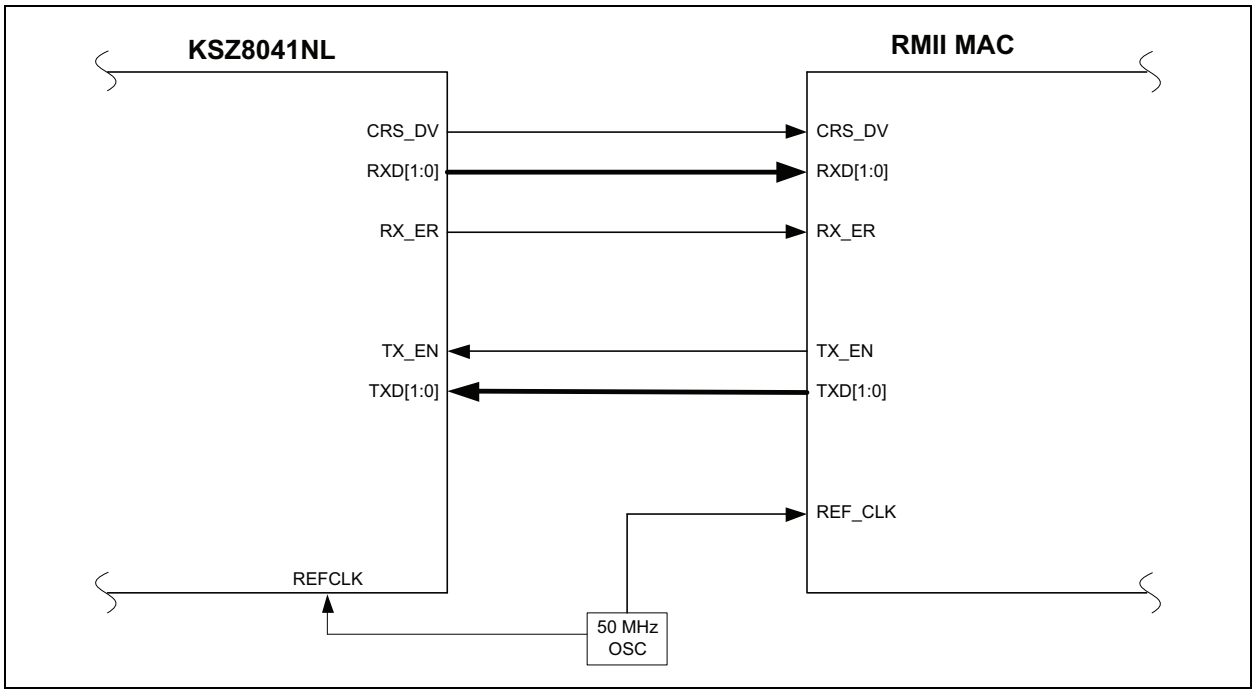
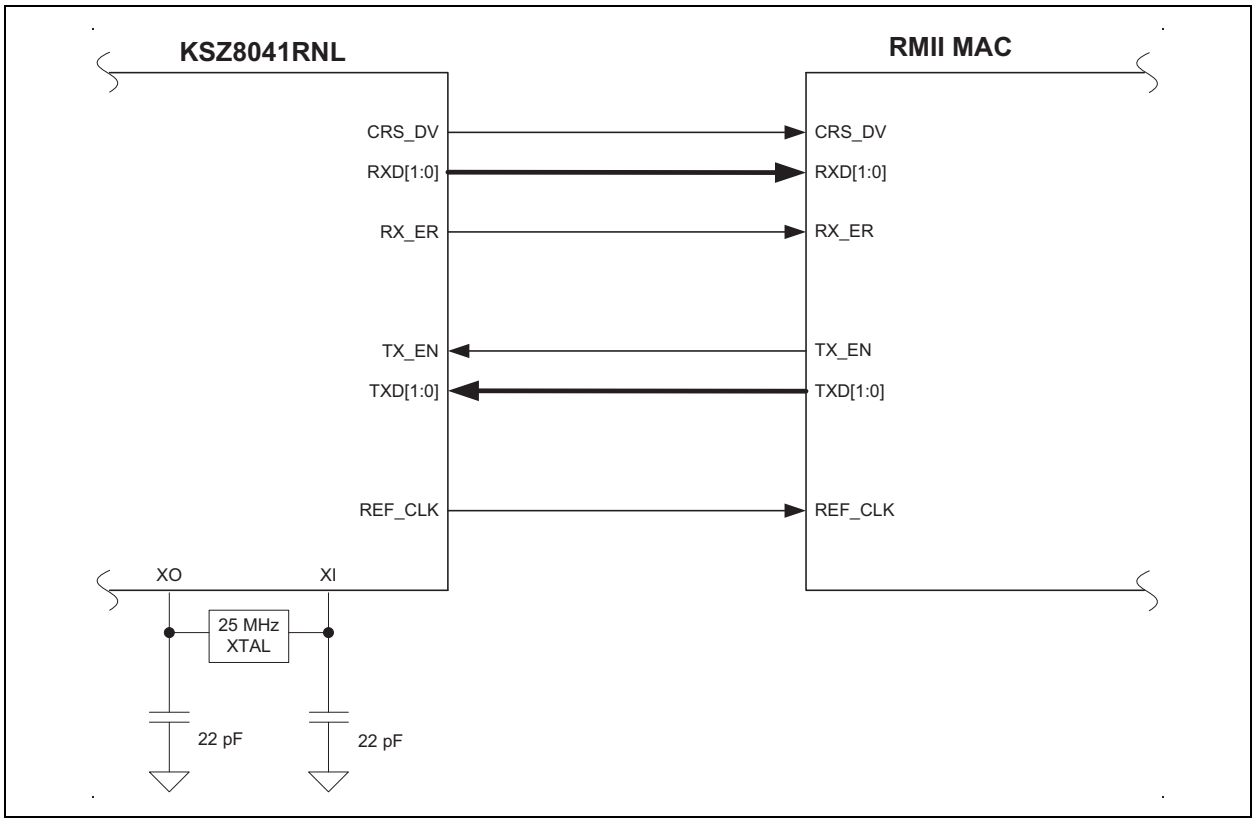


FIGURE 3-3: KSZ8041RNL RMII INTERFACE



3.16 HP Auto MDI/MDI-X

HP Auto MDI/MDI-X configuration eliminates the confusion of whether to use a straight cable or a crossover cable between the KSZ8041NL/RNL and its link partner. This feature allows the KSZ8041NL/RNL to use either type of cable to connect with a link partner that is in either MDI or MDI-X mode. The auto-sense function detects transmit and receive pairs from the link partner, and then assigns transmit and receive pairs of the KSZ8041NL/RNL accordingly.

HP Auto MDI/MDI-X is enabled by default. Writing “1” to register 1F bit 13 disables HP Auto MDI/MDL-X. Register 1F bit 14 selects MDI and MDI-X mode if HP Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support auto MDI/MDI-X.

The IEEE 802.3 Standard MDI and MDI-X is defined in Table 3-5.

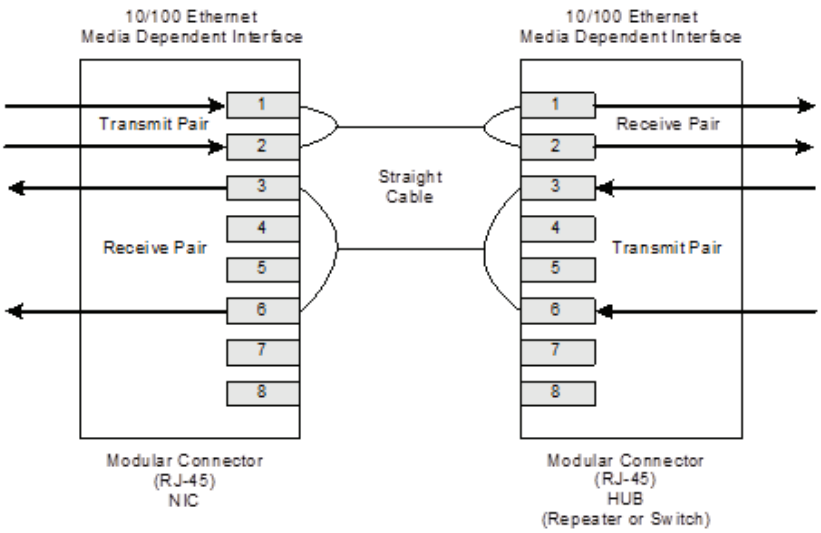
TABLE 3-5: MDI/MDI-X PIN DESCRIPTION

MDI		MDI-X	
RJ-45 Pin	**Signal**	**RJ-45 Pin**	**Signal**
1	TD+	1	RD+
2	TD–	2	RD–
3	RD+	3	TD+
6	RD–	6	TD–

3.16.1 STRAIGHT CABLE

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. Figure 3-4 depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

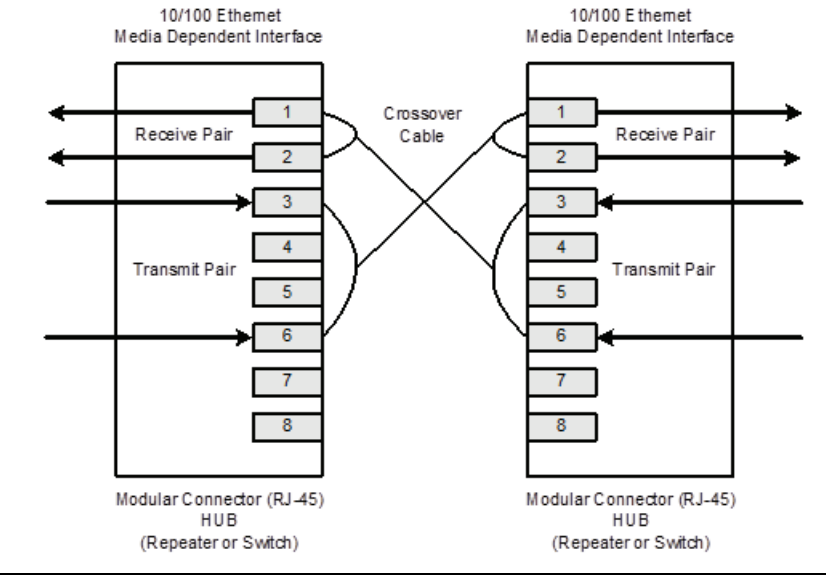
FIGURE 3-4: TYPICAL STRAIGHT CABLE CONNECTION



3.16.2 CROSSOVER CABLE

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. Table 3-4 depicts a typical crossover cable connection between two switches or hubs (two MDI-X devices).

FIGURE 3-5: TYPICAL CROSSOVER CABLE CONNECTION



3.17 Power Management

The KSZ8041NL/RNL offers the following two power management modes:

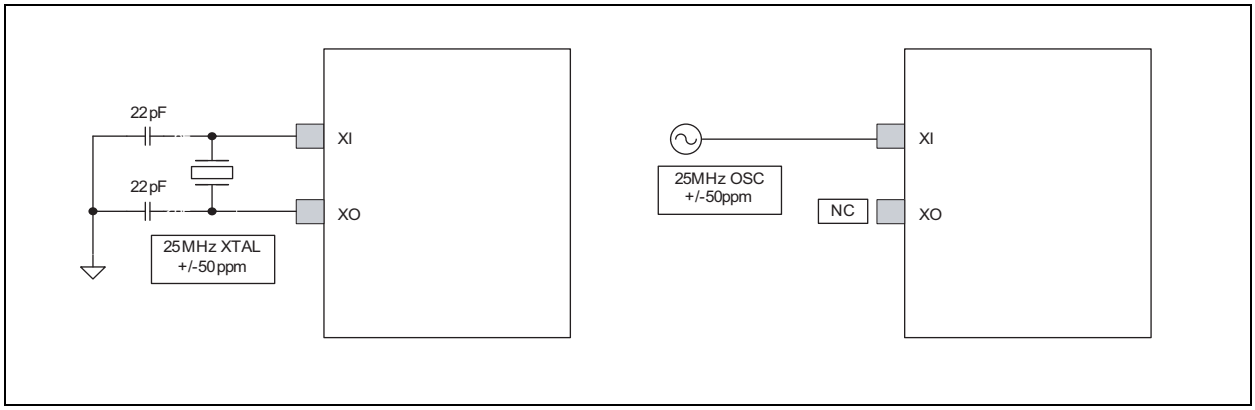
- Power Saving Mode
  This mode is used to reduce power consumption when the cable is unplugged. It is in effect when the auto-negotiation mode is enabled, the cable is disconnected, and register 1F bit 10 is set to 1. Under the power saving mode, the KSZ8041NL/RNL shuts down all transceiver blocks, except for transmitter, energy detect, and PLL circuits. Additionally, for the KSZ8041NL in MII mode, the RXC clock output is disabled. RXC clock is enabled after the cable is connected and a link is established.
  Power-saving mode is disabled by writing “0” to register 1F bit 10.
- Power-Down Mode
  This mode is used to power down the entire KSZ8041NL/RNL device when it is not in use. Power down mode is enabled by writing “1” to register 0 bit 11. In the power down state, the KSZ8041NL/RNL disables all internal functions, except for the MII management interface.

3.18 Reference Clock Connection Options

A crystal or clock source, such as an oscillator, is used to provide the reference clock for the KSZ8041NL/RNL.

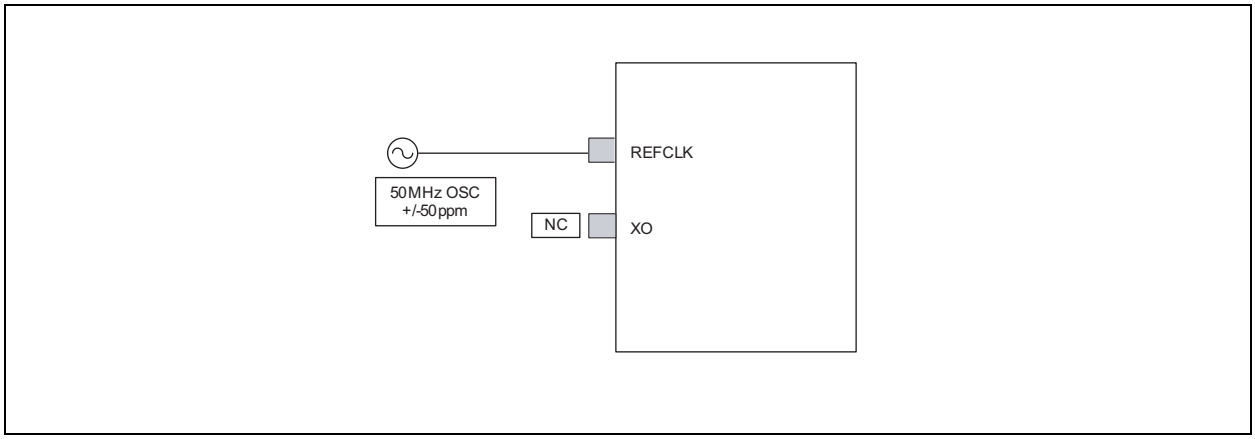
Figure 3-6 illustrates how to connect the 25-MHz crystal and oscillator reference clock.

FIGURE 3-6: 25-MHZ CRYSTAL/OSCILLATOR REFERENCE CLOCK



For the KSZ8041NL, Figure 3-7 illustrates how to connect the 50-MHz oscillator reference clock for RMII mode.

FIGURE 3-7: 50-MHZ OSCILLATOR REFERENCE CLOCK FOR KSZ8041NL RMII MODE



3.19 Reference Circuit for Power and Ground Connections

The KSZ8041NL/RNL is a single 3.3V supply device with a built-in 1.8V low-noise regulator. The power and ground connections are shown in Figure 3-8 and Table 3-6.

FIGURE 3-8: KSZ8041NL/RNL POWER AND GROUND CONNECTIONS

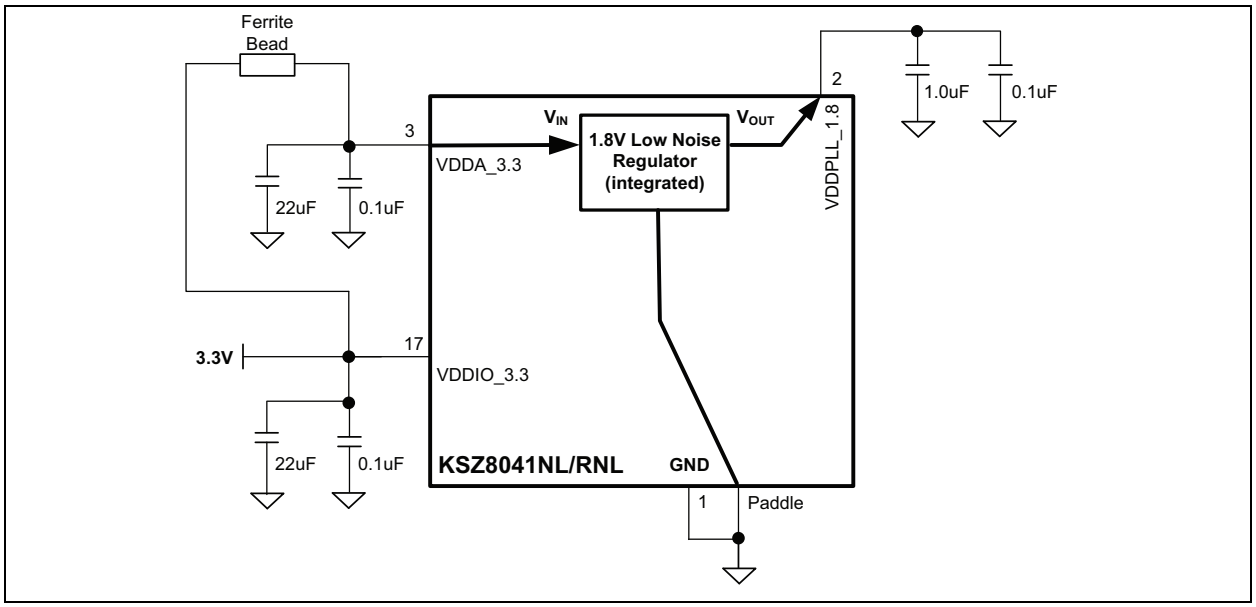


TABLE 3-6: KSZ8041NL/RNL POWER PIN DESCRIPTION

Power Pin	Pin Number	Description
VDDPLL_1.8	2	Decouple with 1.0 µF and 0.1 µF capacitors to ground.
VDDA_3.3	3	Connect to the board's 3.3V supply through ferrite bead.
VDDIO_3.3	17	Connect to the board's 3.3V supply.

4.0 REGISTERS

4.1 Register Map

Table 4-1 summarizes the register map.

TABLE 4-1: REGISTER MAP

Register Number (Hex)	Description
0h	Basic Control
1h	Basic Status
2h	PHY Identifier 1
3h	PHY Identifier 2
4h	Auto-Negotiation Advertisement
5h	Auto-Negotiation Link Partner Ability
6h	Auto-Negotiation Expansion
7h	Auto-Negotiation Next Page
8h	Link Partner Next Page Ability
9h – 13h	Reserved
14h	MII Control
15h	RXER Counter
16h – 1Ah	Reserved
1Bh	Interrupt Control/Status
1Ch – 1Dh	Reserved
1Eh	PHY Control 1
1Fh	PHY Control 2

4.2 Register Descriptions

Table 4-2 provides a list of supported registers and their descriptions.

TABLE 4-2: REGISTER DESCRIPTIONS

Address	Name	Description	Mode (Note 4-1)	Default
Register 0h – Basic Control				
0.15	Reset	1 = Software reset 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.14	Loop-Back	1 = Loop-back mode 0 = Normal operation	RW	0
0.13	Speed Select (LSB)	1 = 100 Mbps 0 = 10 Mbps This bit is ignored if auto-negotiation is enabled (register 0.12 = 1).	RW	Set by SPEED strapping pin. See Table 2-2 and Table 2-4 for details.
0.12	Auto-Negotiation Enable	1 = Enable auto-negotiation process 0 = Disable auto-negotiation process If enabled, auto-negotiation result overrides the settings in register 0.13 and 0.8.	RW	Set by NWAYEN strapping pin. See Table 2-2 and Table 2-4 for details.
0.11	Power Down	1 = Power-down mode 0 = Normal operation	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII and TX+/TX- 0 = Normal operation	RW	Set by ISO strapping pin. See Table 2-2 and Table 2-4 for details.
0.9	Restart Auto-Negotiation	1 = Restart auto-negotiation process 0 = Normal operation This bit is self-cleared after a '1' is written to it.	RW/SC	0
0.8	Duplex Mode	1 = Full-duplex 0 = Half-duplex	RW	Inverse of DUPLEX strapping pin value. See Table 2-2 and Table 2-4 for details.
0.7	Collision Test	1 = Enable COL test 0 = Disable COL test	RW	0
0.6:1	Reserved		RO	000_000
0.0	Disable Transmitter	0 = Enable transmitter 1 = Disable transmitter	RW	0
Register 1h – Basic Status				
1.15	100BASE-T4	1 = T4 capable 0 = Not T4 capable	RO	0
1.14	100BASE-TX Full Duplex	1 = Capable of 100 Mbps full-duplex 0 = Not capable of 100 Mbps full-duplex	RO	1

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
1.13	100BASE-TX Half Duplex	1 = Capable of 100 Mbps half-duplex 0 = Not capable of 100 Mbps half-duplex	RO	1
1.12	10BASE-T Full Duplex	1 = Capable of 10 Mbps full-duplex 0 = Not capable of 10 Mbps full-duplex	RO	1
1.11	10BASE-T Half Duplex	1 = Capable of 10 Mbps half-duplex 0 = Not capable of 10 Mbps half-duplex	RO	1
1.10:7	Reserved	—	RO	0000
1.6	No Preamble	1 = Preamble suppression 0 = Normal preamble	RO	1
1.5	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RO	0
1.4	Remote Fault	1 = Remote fault 0 = No remote fault	RO/LH	0
1.3	Auto-Negotiation Ability	1 = Capable to perform auto-negotiation 0 = Not capable to perform auto-negotiation	RO	1
1.2	Link Status	1 = Link is up 0 = Link is down	RO/LL	0
1.1	Jabber Detect	1 = Jabber detected 0 = Jabber not detected (default is low)	RO/LH	0
1.0	Extended Capability	1 = Supports extended capabilities registers	RO	1
Register 2h – PHY Identifier 1				
2.15.0	PHY ID Number	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0022h
Register 3h – PHY Identifier 2				
3.15:10	PHY ID Number	Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI). Kendin Communication's OUI is 0010A1 (hex)	RO	0001_01
3.9:4	Model Number	Six bit manufacturer's model number	RO	01_0001
3.3:0	Revision Number	Four bit manufacturer's revision number	RO	Indicates silicon revision

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
Register 4h – Auto-Negotiation Advertisement				
4.15	Next Page	1 = Next page capable 0 = No next page capability	RW	0
4.14	Reserved	—	RO	0
4.13	Remote Fault	1 = Remote fault supported 0 = No remote fault	RW	0
4.12	Reserved	—	RO	0
4.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RW	00
4.9	100BASE-T4	1 = T4 capable 0 = No T4 capability	RO	0
4.8	100BASE-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100 Mbps full-duplex capability	RW	Set by SPEED strapping pin. See Table 2-2 and Table 2-4 for details.
4.7	100BASE-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RW	Set by SPEED strapping pin. See Table 2-2 and Table 2-4 for details.
4.6	10BASE-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RW	1
4.5	10BASE-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RW	1
4.4:0	Selector Field	[00001] = IEEE 802.3	RW	0_0001
Register 5h – Auto-Negotiation Link Partner Ability				
5.15	Next Page	1 = Next page capable 0 = No next page capability	RO	0
5.14	Acknowledge	1 = Link code word received from partner 0 = Link code word not yet received	RO	0
5.13	Remote Fault	1 = Remote fault detected 0 = No remote fault	RO	0
5.12	Reserved	—	RO	0
5.11:10	Pause	[00] = No PAUSE [10] = Asymmetric PAUSE [01] = Symmetric PAUSE [11] = Asymmetric & Symmetric PAUSE	RO	00
5.9	100BASE-T4	1 = T4 capable 0 = No T4 capability	RO	0
5.8	100BASE-TX Full-Duplex	1 = 100 Mbps full-duplex capable 0 = No 100 Mbps full-duplex capability	RO	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
5.7	100BASE-TX Half-Duplex	1 = 100 Mbps half-duplex capable 0 = No 100 Mbps half-duplex capability	RO	0
5.6	10BASE-T Full-Duplex	1 = 10 Mbps full-duplex capable 0 = No 10 Mbps full-duplex capability	RO	0
5.5	10BASE-T Half-Duplex	1 = 10 Mbps half-duplex capable 0 = No 10 Mbps half-duplex capability	RO	0
5.4:0	Selector Field	[00001] = IEEE 802.3	RO	0_0001
Register 6h – Auto-Negotiation Expansion				
6.15:5	Reserved	—	RO	0000_0000_000
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection 0 = No fault detected by parallel detection.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner has next page capability 0 = Link partner does not have next page capability	RO	0
6.2	Next Page Able	1 = Local device has next page capability 0 = Local device does not have next page capability	RO	1
6.1	Page Received	1 = New page received 0 = New page not received yet	RO/LH	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner has auto-negotiation capability 0 = Link partner does not have auto-negotiation capability	RO	0
Register 7h – Auto-Negotiation Next Page				
7.15	Next Page	1 = Additional next page(s) will follow 0 = Last page	RW	0
7.14	Reserved	—	RO	0
7.13	Message Page	1 = Message page 0 = Unformatted page	RW	1
7.12	Acknowledge2	1 = Will comply with message 0 = Cannot comply with message	RW	0
7.11	Toggle	1 = Previous value of the transmitted link code word equaled logic one 0 = Logic zero	RO	0
7.10:0	Message Field	11-bit wide field to encode 2048 messages	RW	000_0000_0001

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
Register 8h – Link Partner Next Page Ability				
8.15	Next Page	1 = Additional Next Page(s) will follow 0 = Last page	RO	0
8.14	Acknowledge	1 = Successful receipt of link word 0 = No successful receipt of link word	RO	0
8.13	Message Page	1 = Message page 0 = Unformatted page	RO	0
8.12	Acknowledge2	1 = Able to act on the information 0 = Not able to act on the information	RO	0
8.11	Toggle	1 = Previous value of transmitted link code word equal to logic zero 0 = Previous value of transmitted link code word equal to logic one	RO	0
8.10:0	Message Field	—	RO	000_0000_0000
Register 14h – MII Control				
14.15:8	Reserved	—	RO	0000_0000
14.7	100BASE-TX Preamble Restore	1 = Restore received preamble to MII output (random latency) 0 = Consume 1-byte preamble before sending frame to MII output for fixed latency	RW	0 or 1 (if CONFIG[2:0] = 100) See Table 2-2 and Table 2-4 for details.
14.6	10BASE-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all 7-bytes of preamble before sending frame (starting with SFD) to MII output	RW	0
14.5:0	Reserved	—	RO	00_0001
Register 15h – RXER Counter				
15.15:0	RXER Counter	Receive error counter for Symbol Error frames	RO/SC	000h
Register 1Bh – Interrupt Control/Status				
1b.15	Jabber Interrupt Enable	1 = Enable Jabber Interrupt 0 = Disable Jabber Interrupt	RW	0
1b.14	Receive Error Interrupt Enable	1 = Enable Receive Error Interrupt 0 = Disable Receive Error Interrupt	RW	0
1b.13	Page Received Interrupt Enable	1 = Enable Page Received Interrupt 0 = Disable Page Received Interrupt	RW	0
1b.12	Parallel Detect Fault Interrupt Enable	1 = Enable Parallel Detect Fault Interrupt 0 = Disable Parallel Detect Fault Interrupt	RW	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
1b.11	Link Partner Acknowledge Interrupt Enable	1 = Enable Link Partner Acknowledge Interrupt 0 = Disable Link Partner Acknowledge Interrupt	RW	0
1b.10	Link Down Interrupt Enable	1= Enable Link Down Interrupt 0 = Disable Link Down Interrupt	RW	0
1b.9	Remote Fault Interrupt Enable	1 = Enable Remote Fault Interrupt 0 = Disable Remote Fault Interrupt	RW	0
1b.8	Link Up Interrupt Enable	1 = Enable Link Up Interrupt 0 = Disable Link Up Interrupt	RW	0
1b.7	Jabber Interrupt	1 = Jabber occurred 0 = Jabber did not occur	RO/SC	0
1b.6	Receive Error Interrupt	1 = Receive Error occurred 0 = Receive Error did not occur	RO/SC	0
1b.5	Page Receive Interrupt	1 = Page Receive occurred 0 = Page Receive did not occur	RO/SC	0
1b.4	Parallel Detect Fault Interrupt	1 = Parallel Detect Fault occurred 0 = Parallel Detect Fault did not occur	RO/SC	0
1b.3	Link Partner Acknowledge Interrupt	1= Link Partner Acknowledge occurred 0= Link Partner Acknowledge did not occur	RO/SC	0
1b.2	Link Down Interrupt	1= Link Down occurred 0= Link Down did not occur	RO/SC	0
1b.1	Remote Fault Interrupt	1= Remote Fault occurred 0= Remote Fault did not occur	RO/SC	0
1b.0	Link Up Interrupt	1= Link Up occurred 0= Link Up did not occur	RO/SC	0
Register 1Eh – PHY Control 1				
1e:15:14	LED mode	[00] = LED1 : Speed LED0 : Link/Activity [01] = LED1 : Activity LED0 : Link [10], [11] = Reserved	RW	00
1e.13	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed	RO	—
1e.12	Reserved	—	RO	0
1e.11	MDI/MDI-X State	0 = MDI 1 = MDI-X	RO	—
1e:10:8	Reserved	—	—	—
1e:7	Remote loopback	0 = Normal mode 1 = Remote (analog) loop back is enabled	RW	0

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
1e:6:0	Reserved	—	—	—
Register 1Fh – PHY Control 2				
1f:15	HP_MDIX	0 = Auto MDI/MDI-X mode 1 = HP Auto MDI/MDI-X mode	RW	1
1f:14	MDI/MDI-X Select	When Auto MDI/MDI-X is disabled, 0 = MDI mode Transmit on TX+/- (pins 7, 6) and Receive on RX+/- (pins 5, 4) 1 = MDI-X mode Transmit on RX+/- (pins 5,4) and Receive on TX+/- (pins 7, 6)	RW	0
1f:13	Pair Swap Disable	1 = Disable auto MDI/MDI-X 0 = Enable auto MDI/MDI-X	RW	0
1f.12	Energy Detect	1 = Presence of signal on RX+/- analog wire pair 0 = No signal detected on RX+/-	RO	0
1f.11	Force Link	1 = Force link pass 0 = Normal link operation This bit bypasses the control logic and allows the transmitter to send a pattern even if there is no link.	RW	0
Register 1Fh – PHY Control 2 (Continued)				
1f.10	Power Saving	1 = Enable power saving 0 = Disable power saving If power saving mode is enabled and the cable is disconnected, the RXC clock output (in MII mode) is disabled. RXC clock is enabled after the cable is connected and a link is established.	RW	0
1f.9	Interrupt Level	1 = Interrupt pin active high 0 = Interrupt pin active low	RW	0
1f.8	Enable Jabber	1 = Enable jabber counter 0 = Disable jabber counter	RW	1
1f.7	Auto-Negotiation Complete	1 = Auto-negotiation process completed 0 = Auto-negotiation process not completed	RW	0
1f.6	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1f.5	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RO	0
1f.4:2	Operation Mode Indication	[000] = Still in auto-negotiation [001] = 10 BASE-T half-duplex [010] = 100 BASE-TX half-duplex [011] = Reserved [101] = 10 BASE-T full-duplex [110] = 100 BASE-TX full-duplex [111] = Reserved	RO	000

TABLE 4-2: REGISTER DESCRIPTIONS (CONTINUED)

Address	Name	Description	Mode (Note 4-1)	Default
1f.1	Enable SQE test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1f.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Note 4-1 RW = Read/Write
RO = Read only
SC = Self-cleared
LH = Latch high
LL = Latch low

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings (Note 5-1)

Supply Voltage ($V_{DDPLL\_1.8}$) ..... –0.5V to +2.4V

Supply Voltage ($V_{DDPLL\_3.3}$, $V_{DDPLL\_3.3}$) ..... –0.5V to +4.0V

Input Voltage (all inputs) ..... –0.5V to +4.0V

Output Voltage (all outputs) ..... –0.5V to +4.0V

Storage Temperature (T_S) ..... –55°C to +150°C

ESD Performance Rating (Note 5-2) ..... +6 kV

5.2 Operating Ratings (Note 5-3)

Supply Voltage ($V_{DDIO\_3.3}$, $V_{DDA\_3.3}$) ..... +3.135V to +3.465V

Ambient Temperature

(T_A, Commercial) ..... 0°C to +70°C

(T_A, Industrial) ..... –40°C to +85°C

(T_A, Automotive Qualified) ..... –40°C to +85°C

Maximum Junction Temperature (T_J maximum) ..... +125°C

Thermal Resistance (θ_{JA}) ..... 34°C/W

Thermal Resistance (θ_{JC}) ..... 6°C/W

Note 5-1 Exceeding the absolute maximum rating may damage the device. Stresses greater than the absolute maximum rating may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Note 5-2 Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

Note 5-3 The device is not guaranteed to function outside its operating rating.

6.0 ELECTRICAL CHARACTERISTICS

TABLE 6-1: ELECTRICAL CHARACTERISTICS (Note 6-1, Note 6-2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD1}	100BASE-TX	Chip only (no transformer); Full-duplex traffic @ 100% utilization	—	53.0	—	mA
I_{DD2}	10BASE-T	Chip only (no transformer); Full-duplex traffic @ 100% utilization	—	38.0	—	mA
I_{DD3}	Power-Saving Mode	Ethernet cable disconnected (reg. 1F.10 = 1)	—	32.0	—	mA
I_{DD4}	Power-Down Mode	Software power-down (reg. 0.11 = 1)	—	4.0	—	mA
TTL Inputs						
V_{IH}	Input High Voltage	—	2.0	—	—	V
V_{IL}	Input Low Voltage	—	—	—	0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ VDDIO	—	–10	10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 4 mA	—	—	0.4	V
$\|I_{oz}\|$	Output Tri-State Leakage	—	—	—	10	µA
LED Outputs						
I_{LED}	Output Drive Current	Each LED pin (LED0, LED1)	—	8	—	mA
100BASE-TX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination across differential output	0.95	—	1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination across differential output	—	—	2	%
t_r, t_f	Rise/Fall Time	—	3	—	5	ns
	Rise/Fall Time Imbalance	—	0	—	0.5	ns
	Duty Cycle Distortion	—	—	—	±0.25	ns
	Overshoot	—	—	—	5	%
V_{SET}	Reference Voltage of ISET	—	—	0.65	—	V
—	Output Jitter	Peak-to-peak	—	0.7	1.4	ns
10BASE-T Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	100Ω termination across differential output	2.2	—	2.8	V
—	Jitter Added	Peak-to-peak	—	—	3.5	ns
t_r, t_f	Rise/Fall Time	—	—	25	—	ns
10BASE-T Receive						
V_{SQ}	Squelch Threshold	5 MHz square wave	—	400	—	mV

Note 6-1 Current consumption is for the single 3.3V supply KSZ8041NL/RNL device only, and includes the 1.8V supply voltage (VDDPLL_1.8) that is provided by the KSZ8041NL/RNL. The PHY port's transformer consumes an additional 45 mA @ 3.3V for 100BASE-TX and 70 mA @ 3.3V for 10BASE-T.

Note 6-2 T_A = 25°C. Specification for packaged product only.

7.0 TIMING DIAGRAMS

7.1 MII SQE Timing

FIGURE 7-1: MII SQE TIMING (10BASE-T)

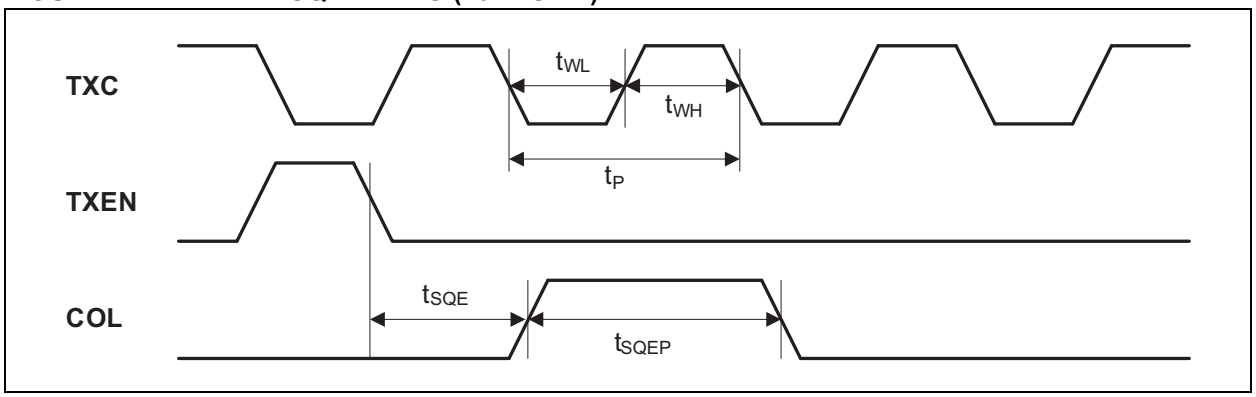


TABLE 7-1: MII SQE TIMING (10BASE-T) PARAMETERS

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC Period	—	400	—	ns
t_{WL}	TXC Pulse Width Low	—	200	—	ns
t_{WH}	TXC Pulse Width High	—	200	—	ns
t_{SQE}	COL (SQE) Delay After TXEN De-Asserted	—	2.5	—	us
t_{SQEP}	COL (SQE) Pulse Duration	—	1.0	—	us

7.2 MII Transmit Timing (10BASE-T)

FIGURE 7-2: MII TRANSMIT TIMING (10BASE-T)

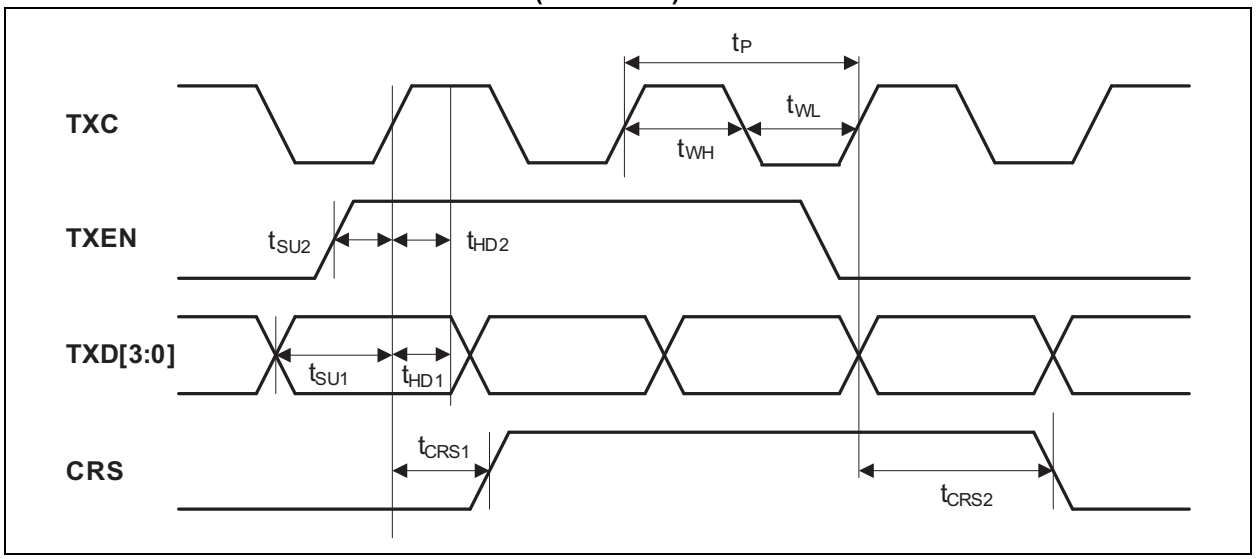


TABLE 7-2: MII TRANSMIT TIMING (10BASE-T) PARAMETERS

Timing Parameter	Description	Min.	Typ.	Max.	Units
t_P	TXC Period	—	400	—	ns
t_{WL}	TXC Pulse Width Low	—	200	—	ns
t_{WH}	TXC Pulse Width High	—	200	—	ns
t_{SU1}	TXD[3:0] Setup to Rising Edge of TXC	10	—	—	ns
t_{SU2}	TXEN Setup to Rising Edge of TXC	10	—	—	ns
t_{HD1}	TXD[3:0] Hold from Rising Edge of TXC	0	—	—	ns
t_{HD2}	TXEN Hold from Rising Edge of TXC	0	—	—	ns
t_{CRS1}	TXEN High to CRS Asserted Latency	—	160	—	ns
t_{CRS2}	TXEN Low to CRS De-Asserted Latency	—	510	—	ns

7.3 MII Receive Timing (10BASE-T)

FIGURE 7-3: MII RECEIVE TIMING (10BASE-T)

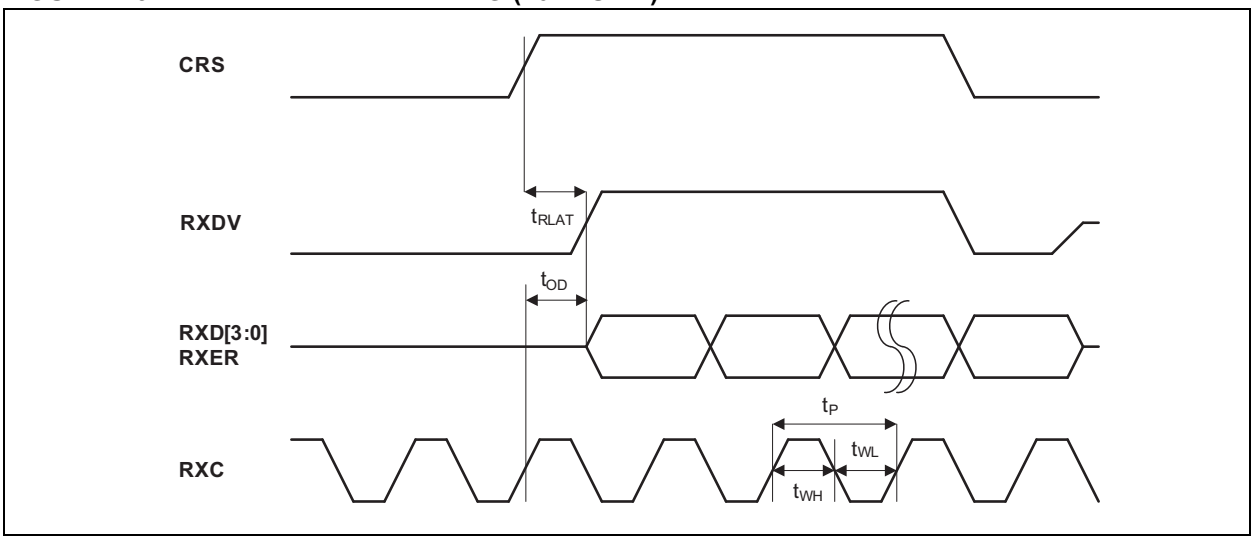


TABLE 7-3: MII RECEIVE TIMING (10BASE-T) PARAMETERS

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	RXC Period	—	400	—	ns
t_{WL}	RXC Pulse Width Low	—	200	—	ns
t_{WH}	RXC Pulse Width High	—	200	—	ns
t_{OD}	(RXD[3:0], RXER, RXDV) Output Delay from Rising Edge of RXC	182	—	225	ns
t_{RLAT}	CRS to (RXD[3:0], RXER, RXDV) Latency	—	6.5	—	µs

7.4 MII Transmit Timing (100BASE-TX)

FIGURE 7-4: MII TRANSMIT TIMING (100BASE-TX)

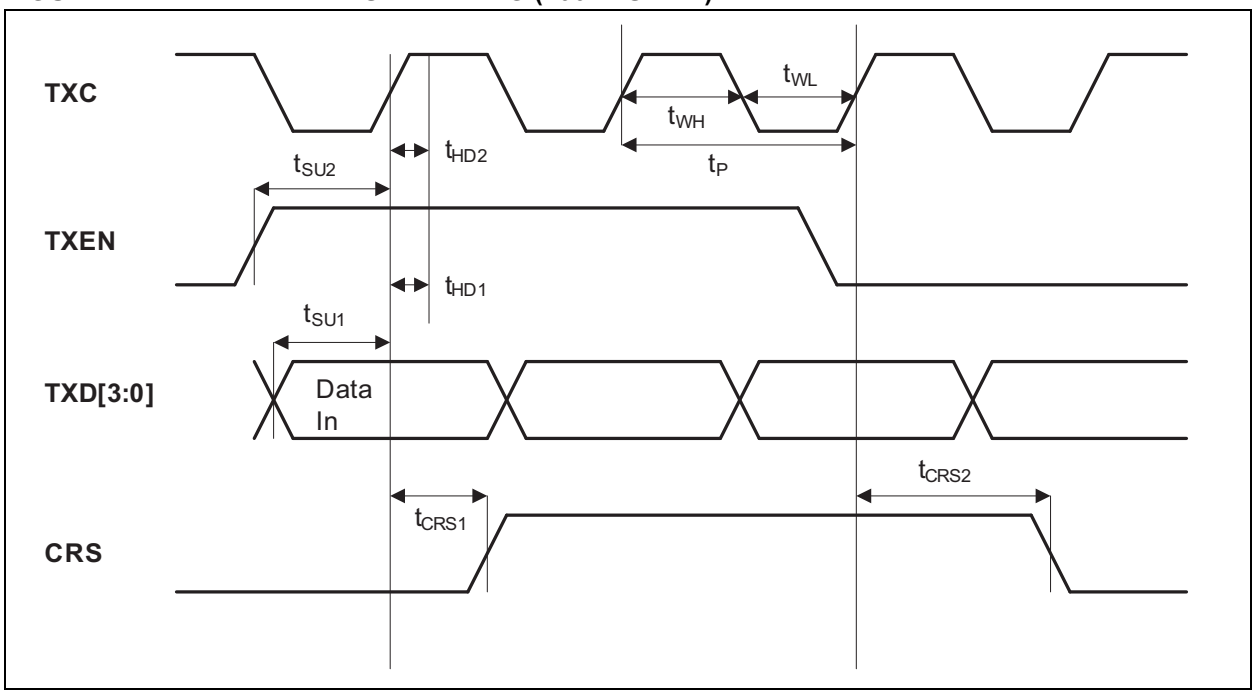


TABLE 7-4: MII TRANSMIT TIMING (100BASE-TX) PARAMETERS

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	TXC Period	—	40	—	ns
t_{WL}	TXC Pulse Width Low	—	20	—	ns
t_{WH}	TXC Pulse Width High	—	20	—	ns
t_{SU1}	TXD[3:0] Setup to Rising Edge of TXC	10	—	—	ns
t_{SU2}	TXEN Setup to Rising Edge of TXC	10	—	—	ns
t_{HD1}	TXD[3:0] Hold from Rising Edge of TXC	0	—	—	ns
t_{HD2}	TXEN Hold from Rising Edge of TXC	0	—	—	ns
t_{CRS1}	TXEN High to CRS Asserted Latency	—	34	—	ns
t_{CRS2}	TXEN Low to CRS De-Asserted Latency	—	33	—	ns

7.5 MII Receive Timing (100BASE-TX)

FIGURE 7-5: MII RECEIVE TIMING (100BASE-TX)

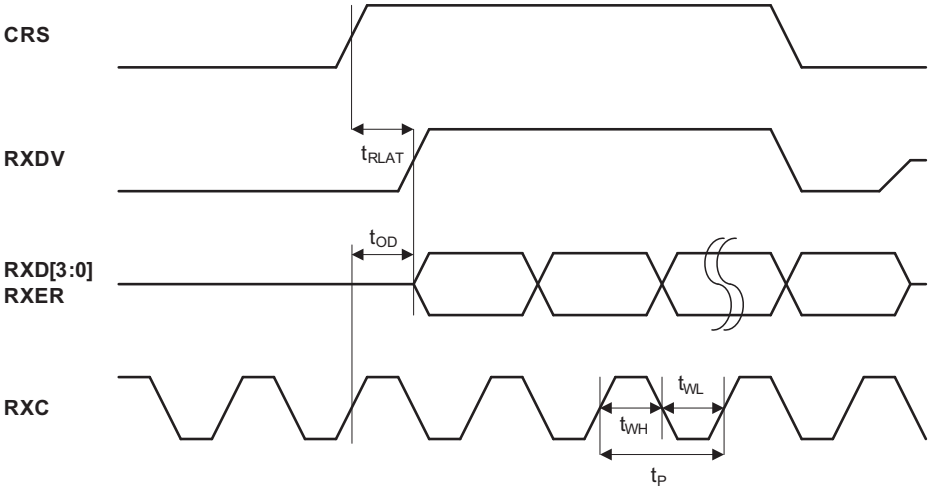


TABLE 7-5: MII RECEIVE TIMING (100BASE-TX) PARAMETERS

Timing Parameter	Description	Min.	Typ	Max.	Units
t_P	RXC Period	—	40	—	ns
t_{WL}	RXC Pulse Width Low	—	20	—	ns
t_{WH}	RXC Pulse Width High		20	—	ns
t_{OD}	(RXD[3:0], RXER, RXDV) Output Delay from Rising Edge of RXC	19	—	25	ns
t_{RLAT}	CRS to RXDV Latency	—	140	—	ns
	CRS to RXD[3:0] Latency	—	52	—	ns
	CRS to RXER Latency	—	60	—	ns

7.6 RMII Timing

FIGURE 7-6: RMII TIMING – DATA RECEIVED FROM RMII

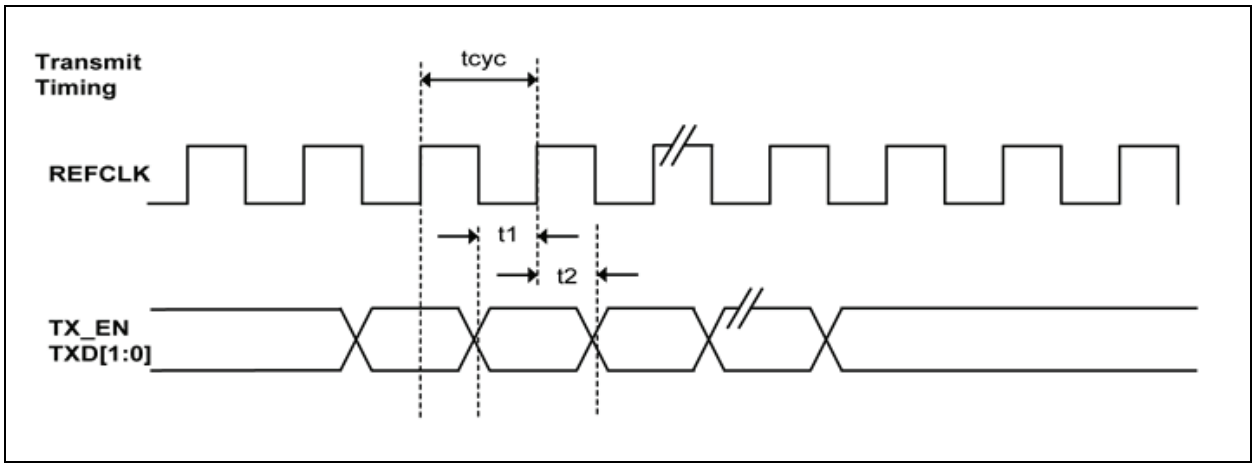


FIGURE 7-7: RMII TIMING – DATA INPUT TO RMII

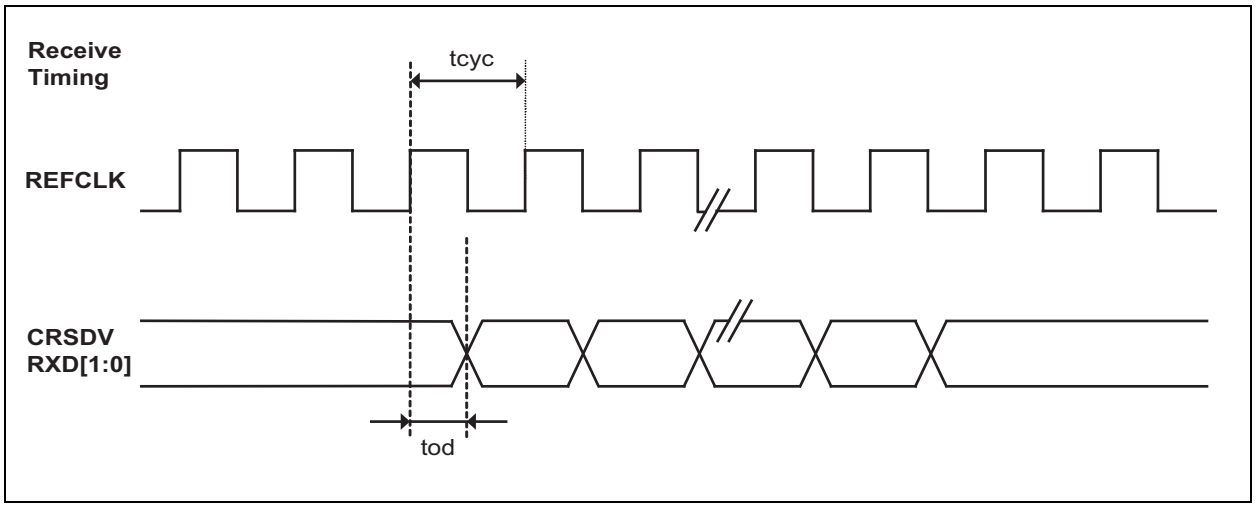


TABLE 7-6: RMII TIMING PARAMETERS – KSZ8041NL

Timing Parameter	Description	Min.	Typ	Max.	Units
t_{cyc}	Clock Cycle	—	20	—	ns
t_1	Setup Time	4	—	—	ns
t_2	Hold Time	2	—	—	ns
t_{od}	Output Delay	3	—	9	ns

TABLE 7-7: RMII TIMING PARAMETERS – KSZ8041RNL

Timing Parameter	Description	Min.	Typ	Max.	Units
t_{cyc}	Clock Cycle	—	20	—	ns
t_1	Setup Time	4	—	—	ns
t_2	Hold Time	1	—	—	ns
t_{od}	Output Delay	9	11	13	ns

7.7 Auto-Negotiation Timing

FIGURE 7-8: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

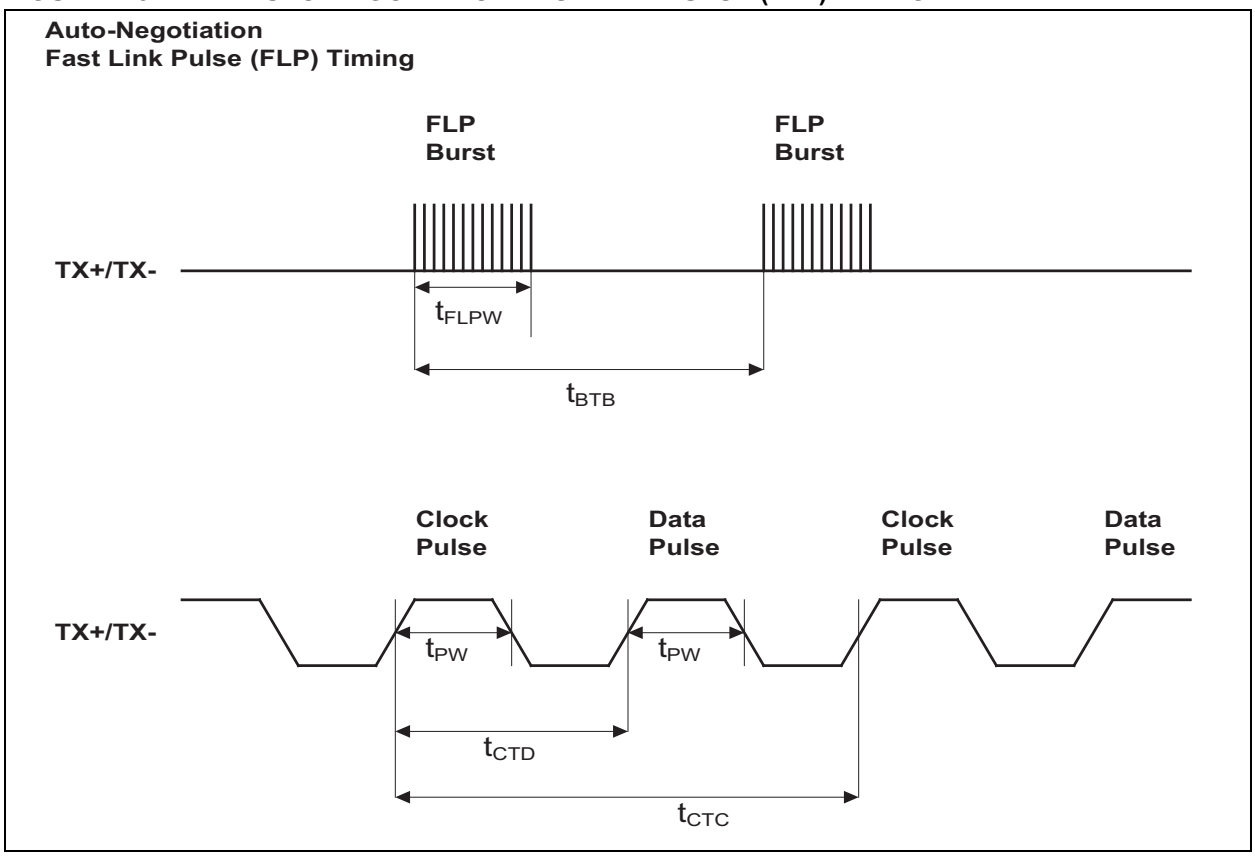


TABLE 7-8: AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING PARAMETERS

Timing Parameter	Description	Min.	Typ	Max.	Units
t_{BTB}	FLP Burst to FLP Burst	8	16	24	ms
t_{FLPW}	FLP Burst Width	—	2	—	ms
t_{PW}	Clock/Data Pulse Width	—	100	—	ns
t_{CTD}	Clock Pulse to Data Pulse	55.5	64	69.5	µs
t_{CTC}	Clock Pulse to Clock Pulse	111	128	139	µs
—	Number of Clock/Data Pulse per FLP Burst	17	—	33	—

7.8 MDC/MDIO Timing

FIGURE 7-9: MDC/MDIO TIMING

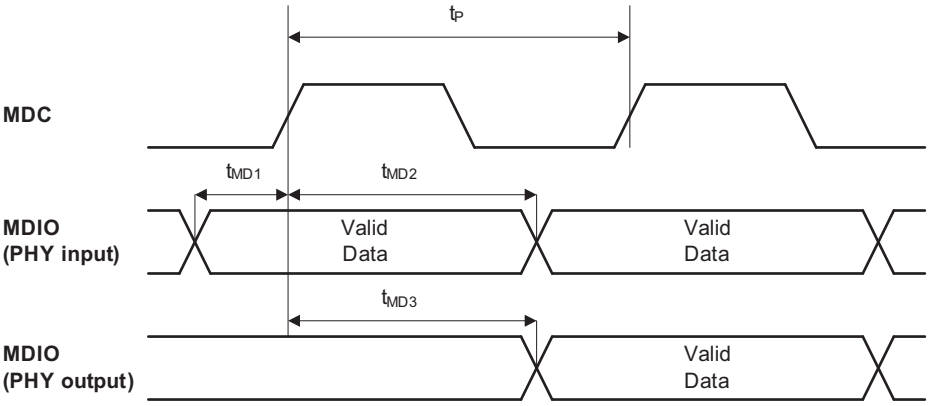


TABLE 7-9: MDC/MDIO TIMING PARAMETERS

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	MDC Period	—	400	—	ns
t_{1MD1}	MDIO (PHY Input) Setup to Rising Edge of MDC	10	—	—	ns
t_{MD2}	MDIO (PHY Input) Hold from Rising Edge of MDC	4	—	—	ns
t_{MD3}	MDIO (PHY Output) Delay from Rising Edge of MDC	—	222	—	ns

7.9 Power-Up/Reset Timing

The KSZ8041NL/RNL reset timing requirement is summarized in Figure 7-10 and Figure 7-10.

FIGURE 7-10: POWER-UP/RESET TIMING

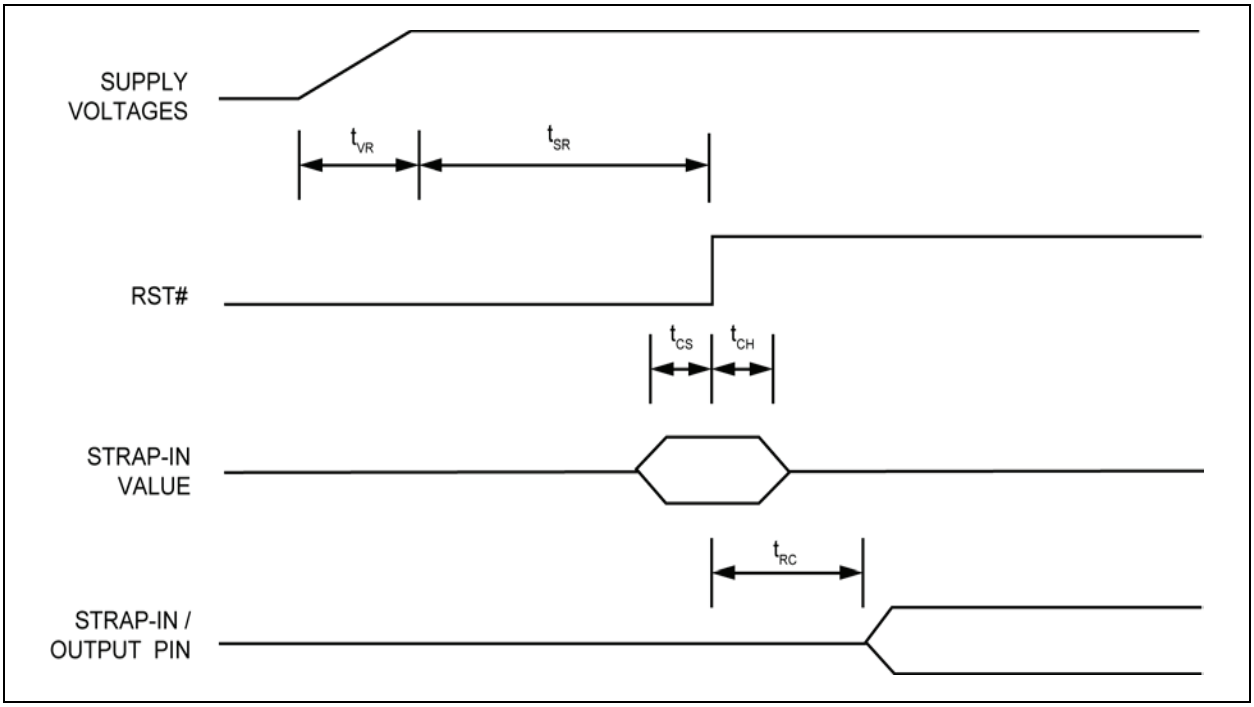


TABLE 7-10: POWER-UP/RESET TIMING PARAMETERS

Parameters	Description	Min	Max	Units
t_{VR}	Supply Voltage (V_{DDIO}_3.3, V_{DDA}_3.3) Rise Time	250	—	µs
t_{sr}	Stable Supply Voltage to Reset High	10	—	ms
t_{cs}	Configuration Setup Time	5	—	ns
t_{ch}	Configuration Hold Time	5	—	ns
t_{rc}	Reset to Strap-In Pin Output	6	—	ns

The supply voltage (V_{DDIO}_3.3 and V_{DDA}_3.3) power-up waveform should be monotonic. The 250 µs minimum rise time is from 10% to 90%.

After the deassertion of reset, it is recommended to wait a minimum of 100 µs before starting programming on the MIIM (MDC/MDIO) Interface.

7.10 Reset Circuit

The reset circuit in Figure 7-11 is recommended for powering up the KSZ8041NL/RNL if reset is triggered by the power supply.

FIGURE 7-11: RECOMMENDED RESET CIRCUIT

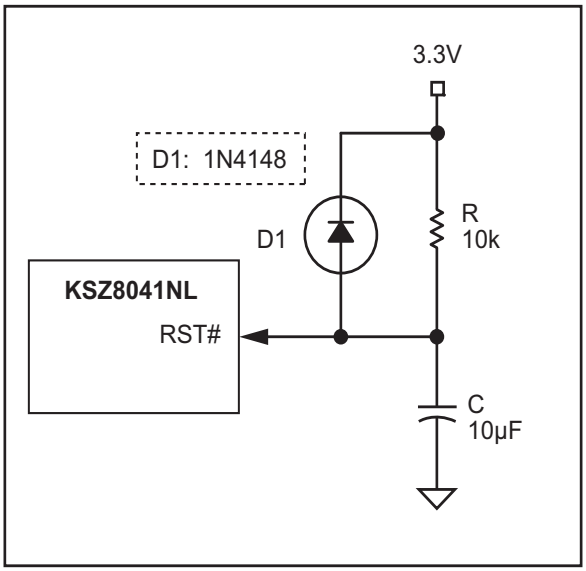
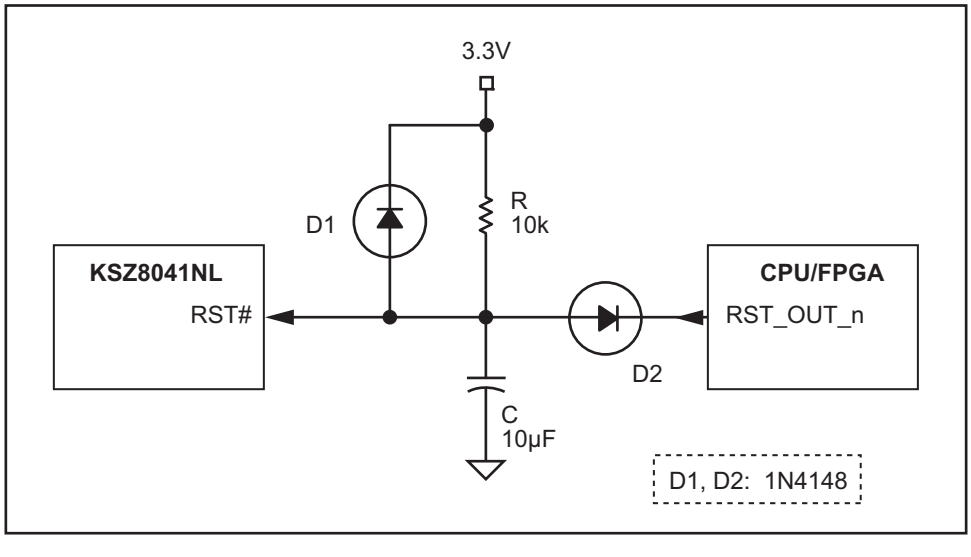


Figure 7-12 shows a reset circuit recommended for applications where reset is driven by another device (for example, the CPU or an FPGA). The reset out RST_OUT_n from CPU/FPGA provides the warm reset after power up reset. D2 is required if using different VDDIO voltage between the switch and CPU/FPGA. Diode D2 should be selected to provide maximum 0.3V V_F (Forward Voltage), for example, VISHAY BAT54, MSS1P2L. Alternatively, a level shifter device can also be used. D2 is not required if PHY and CPU/FPGA use same V_{DDIO} voltage.

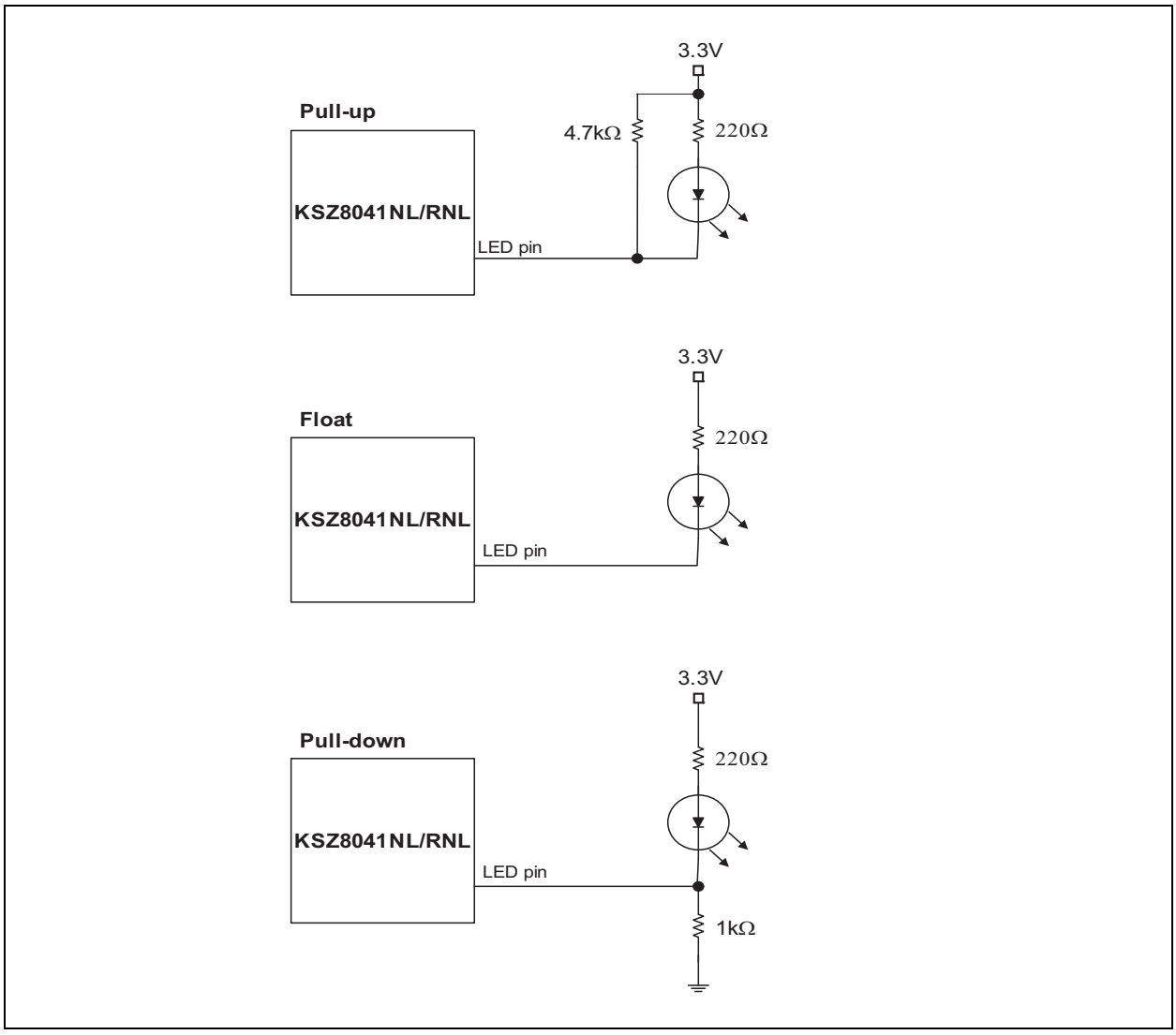
FIGURE 7-12: RECOMMENDED RESET CIRCUIT FOR INTERFACING WITH CPU/FPGA RESET OUTPUT



7.11 Reference Circuits for LED Strapping Pins

The Figure 7-13 shows the reference circuits for pull-up, float, and pull-down on the LED1 and LED0 strapping pins.

FIGURE 7-13: REFERENCE CIRCUITS FOR LED STRAPPING PINS



8.0 SELECTION OF ISOLATION TRANSFORMER

A 1:1 isolation transformer is required at the line interface. An isolation transformer with integrated common-mode chokes is recommended for exceeding FCC requirements.

Table 8-1 gives the recommended transformer characteristics.

TABLE 8-1: TRANSFORMER SELECTION CRITERIA

Parameter	Value	Test Condition
Turns Ratio	1 CT : 1 CT	—
Open-Circuit Inductance (minimum)	350 μH	100 mV, 100 kHz, 8 mA
Leakage Inductance (maximum)	0.4 μH	1 MHz (minimum)
Inter-Winding Capacitance (typical)	12 pF	—
DC Resistance (typical)	0.9Ω	—
Insertion Loss (maximum)	–1.0 dB	0 MHz – 65 MHz
HIPOT (minimum)	1500 V_{RMS}	—

TABLE 8-2: QUALIFIED SINGLE PORT MAGNETICS

Magnetic Manufacturer	Part Number	Auto MDI-X	Number of Ports
Bel Fuse	S558-5999-U7	Yes	1
Bel Fuse (Mag Jack)	SI-46001	Yes	1
Bel Fuse (Mag Jack)	SI-50170	Yes	1
Delta	LF8505	Yes	1
LanKom	LF-H41S	Yes	1
Pulse	H1102	Yes	1
Pulse (low cost)	H1260	Yes	1
Transpower	HB726	Yes	1
TDK (Mag Jack)	TLA-6T718	Yes	1

9.0 SELECTION OF REFERENCE CRYSTAL

TABLE 9-1: TYPICAL REFERENCE CRYSTAL CHARACTERISTICS

Characteristics	Value	Units
Frequency	25	MHz
Frequency Tolerance (maximum)	±50	ppm
Load Capacitance	20	pF
Series Resistance	40	Ω

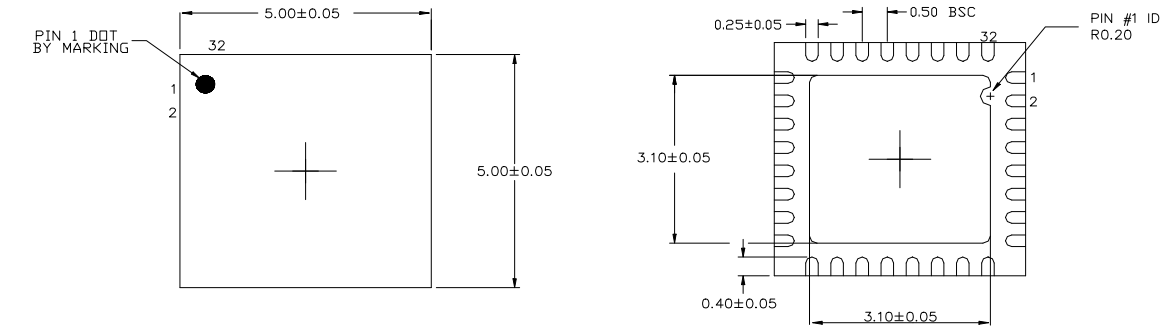
10.0 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

FIGURE 10-1: 32-LEAD QFN 5X5 PACKAGE

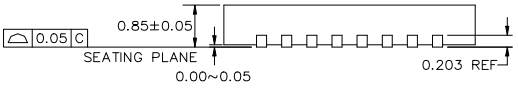
TITLE
32 LEAD QFN 5x5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	QFN55-32LD-PL-1	UNIT	MM

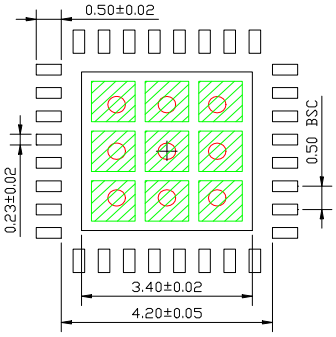


TOP VIEW
NOTE: 1, 2, 3

BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.87x0.87 MM IN SIZE, 1.07 MM PITCH.

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002245B (11-17-17)	Figure 10-1	Updated the 32-LEAD QFN 5X5 Package illustration.
	—	Minor text changes throughout.
DS00002245A (05-02-17)	ALL	KSZ8041NL/RNL Datasheet initial conversion to Microchip DS00002245A.

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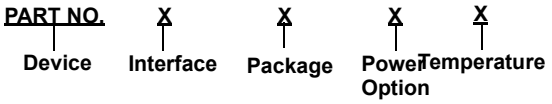

Device:	KSZ8041 – 10BASE-T/100BASE-TX Physical Layer Transceiver		
Interface:	Blank	=	MII/RMII
	R	=	RMII
Package:	N	=	32-pin QFN
Power Option:	L	=	Integrated LDO/LDO Controller/Regulator
Temperature:	Blank	=	Commercial (0°C to +70°C)
	I	=	Industrial (–40°C to +85°C)
	U	=	Automotive Grade 3 (–40°C to +85°C) (RMII Versions Only)
	AM	=	Automotive Grade 3 (–40°C to +85°C) (MII/RMII Version Only)

Examples:

a) KSZ8041NL – 10BASE-T/100BASE-TX Physical Layer Transceiver, MII/RMII, 32-pin QFN Commercial temperature

b) KSZ8041NLI – 10BASE-T/100BASE-TX Physical Layer Transceiver, MII/RMII, 32-pin QFN, Industrial Temperature

c) KSZ8041NL-AM – 10BASE-T/100BASE-TX Physical Layer Transceiver, MII/RMII, 32-pin QFN
Industrial temperature, Automotive Grade 3

d) KSZ8041RNLU – 10BASE-T/100BASE-TX Physical Layer Transceiver, RMII, 32-pin QFN Automotive Grade 3

e) KSZ8041RNL – 10BASE-T/100BASE-TX Physical Layer Transceiver, RMII, 32-pin QFN, Commercial temperature

f) KSZ8041RNLI – 10BASE-T/100BASE-TX Physical Layer Transceiver, RMII, 32-pin QFN, Industrial temperature

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