MSKSEMI 美森科













ESD

T\/

TSS

MOV

GDT

PLEC

BSS84-MS

Product specification





General Features

- -55 V,-0.3A, RDS(ON) =4.0Ω@VGS = 10V
- Improved dv/dt capability
- Fast switching
- Green Device Available
- ESD protected up to 2KV

Application

- Notebook
- Load Switch
- Battery Protection

Reference News

PACKAGE OUTLINE	Pin Configuration	Marking
SOT-363	Go	B84



Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
Vos	Drain-Source Voltage	-55	V
Vgs	Gate-Source Voltage	±20	V
l _D	Drain Current – Continuous (T _A =25°C)	-0.3	Α
	Drain Current – Continuous (T _A =70°C)	-0.2	А
Ірм	Drain Current – Pulsed ¹	-1.2	Α
Po	Power Dissipation (T _A =25°C)	1.0	W
ILD	Power Dissipation – Derate above 25°C	12.5	mW/°C
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Тур.	Max.	Unit
RθJA	Thermal Resistance Junction to ambient		80	°C/W

Electrical Characteristics (TJ=25 $^{\circ}$ C , unless otherwise noted)

Off Characteristics

Symbol	Parameter Conditions		Min.	Тур.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-55			V
lpss	Drain-Source Leakage Current	V _{DS} =-55V , V _{GS} =0V , T _J =25°C			- 1	uA
1055	Brain-Source Learlage Outrette	V _{DS} =-48V , V _{GS} =0V , T _J =125°C			- 10	uA
lgss	Gate-Source Leakage Current	Vgs= ±20V , Vps=0V			±20	uA

On Characteristics

RDS(ON)	Static Drain-Source On-Resistance	atic Drain-Source On-Resistance		4.0	5	Ω
Taba(ON) Static Di	Statio Brain Source on Hodistance	Vgs=-4.5V , Ip=-0.2A		3.5	6.0	
V _{GS(th)}	Gate Threshold Voltage	Vgs=Vps , Ip =-250uA	-1.0	- 1.7	-2.5	V
gfs	Forward Transconductance	V _{DS} =-10V , I _D =-0.3A		0.4		S



Dynamic and switching Characteristics

Qg	Total Gate Charge ^{2, 3}			2.8	
Qgs	Gate-Source Charge ^{2,3}	VDS=-30V , VGS=-10V , ID=-0.3A		0.96	 nC
Q_{gd}	Gate-Drain Charge ^{2,3}			0.6	
Td(on)	Turn-On Delay Time ^{2, 3}			3	
Tr	Rise Time ^{2,3}	V_{DD} =-30V , V_{GS} =-10V , R_G =6 Ω		5	
Td(off)	Turn-Off Delay Time ^{2,3}	In=-0.3A		14	 ns
Tf	Fall Time ^{2,3}			9	
Ciss	Input Capacitance			30.5	
Coss	Output Capacitance	V _{DS} =-30V , V _{GS} =0V , F=1MHz		15.1	 pF
Crss	Reverse Transfer Capacitance			7	

Drain-Source Diode Characteristics and Maximum Ratings

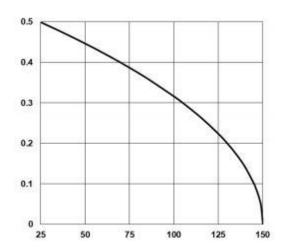
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
ls	Continuous Source Current	V _G =V _D =0V , Force Current			-0.3	Α
Isм	Pulsed Source Current	VG-VD-0V , Force Current			-0.6	Α
VsD	Diode Forward Voltage	Vgs=0V , Is=-0.2A , TJ=25°C			-1.2	V
Trr	Reverse Recovery Time	VR=-50V, IS=-0.3A		13.5		nS
Qrr	Reverse Recovery Charge	di/dt=100A/ps, TJ=25C		3		nC

Note:

- 1. Repetitive Rating: Pulsed width limited by maximum junction temperature.
- 2. The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%
- 3. Essentially independent of operating temperature.

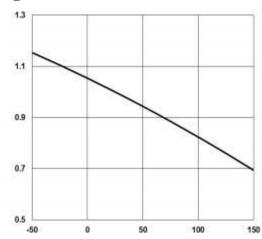
, Continuous Drain Current (A)

Normalized Gate Threshold Voltage



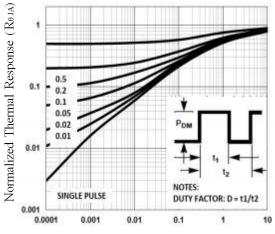
 T_J , Junction Temperature (°C)

Fig.1 Continuous Drain Current vs. Tc



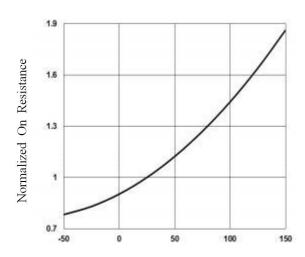
T_J , Junction Temperature (°C)

Fig.3 Normalized V_{th} vs. T_J



Square Wave Pulse Duration(s)

Fig. 5 Normalized Transient Impedance



T_J , Junction Temperature (°C)

Fig. 2 Normalized RDSON vs. TJ

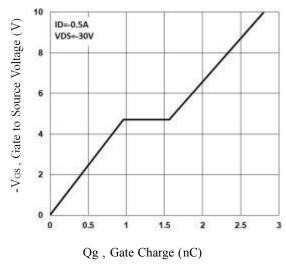
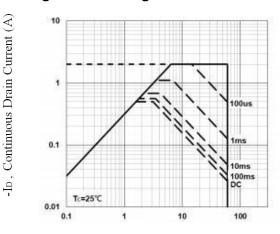
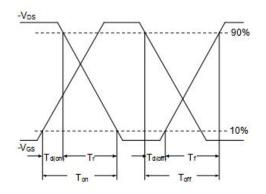


Fig.4 Gate Charge Waveform



-VDS,Drain to Source Voltage (V)

Fig.6 Maximum Safe Operation Area



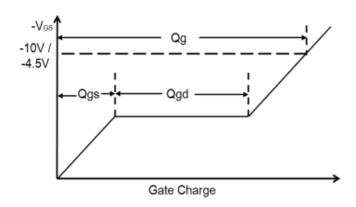


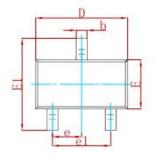
Fig. 7 Switching Time Waveform

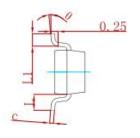
Fig. 8 Gate Charge Waveform

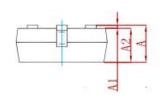




PACKAGE MECHANICAL DATA

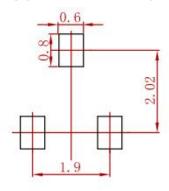






Cumbal	Dimensions In Millimeter		Dimension	s In Inches
Symbol	Min	Max	Min	Max
Α	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
С	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
е	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550	REF	0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Suggested Pad Layout



Note:

- 1.Controlling dimension:in millimeters.
- 2.General tolerance:± 0.05mm.
- 3. The pad layout is for reference purposes only.

REEL SPECIFICATION

P/N	PKG	QTY
BSS84-MS	SOT-23	3000



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