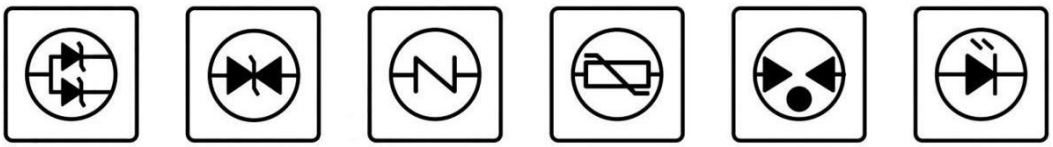
MSKSEMI 美森科
SEMICONDUCTOR



L293DN(MS)

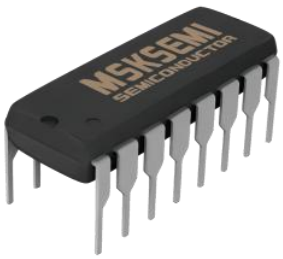
Product specification

DESCRIPTION

The Device is a monolithic integrated high volt-age, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power tran- sistors. To simplify use as two bridges each pair of chan-nels is equipped with an enable input. A separate supply input is provided for the logic, allowing op-eration at a lower voltage and internal clamp di-odes are included.
This device is suitable for use in switching appli-cations at frequencies up to 5 kHz.
The L293DN(MS) is assembled in a 16 lead plastic packaage which has 4 center pins connected to- gether and used for heatsinking.

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (non repeti- tive) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

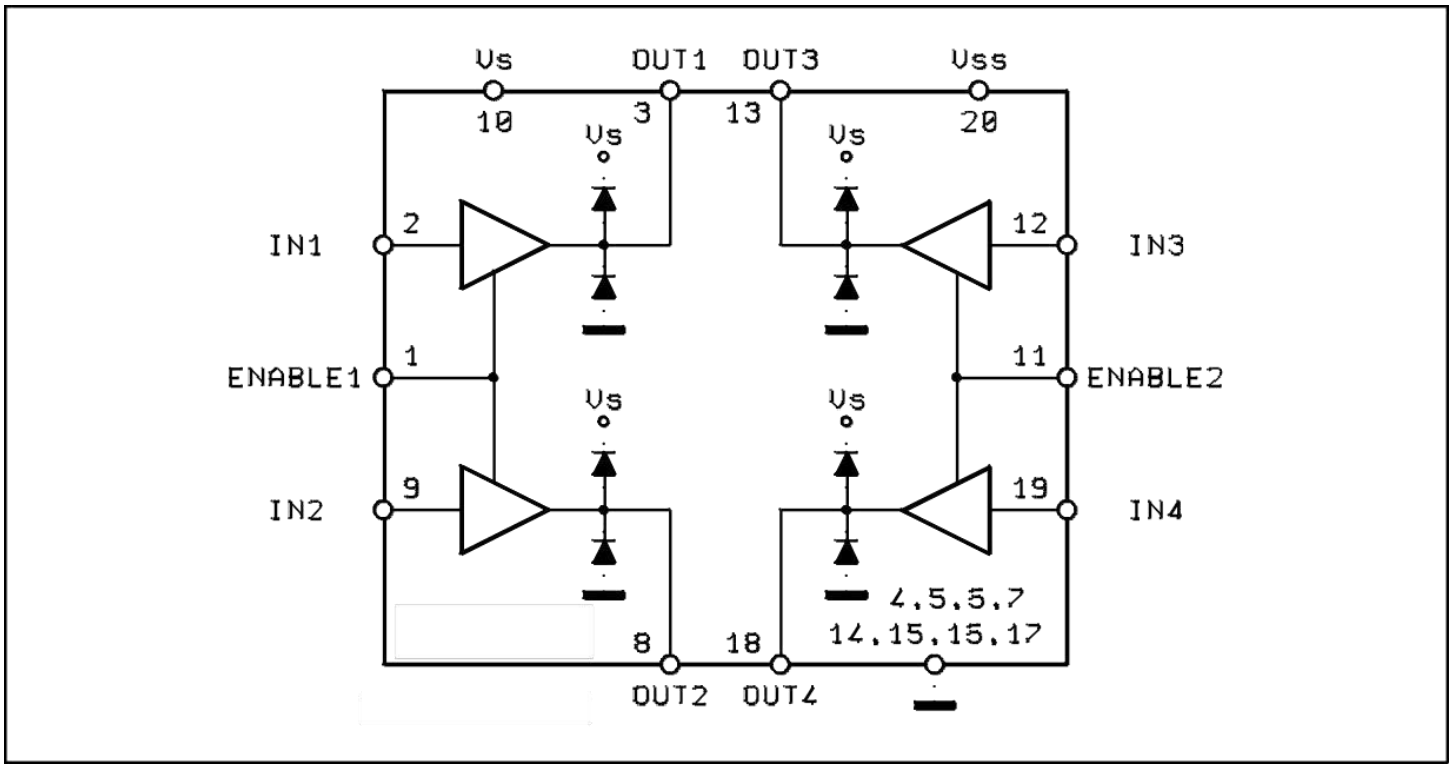
Reference News

PACKAGE OUTLINE	Marking
	
DIP-16	

ordering information

P/N	PKG	QTY
L293DN(MS)	DIP-16	25/One tube 1000/a box of

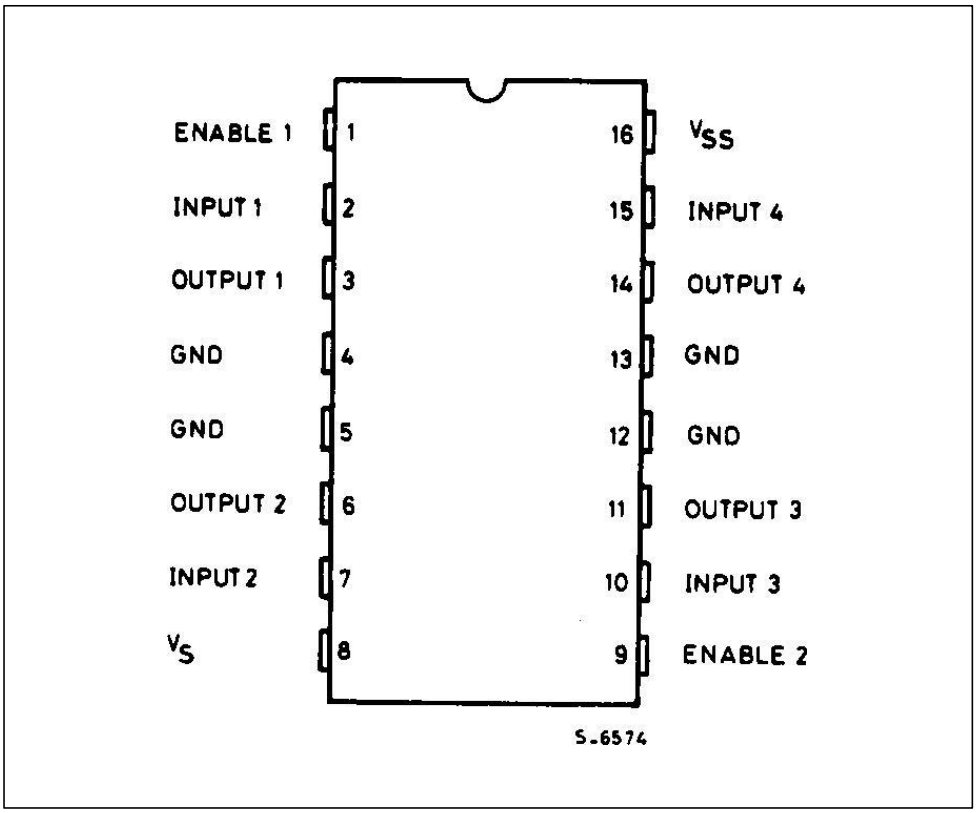
BLOCK DIAGRAM



ABSOLUTEMAXIMUMRATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	36	V
V_{SS}	Logic Supply Voltage	36	V
V_i	Input Voltage	7	V
V_{en}	Enable Voltage	7	V
I_o	Peak Output Current (100 µs non repetitive)	1.2	A
P_{tot}	Total Power Dissipation at T_{pins} = 90℃	4	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	℃

PIN CONNECTIONS (Top view)



THERMAL DATA

Symbol	Decription	DIP	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins max.	–	℃/W
$R_{th\ j\text{-}amb}$	Thermal Resistance junction-ambient max.	80	℃/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case max.	14	

(*) With 6sq. cm on board heatsink.

ELECTRICAL CHARACTERISTICS (for each channel, VS =24V, VSS =5 V, Tamb = 25℃, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Supply Voltage (pin 10)		V_{SS}		36	V
V_{SS}	Logic Supply Voltage (pin 20)		4.5		36	V
I_S	Total Quiescent Supply Current (pin 10)	V_i = L ; I_O = 0 ; V_{en} = H		2	6	mA
		V_i = H ; I_O = 0 ; V_{en} = H		16	24	mA
		V_{en} = L			4	mA
I_{SS}	Total Quiescent Logic Supply Current (pin 20)	V_i = L ; I_O = 0 ; V_{en} = H		44	60	mA
		V_i = H ; I_O = 0 ; V_{en} = H		16	22	mA
		V_{en} = L		16	24	mA
V_{IL}	Input Low Voltage (pin 2, 9, 12, 19)		– 0.3		1.5	V
V_{IH}	Input High Voltage (pin 2, 9, 12, 19)	V_{SS} < 7 V	2.3		V_{SS}	V
		V_{SS} > 7 V	2.3		7	V
I_{IL}	Low Voltage Input Current (pin 2, 9, 12, 19)	V_{IL} = 1.5 V			– 10	μA
I_{IH}	High Voltage Input Current (pin 2, 9, 12, 19)	2.3 V < V_{IH} < V_{SS} – 0.6 V		30	100	μA
$V_{en\ L}$	Enable Low Voltage (pin 1, 11)		– 0.3		1.5	V
$V_{en\ H}$	Enable High Voltage (pin 1, 11)	V_{SS} < 7 V	2.3		V_{SS}	V
		V_{SS} > 7 V	2.3		7	V
$I_{en\ L}$	Low Voltage Enable Current (pin 1, 11)	$V_{en\ L}$ = 1.5 V		– 30	– 100	μA
$I_{en\ H}$	High Voltage Enable Current (pin 1, 11)	2.3 V < $V_{en\ H}$ < V_{SS} – 0.6 V			± 10	μA
$V_{CE(sat)H}$	Source Output Saturation Voltage (pins 3, 8, 13, 18)	I_O = – 0.6 A		1.4	1.8	V
$V_{CE(sat)L}$	Sink Output Saturation Voltage (pins 3, 8, 13, 18)	I_O = + 0.6 A		1.2	1.8	V
V_F	Clamp Diode Forward Voltage	I_O = 600nA		1.3		V
t_r	Rise Time (*)	0.1 to 0.9 V_O		250		ns
t_f	Fall Time (*)	0.9 to 0.1 V_O		250		ns
t_{on}	Turn-on Delay (*)	0.5 V_i to 0.5 V_O		750		ns
t_{off}	Turn-off Delay (*)	0.5 V_i to 0.5 V_O		200		ns

(*) See fig. 1.

TRUTH TABLE (one channel)

Input	Enable (*)	Output
H	H	H
L	H	L
H	L	Z
L	L	Z

Z = High output impedance
(*) Relative to the considered channel

Figure 1: Switching Times

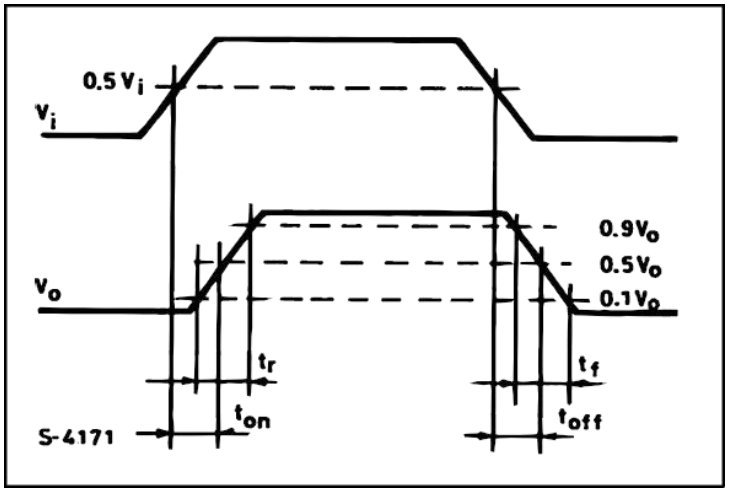
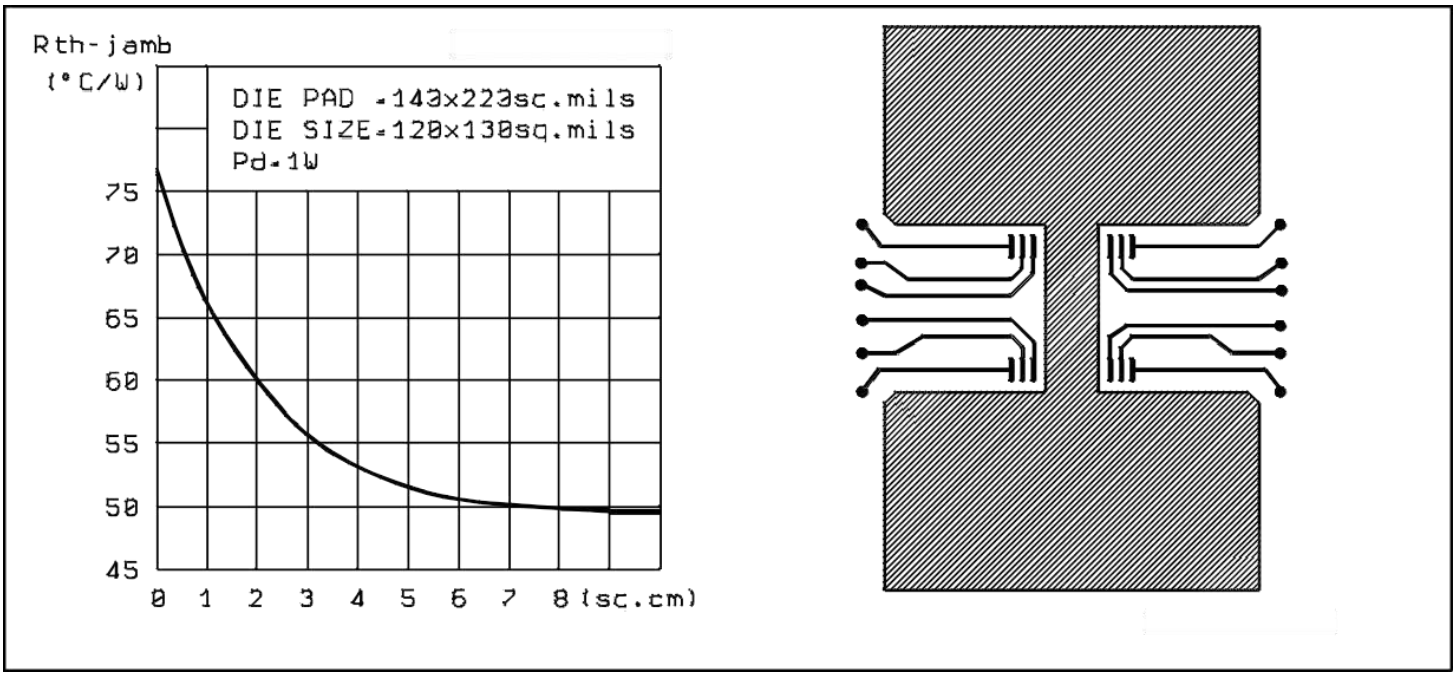
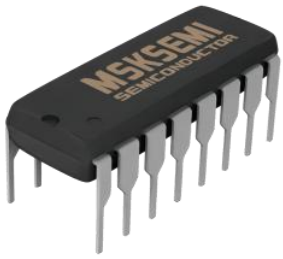


Figure 2: Junction to ambient thermal resistance vs. area on board heatsink (SO12+4+4 package)

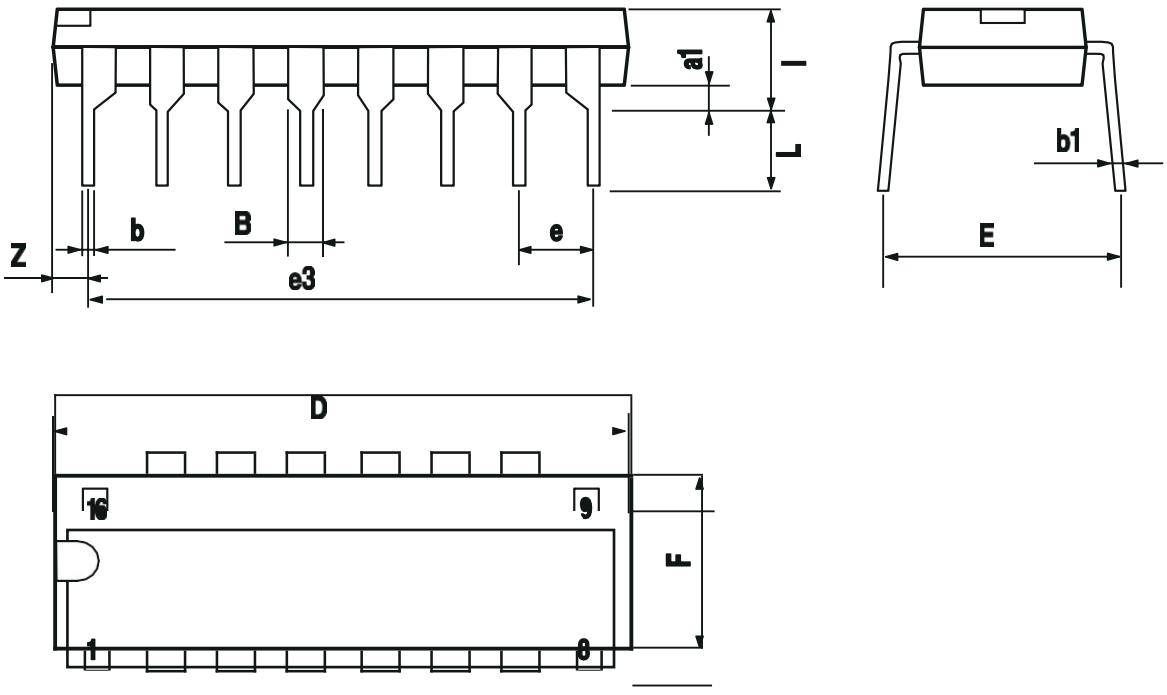


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

OUTLINE AND MECHANICAL DATA



DIP-16



Attention

■ Any and all MSKSEMI Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your MSKSEMI Semiconductor representative nearest you before using any MSKSEMI Semiconductor products described or contained herein in such applications.

■ MSKSEMI Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specificationsof any andall MSKSEMI Semiconductor products described orcontained herein.

■ Specifications of any and all MSKSEMI Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer'sproducts orequipment.

■ MSKSEMI Semiconductor. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with someprobability. It is possiblethat these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits anderror prevention circuitsfor safedesign, redundant design, and structural design.

■ In the event that any or all MSKSEMI Semiconductor products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from theauthorities concerned in accordance with the above law.

■ No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of MSKSEMI Semiconductor.

■ Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. MSKSEMI Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringementsof intellectual property rights or other rightsof third parties.

■ Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. Whendesigning equipment, referto the "Delivery Specification" for the MSKSEMI Semiconductor productthat you intend to use.

单击下面可查看定价，库存，交付和生命周期等信息

>>MSKSEMI(美森科)