# MSKSEMI 美森科













ESD

TVS

TSS

MOV

GDT

PLED

L293DNE(MS)

**Product specification** 





#### DESCRIPTION

The Device is a monolithic integrated high volt-age, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoides, DC and stepping motors) and switching power tran- sistors. To simplify use as two bridges each pair of chan-nels is equipped with an enable input. A separate supply input is provided for the logic, allowing op-eration at a lower voltage and internal clamp di-odes are included.

This device is suitable for use in switching appli-cations at frequencies up to 5 kHz.

The L293DNE(MS) is assembled in a 16 lead plastic packaage which has 4 center pins connected to- gether and used for heatsinking.

- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (non repeti- tive) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

#### **Reference News**

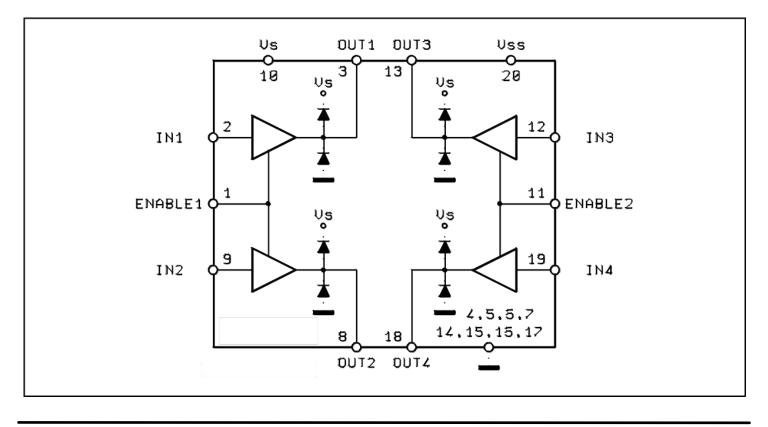
PACKAGE OUTLINE	Marking	
Section of the sectio	MSKSEMI L293D MS****	
DIP-16		

#### ordering information

P/N	PKG	QTY
L293DNE(MS)	DIP-16	25/One tube 1000/a box of



## **BLOCK DIAGRAM**

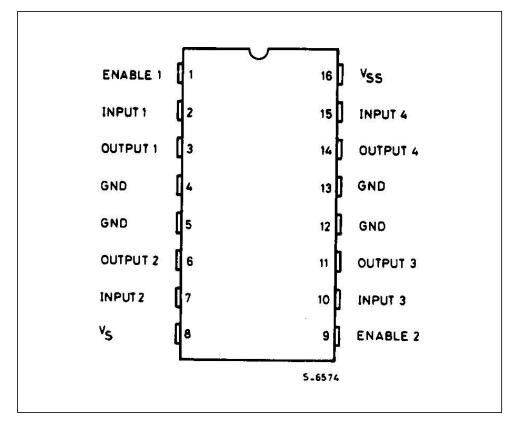


## ABSOLUTEMAXIMUMRATINGS

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	36	V
Vss	Logic Supply Voltage	36	V
Vi	Input Voltage	7	V
Ven	Enable Voltage	7	V
lo	Peak Output Current (100 µs non repetitive)	1.2	А
Ptot	Total Power Dissipation at T <sub>pins</sub> = 90 ℃	4	W
Tstg,Tj	Storage and Junction Temperature	– 40 to 150	°C



# PIN CONNECTIONS (Top view)



## THERMAL DATA

Symbol	Decription	DIP	Unit
Rth j-pins	Thermal Resistance Junction-pins max.	_	°C <b>/W</b>
Rth j-amb	Thermal Resistance junction-ambient max.	80	°C/W
Rth j-case	Thermal Resistance Junction-case max.	14	

(\*) With 6sq. cm on board heatsink.



# **ELECTRICAL CHARACTERISTICS** (for each channel, VS =24V, VSS =5 V, Tamb = 25°C, unless

### otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Vs	Supply Voltage (pin 10)		Vss		36	V
Vss	Logic Supply Voltage (pin 20)		4.5		36	V
	T LLO : LO LO L	$V_i = L$ ; $I_0 = 0$ ; $V_{en} = H$		2	6	mA
ls	Total Quiescent Supply Current (pin 10)	$V_i = H ; I_0 = 0 ; V_{en} = H$		16	24	mA
		V <sub>en</sub> = L			4	mA
		$V_i = L$ ; $I_0 = 0$ ; $V_{en} = H$		44	60	mA
Iss	Total Quiescent Logic Supply Current (pin 20)	$V_i = H ; I_0 = 0 ; V_{en} = H$		16	22	mA
		V <sub>en</sub> = L		16	24	mA
VIL	Input Low Voltage (pin 2, 9, 12, 19)		- 0.3		1.5	V
	Input High Voltage (pin 2, 9,	V <sub>SS</sub> < 7 V	2.3		V <sub>SS</sub>	V
VIH	12, 19)	V <sub>SS</sub> > 7 V	2.3		7	V
I <sub>IL</sub>	Low Voltage Input Current (pin 2, 9, 12, 19)	V <sub>IL</sub> = 1.5 V			- 10	μA
Іін	High Voltage Input Current (pin 2, 9, 12, 19)	2.3 V < V <sub>IH</sub> < V <sub>SS</sub> – 0.6 V		30	100	μA
Ven L	Enable Low Voltage (pin 1, 11)		- 0.3		1.5	V
	Enable High Voltage	V <sub>SS</sub> < 7 V	2.3		Vss	V
Ven H	(pin 1, 11)	V <sub>SS</sub> > 7 V	2.3		7	V
len L	Low Voltage Enable Current (pin 1, 11)	V <sub>en L</sub> = 1.5 V		- 30	- 100	μA
I <sub>en H</sub>	High Voltage Enable Current (pin 1, 11)	$2.3 V < V_{en H} < V_{SS} - 0.6 V$			± 10	μΑ
VCE(sat)H	Source Output Saturation Voltage (pins 3, 8, 13, 18)	lo = - 0.6 A		1.4	1.8	V
V <sub>CE(sat)</sub> L	Sink Output Saturation Voltage (pins 3, 8, 13, 18)	I <sub>0</sub> = + 0.6 A		1.2	1.8	V
VF	Clamp Diode Forward Voltage	I <sub>0</sub> = 600nA		1.3		V
tr	Rise Time (*)	0.1 to 0.9 V <sub>o</sub>		250		ns
t <sub>f</sub>	Fall Time (*)	0.9 to 0.1 V <sub>O</sub>		250		ns
ton	Turn-on Delay (*)	0.5 V <sub>i</sub> to 0.5 V <sub>o</sub>		750		ns
toff	Turn-off Delay (*)	0.5 V <sub>i</sub> to 0.5 V <sub>o</sub>		200		ns

(\*) See fig. 1.

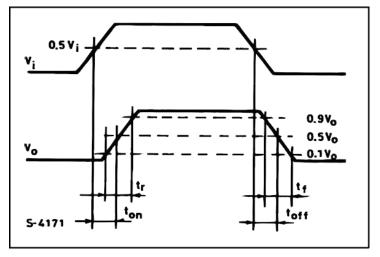


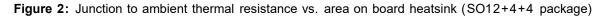
# TRUTH TABLE (one channel)

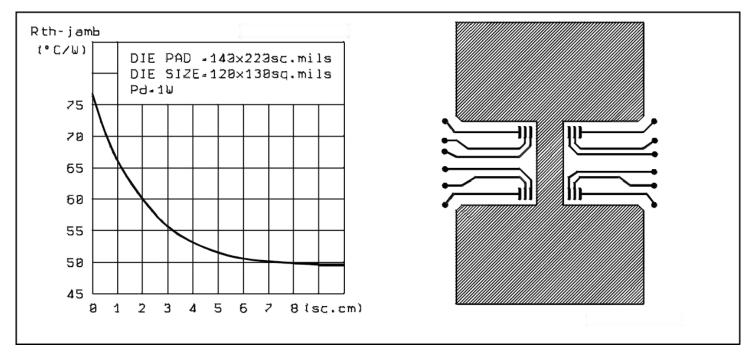
Input	Enable (*)	Output
Н	Н	Н
L	Н	L
H	L	Z
L	L	Z

Z = High output impedance (\*) Relative to the considered channel

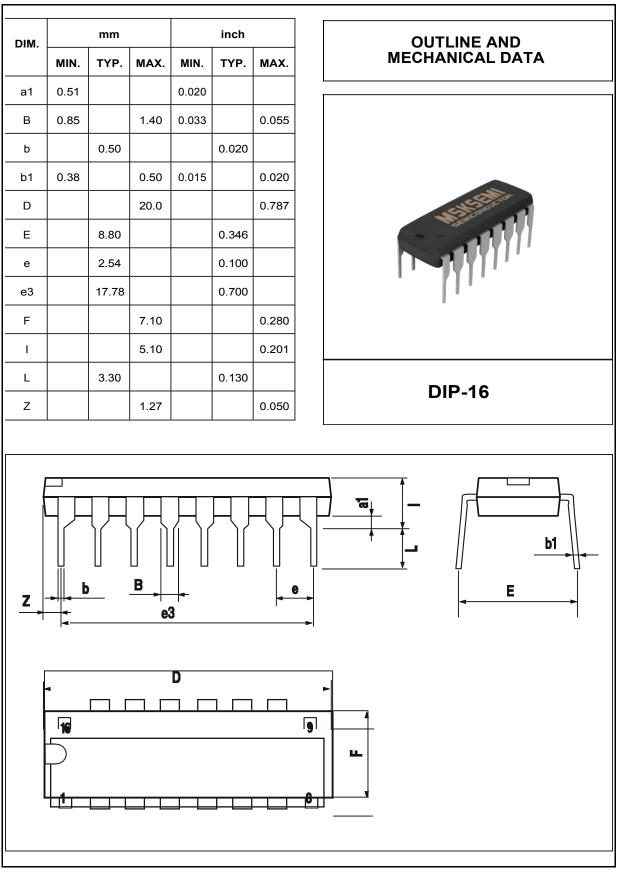
Figure 1: Switching Times











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