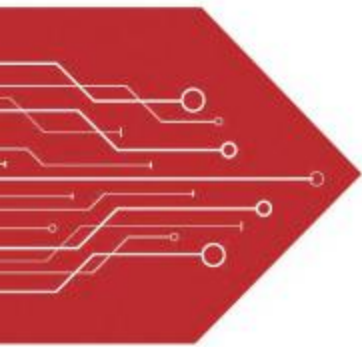


# MSKSEMI

SEMICONDUCTOR



ESD



TVS



TSS



MOV



GDT



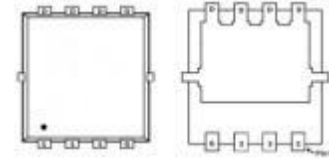
PLED

Product data sheet

[www.msksemi.com](http://www.msksemi.com)

## Description

The MSK50P03NF uses advanced trench technology excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.



## General Features

$V_{DS} = -30V, I_D = -50A$

$R_{DS(ON)} < 18m\Omega @ V_{GS} = -4.5V$

$R_{DS(ON)} < 13m\Omega @ V_{GS} = -10V$

High Power and current handling capability

Lead free product is acquired

Surface mount package

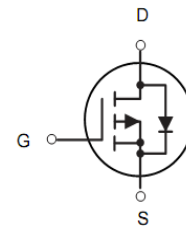
## Application

PWM applications

Load switch

Power management

DFN5X6-8L



P-Channel MOSFET

### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-30	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous ( $T_C = 25^\circ C$ )	I <sub>D</sub>	-50	A
Drain Current-Continuous ( $T_C = 100^\circ C$ )		-24	
Drain Current-Pulsed (Note 1)	I <sub>DM</sub>	-80	A
Maximum Power Dissipation ( $T_C = 25^\circ C$ )	P <sub>D</sub>	3	W
Maximum Power Dissipation ( $T_C = 100^\circ C$ )		1.3	
Single pulse avalanche energy (Note 5)	E <sub>AS</sub>	231	mJ
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 To 150	°C
Thermal Resistance, Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	41.67	°C/W

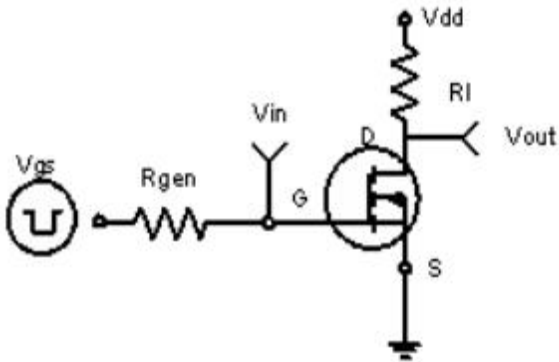
**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	-	-	-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.5	-3	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-10A	-	11.5	15	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-7A	-	18	25	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-10A	-	20	-	S
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, F=1.0MHz	-	1750	-	PF
Output Capacitance	C <sub>oss</sub>		-	215	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	180	-	PF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-15V, I <sub>D</sub> =-10A, V <sub>GS</sub> =-10V, R <sub>GEN</sub> =1Ω	-	9	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	8	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	28	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	10	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-15V, I <sub>D</sub> =-10A, V <sub>GS</sub> =-10V	-	24	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.5	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	6	-	nC
Diode Forward Current <sup>(Note 2)</sup>	I <sub>s</sub>		-	-	-12	A
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>s</sub> =-12A	-	-	-1.2	V

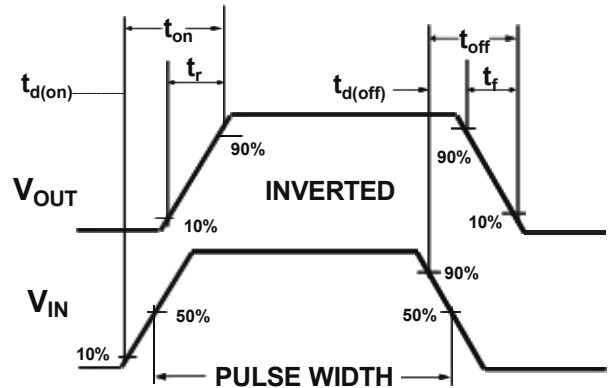
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E<sub>AS</sub> condition: T<sub>j</sub>=25°C, V<sub>DD</sub>=-15V, V<sub>G</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω, I<sub>AS</sub>=-34A

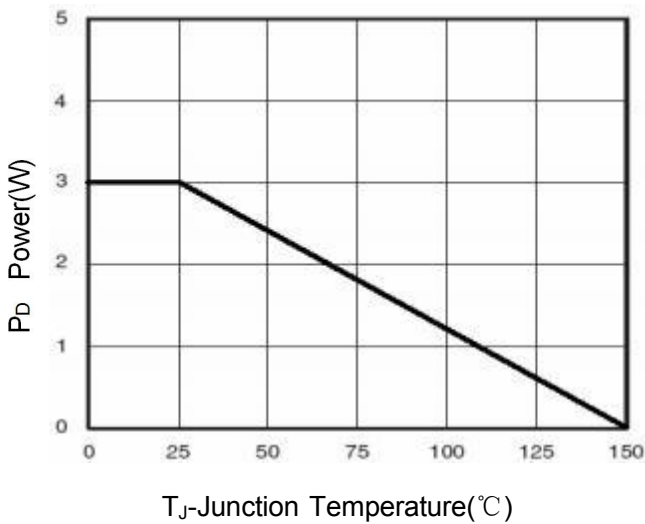
**Typical Electrical and Thermal Characteristics**



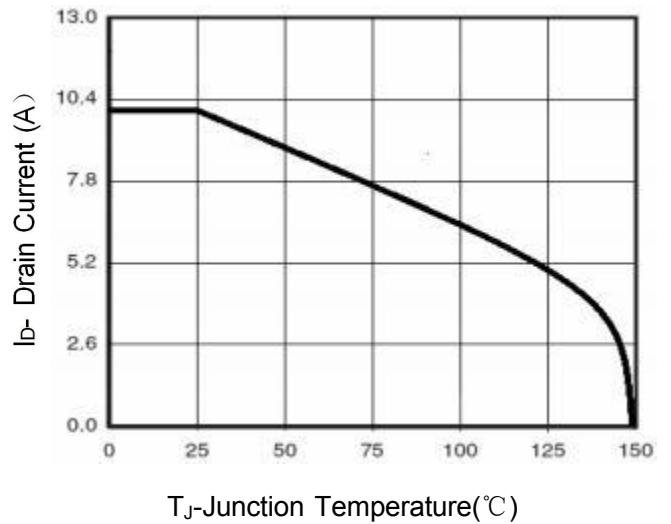
**Figure 1: Switching Test Circuit**



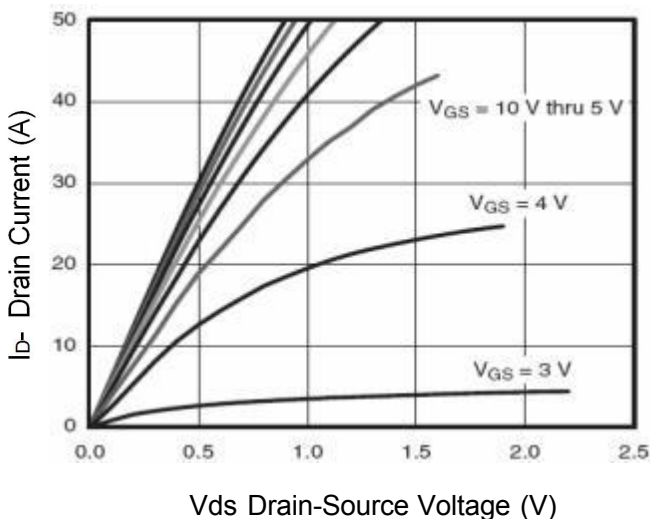
**Figure 2: Switching Waveforms**



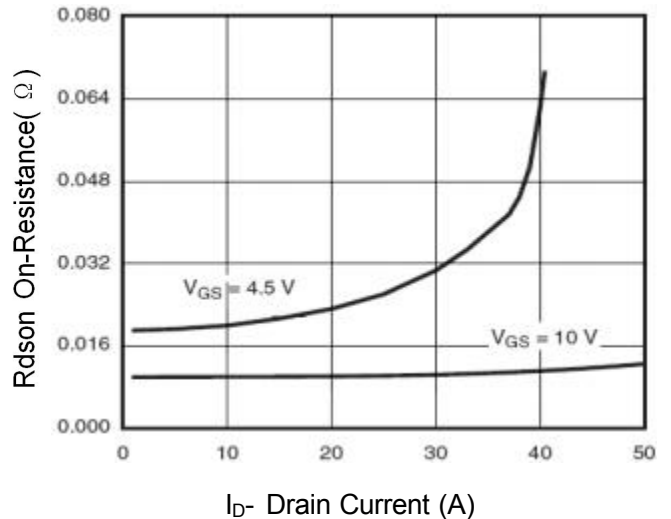
**Figure 3 Power Dissipation**



**Figure 4 Drain Current**

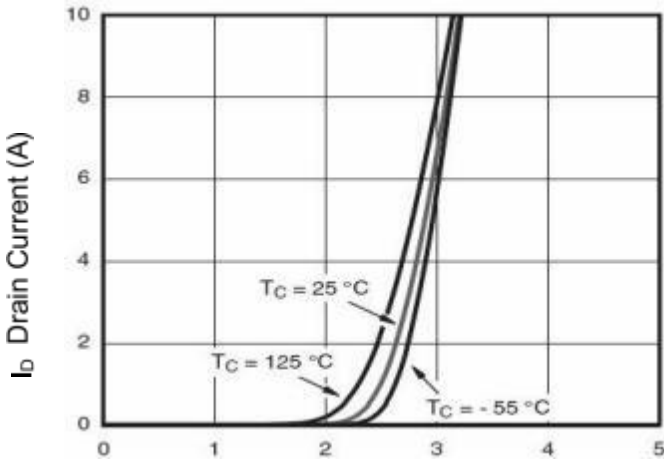


**Figure 5 Output Characteristics**



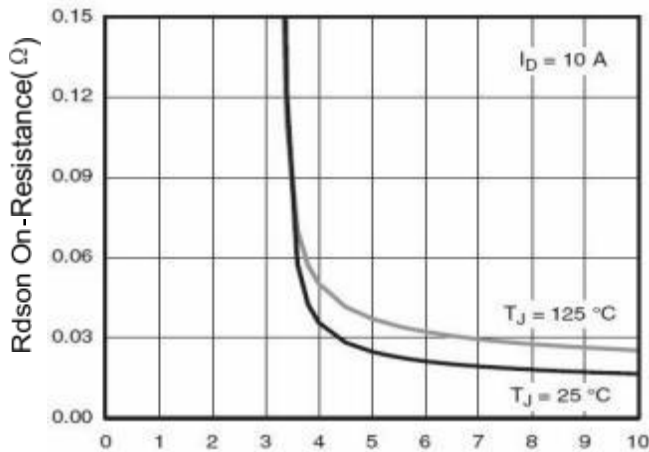
**Figure 6 Drain-Source On-Resistance**

**Figure 5 Output Characteristics**



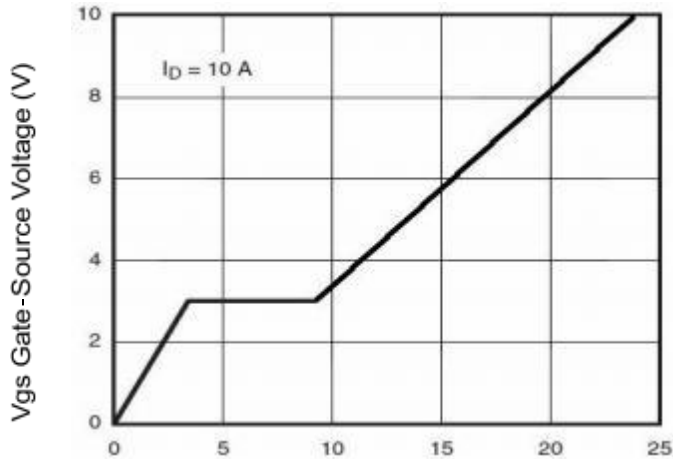
$V_{GS}$  Gate-Source Voltage (V)

**Figure 7 Transfer Characteristics**



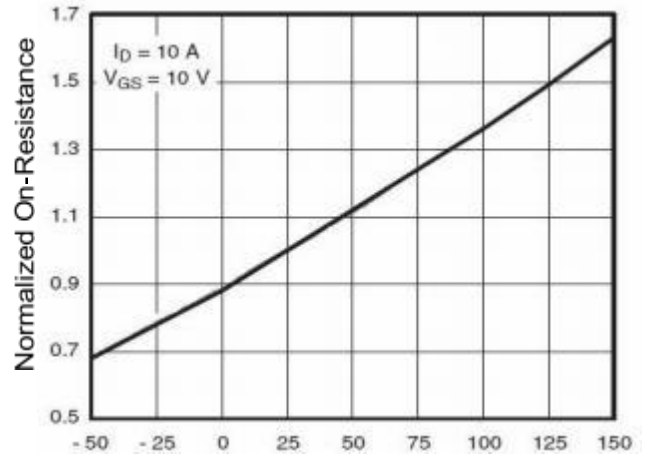
$V_{GS}$  Gate-Source Voltage (V)

**Figure 9 Rdson vs Vgs**



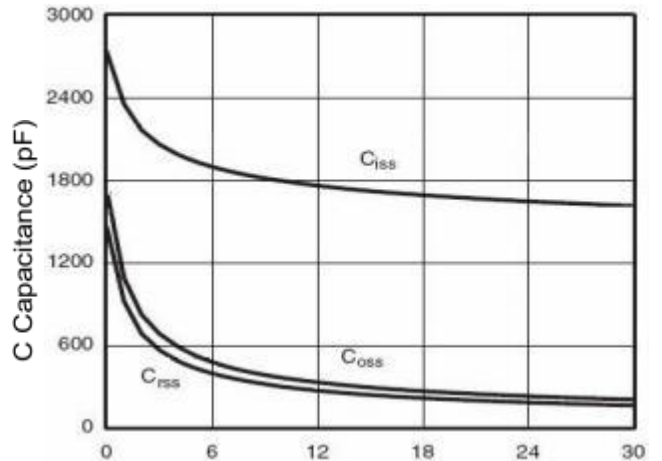
$Q_G$  Gate Charge (nC)

**Figure 11 Gate Charge**



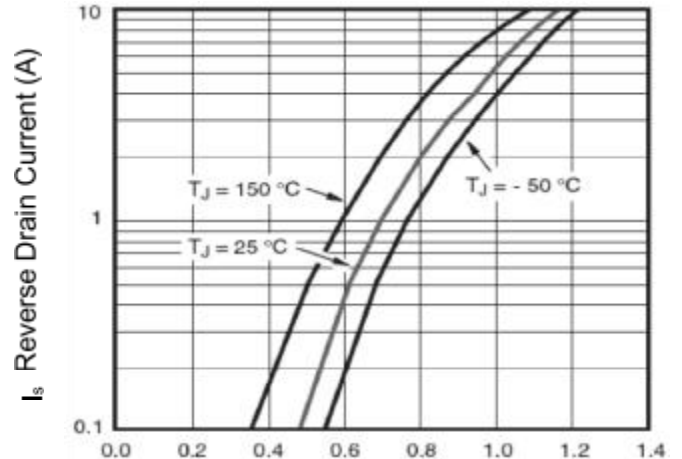
$T_J$ -Junction Temperature ( $^\circ\text{C}$ )

**Figure 8 Drain-Source On-Resistance**



$V_{DS}$  Drain-Source Voltage (V)

**Figure 10 Capacitance vs Vds**



$V_{SD}$  Source-Drain Voltage (V)

**Figure 12 Source- Drain Diode Forward**

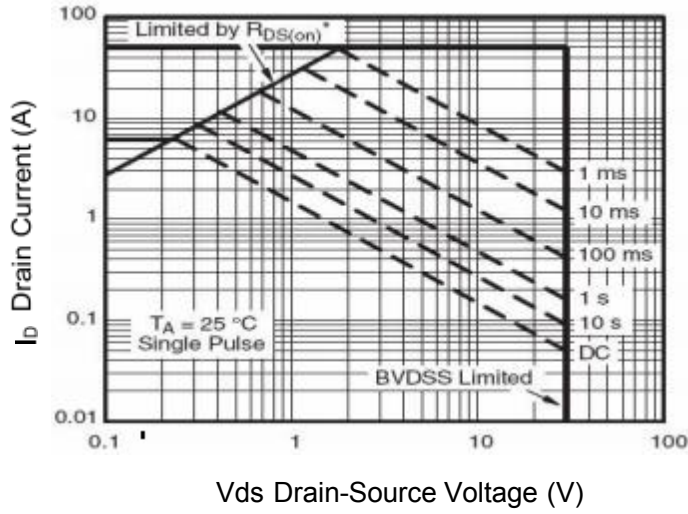


Figure 13 Safe Operation Area

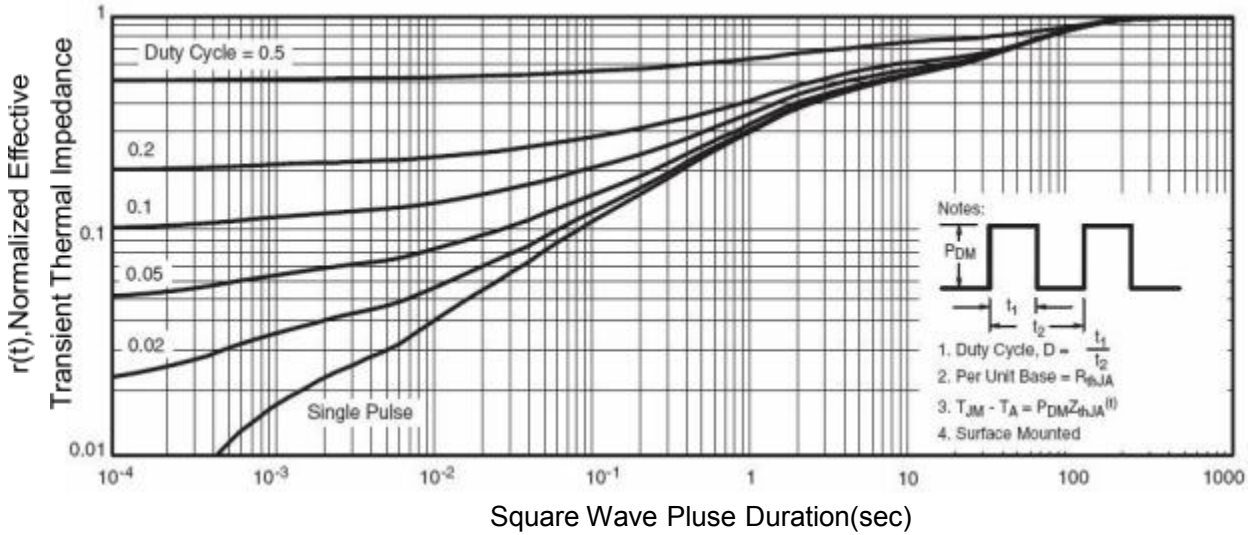
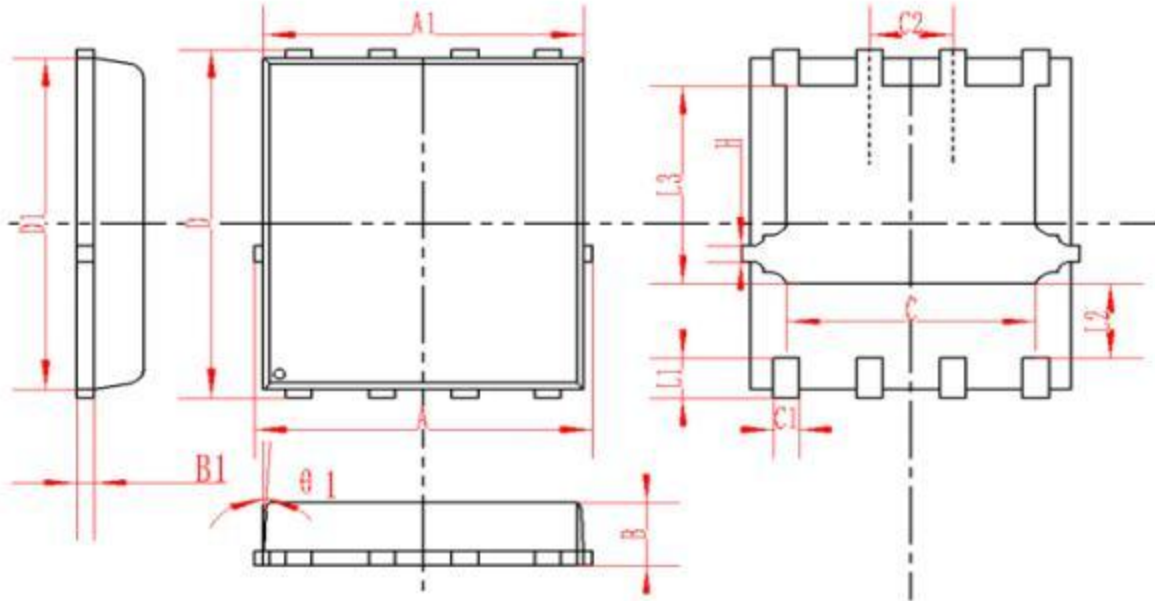


Figure 14 Normalized Maximum Transient Thermal Impedance

**DFN5X6-8L Package Information**



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
theta 1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010

**REEL SPECIFICATION**

P/N	PKG	QTY
MSK50P03NF	DFN5X6-8L	5000

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