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SEMICONDUCTOR



ESD



TVS



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PLED

ULN2001D(MS)

Product specification

GENERAL DESCRIPTION

The ULN2001D(MS) is high-voltage high-current Darlington transistor arrays each containing seven open collector common emitter pairs.

Each pair is rated at 500mA. Suppression diodes are included for inductive load driving, the inputs and outputs are pinned in opposition to simplify board layout.

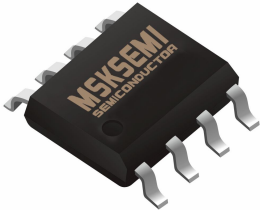
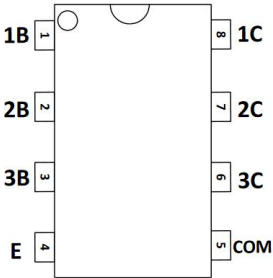
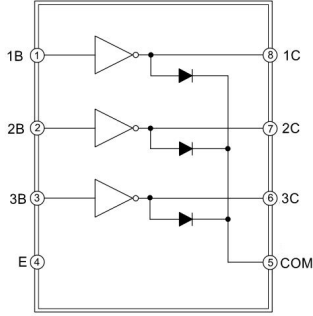

These devices are capable of driving a wide range of loads including solenoids, relays, DC motors, LED displays, filament lamps, thermal print-heads and high-power buffers.

The ULN2001D(MS) is available in both a small outline 8-pin package (SOP8).

FEATURES

- 500-mA-Rated Collector Current(single output)
- High-Voltage Outputs:50V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

Pin Configuration and Functions

PACKAGE OUTLINE	Pin Assignments	ConnectionDiagram	Marking
 <p>SOP-8</p>			 <p>Note: *****=batch</p>

Pin Descriptions

Pin Number	Pin Name	Function
1	1B	Input pair1
2	2B	Input pair2
3	3B	Input pair3
4	E	Common Emitter (ground)
5	COM	Common Clamp Diodes
6	3C	Output pair3
7	2C	Output pair2
8	1C	Output pair1

Electrical Characteristics(TA=+25°C, unless otherwise specified)

Parameter		Test Figure	Test Conditions		TX2001D			Unit
					MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	Figure 6	VCE = 2 V	IC = 200 mA	--	--	2.4	V
				IC = 250 mA	--	--	2.7	
				IC = 300 mA	--	--	3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	Figure 5	II = 250 μ A,	IC = 100 mA	--	0.9	1.1	V
			II = 350 μ A,	IC = 200 mA	--	1	1.3	
			II = 500 μ A,	IC = 350 mA	--	1.2	1.6	
I_{CEX}	Collector cutoff current	Figure 1	VCE = 50 V,	II = 0	--	--	50	μ A
		Figure 2	VCE = 50 V, TA = +105°C	II = 0	--	--	100	
V_F	Clamp forward voltage	Figure 8	IF = 350 mA		--	1.7	2	V
$I_{I(off)}$	Off-state input current	Figure 3	VCE = 50 V, IC = 500 μ A		50	65	--	μ A
II	Input current	Figure 4	VI = 3.85 V		--	0.93	1.35	mA
IR	Clamp reverse current	Figure 7	VR = 50 V	TA = 25°C	--	--	50	μ A
				TA = 70°C	--	--	100	
Ci	Input capacitance		VI = 0, f = 1 MHz		--	15	25	pF

Switching Characteristics (TA = +25°C, unless otherwise specified)

Parameter		Test Conditions	TX2001D			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low- to high-level output	See Figure 9	--	0.25	1	μ s
t_{PHL}	Propagation delay time, high- to low-level output	See Figure 9	--	0.25	1	μ s
V_{OH}	High-level output voltage after switching	VS = 50 V, IO = 300 mA, See Figure 9	VS-20	--	--	mV

Parameter Measurement Information

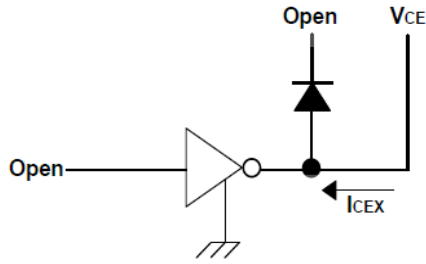


Fig.1 I_{CEX} Test Circuit

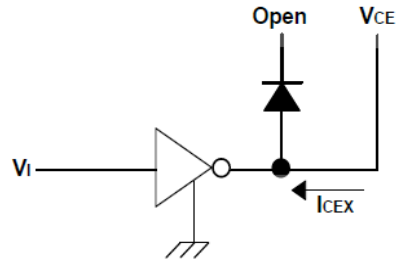


Fig.2 I_{CEX} Test Circuit

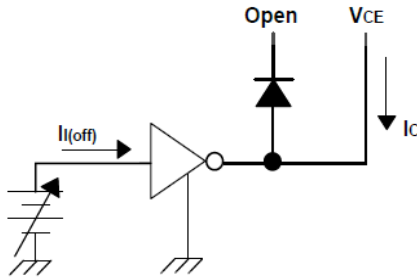


Fig.3 I_{I(off)} Test Circuit

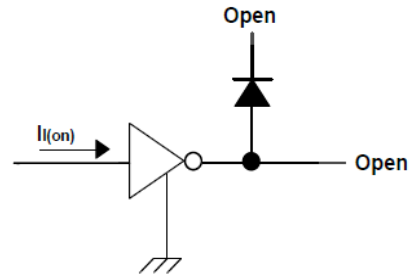


Fig.4 I_I Test Circuit

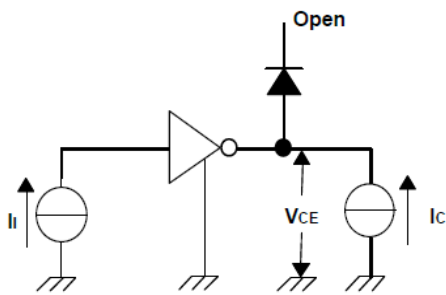


Fig. 5 h_{FE} , V_{CE(sat)} Test Circuit

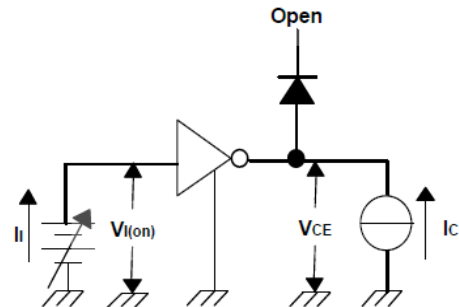


Fig. 6 V_{I(on)} Test Circuit

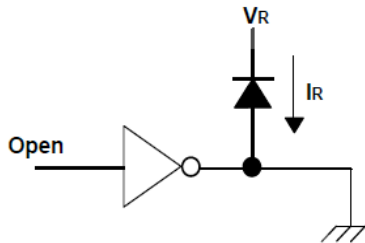


Fig. 7 I_R Test Circuit

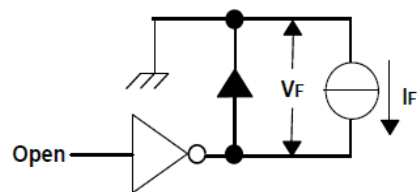


Fig. 8 V_F Test Circuit

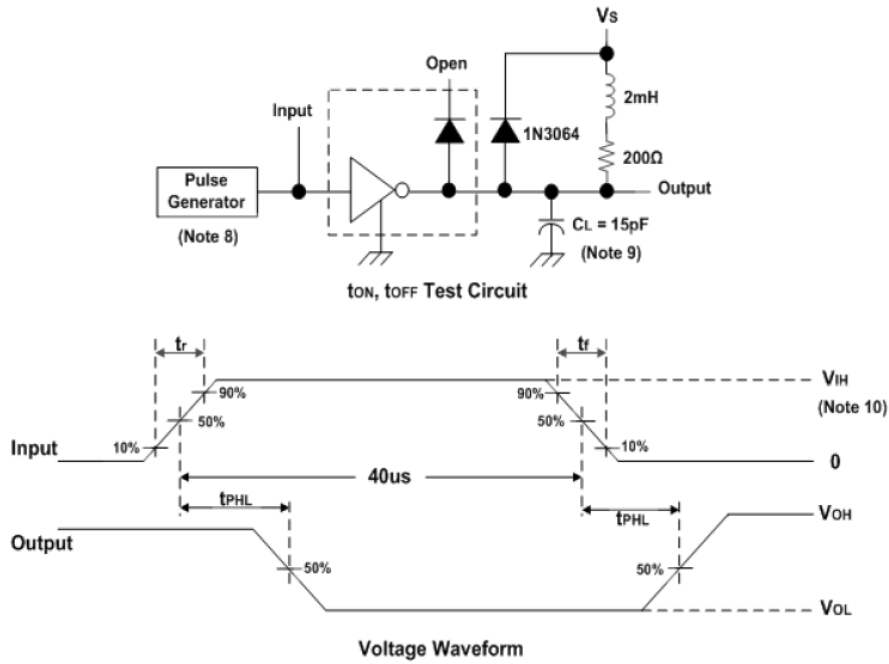


Fig. 9 Latch-Up Test Circuit and Voltage Waveform

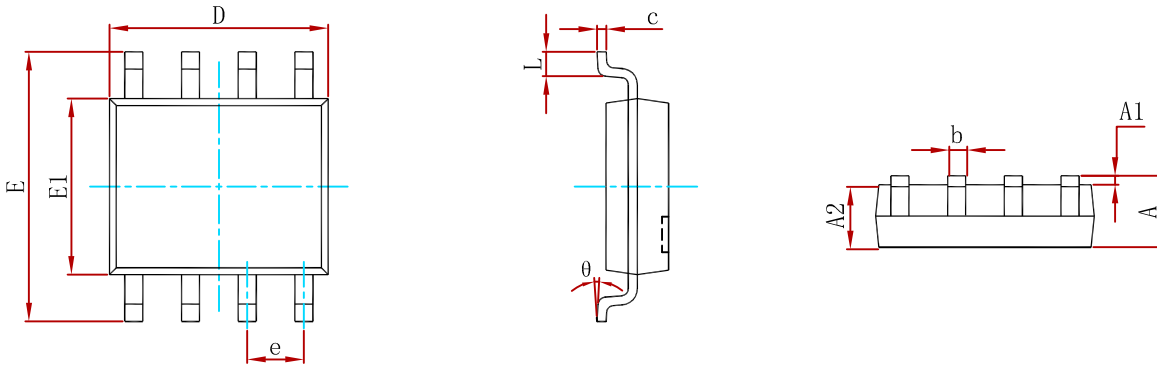
Notes: 8. The pulse generator has the following characteristics:

Pulse Width=12.5Hz, output impedance 50Ω, $t_r \leq 5\text{ns}$, $t_f \leq 10\text{ns}$.

9. C_L includes probe and jig capacitance.

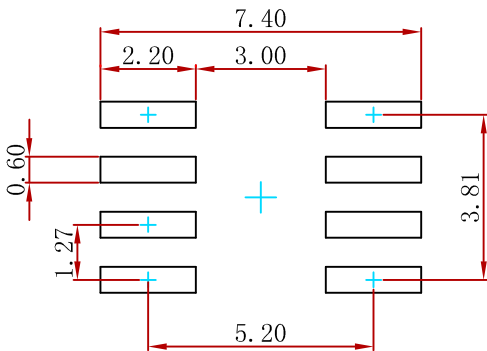
10. $V_{IH} = 3\text{V}$

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

Suggested Pad Layout



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.05\text{mm}$.
 3. The pad layout is for reference purposes only.

REEL SPECIFICATION

P/N	PKG	QTY
ULN2001D(MS)	SOP-8	3500

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