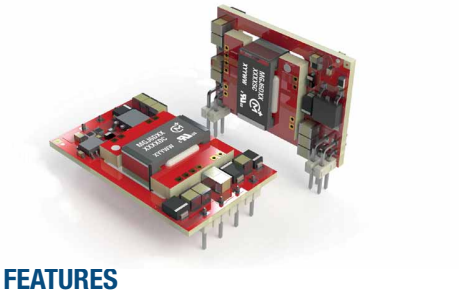
Murata Power Solutions

MGJ6 SIP/DIP Series

5.7kVDC Isolated 6W Gate Drive SIP/DIP DC-DC Converters



FEATURES

- Patent protected
- No opto feedback
- Optimised bipolar output voltages for IGBT/ SiC & MOSFET gate drives
- Configurable dual outputs for all gate drive applications: +15V/-5V, +15V/-10V & +20V/-5V outputs
- Reinforced insulation to UL60950 recognised
- ANSI/AAMI ES60601-1, 2MOPP recognised
- Characterised CMTI >100kV/µS
- Characterised partial discharge performance
- 5.7kVDC isolation test voltage 'Hi Pot Test'
- Ultra low isolation capacitance 15pF
- Continuous barrier withstand voltage 3kVDC
- 5V, 12V & 24V input voltages
- 105°C operating temperature

PRODUCT OVERVIEW

Offering configurable dual output voltages of +15V/-10V, +20V/-5V and +15V/-5V, the MGJ6 series of DC-DC converters is ideal for powering 'high side' and 'low side' gate drive circuits for IGBTs, Silicon Carbide and MOSFETs in bridge circuits.
A choice of asymmetric output voltages allows optimum drive levels for best system efficiency and EMI. The MGJ6 series is characterised for high isolation and dv/dt requirements commonly seen in bridge circuits used in motor drives and inverters.
A disable/frequency synchronisation pin simplifies EMC filter design. The MGJ6 protection features include short circuit protection and overload protection.

RoHS COMPLIANT

25

For full details go to www.murata-ps.com/rohs

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SELECTION GUIDE

Order Code[1]	Input Voltage Range	Typical Application	Output 1			Output 2			Package style
			Rated Output Voltage	Rated Output Current	Output Power	Rated Output Voltage	Rated Output Current	Output Power	
	V	See page 9	V	mA	W	V	mA	W	
MGJ6D051510DC	4.5 - 9	IGBT	+15	240	3.6	-10	240	2.4	DIP
MGJ6D121510DC	9 - 18	IGBT	+15	240	3.6	-10	240	2.4	
MGJ6D241510DC	18 - 36	IGBT	+15	240	3.6	-10	240	2.4	
MGJ6D052005DC	4.5 - 9	SiC	+20	240	4.8	-5	240	1.2	
MGJ6D122005DC	9 - 18	SiC	+20	240	4.8	-5	240	1.2	
MGJ6D242005DC	18 - 36	SiC	+20	240	4.8	-5	240	1.2	
MGJ6D051505DC	4.5 - 9	MOSFET	+15	300	4.5	-5	300	1.5	
MGJ6D121505DC	9 - 18	MOSFET	+15	300	4.5	-5	300	1.5	
MGJ6D241505DC	18 - 36	MOSFET	+15	300	4.5	-5	300	1.5	
MGJ6D051510SC	4.5 - 9	IGBT	+15	240	3.6	-10	240	2.4	SIP
MGJ6D121510SC	9 - 18	IGBT	+15	240	3.6	-10	240	2.4	
MGJ6D241510SC	18 - 36	IGBT	+15	240	3.6	-10	240	2.4	
MGJ6D052005SC	4.5 - 9	SiC	+20	240	4.8	-5	240	1.2	
MGJ6D122005SC	9 - 18	SiC	+20	240	4.8	-5	240	1.2	
MGJ6D242005SC	18 - 36	SiC	+20	240	4.8	-5	240	1.2	
MGJ6D051505SC	4.5 - 9	MOSFET	+15	300	4.5	-5	300	1.5	
MGJ6D121505SC	9 - 18	MOSFET	+15	300	4.5	-5	300	1.5	
MGJ6D241505SC	18 - 36	MOSFET	+15	300	4.5	-5	300	1.5	

1. Components are supplied in tray packaging, please refer to package specification section for more details.
All specifications typical at T_A=25°C, nominal input voltage and rated output current unless otherwise specified.

SELECTION GUIDE (Continued)

Order Code[1]	Input Voltage Range	Typical Application	Output 1				Output 2			
			Load Regulation (Typ)[3]	Load Regulation (Max)[3]	Ripple & Noise (Typ)[2]	Ripple & Noise (Max)[2]	Load Regulation (Typ)	Load Regulation (Max)	Ripple & Noise (Typ)[2]	Ripple & Noise (Max)[2]
	V	See page 9	%		mVp-p		%		mVp-p	
MGJ6D051510DC	4.5 - 9	IGBT	5	10	150	200	5	10	70	110
MGJ6D121510DC	9 - 18	IGBT	5	10	150	200	5	10	70	110
MGJ6D241510DC	18 - 36	IGBT	5	10	150	200	5	10	70	110
MGJ6D052005DC	4.5 - 9	SiC	5	10	150	200	5	10	70	110
MGJ6D122005DC	9 - 18	SiC	5	10	150	200	5	10	70	110
MGJ6D242005DC	18 - 36	SiC	5	10	150	200	5	10	70	110
MGJ6D051505DC	4.5 - 9	MOSFET	5	10	150	200	5	10	70	110
MGJ6D121505DC	9 - 18	MOSFET	5	10	150	200	5	10	70	110
MGJ6D241505DC	18 - 36	MOSFET	5	10	150	200	5	10	70	110
MGJ6D051510SC	4.5 - 9	IGBT	5	10	150	200	5	10	70	110
MGJ6D121510SC	9 - 18	IGBT	5	10	150	200	5	10	70	110
MGJ6D241510SC	18 - 36	IGBT	5	10	150	200	5	10	70	110
MGJ6D052005SC	4.5 - 9	SiC	5	10	150	200	5	10	70	110
MGJ6D122005SC	9 - 18	SiC	5	10	150	200	5	10	70	110
MGJ6D242005SC	18 - 36	SiC	5	10	150	200	5	10	70	110
MGJ6D051505SC	4.5 - 9	MOSFET	5	10	150	200	5	10	70	110
MGJ6D121505SC	9 - 18	MOSFET	5	10	150	200	5	10	70	110
MGJ6D241505SC	18 - 36	MOSFET	5	10	150	200	5	10	70	110

1. Components are supplied in tray packaging, please refer to package specification section for more details.
2. See ripple & noise test method.
3. Between 50% and 100% rated output current.

SELECTION GUIDE (Continued)

Order Code[1]	Nominal Input Voltage	Input Current at Rated Load	Efficiency (Min)	Efficiency (Typ)	Isolation Capacitance	MTTF[2]	
						MIL 217	Telecordia
	V	mA	%		pF	kHrs	
MGJ6D051510DC	5	1500	77.5	80	15	627	12,576
MGJ6D121510DC	12	620	77.5	80	15	789	19,546
MGJ6D241510DC	24	300	80	82	15	784	19,570
MGJ6D052005DC	5	1500	77.5	80	15	627	12,576
MGJ6D122005DC	12	620	77.5	80	15	789	19,546
MGJ6D242005DC	24	300	80	82	15	784	19,570
MGJ6D051505DC	5	1500	77.5	80	15	627	12,576
MGJ6D121505DC	12	620	77.5	80	15	789	19,546
MGJ6D241505DC	24	300	80	82	15	784	19,570
MGJ6D051510SC	5	1500	74	77.5	15	492	13,469
MGJ6D121510SC	12	620	78	80.5	15	789	19,546
MGJ6D241510SC	24	300	80	82	15	784	19,570
MGJ6D052005SC	5	1500	74	77.5	15	492	13,469
MGJ6D122005SC	12	620	78	80.5	15	789	19,546
MGJ6D242005SC	24	300	80	82	15	784	19,570
MGJ6D051505SC	5	1500	74	77.5	15	492	13,469
MGJ6D121505SC	12	620	78	80.5	15	789	19,546
MGJ6D241505SC	24	300	80	82	15	784	19,570

1. Components are supplied in tray packaging, please refer to package specification section for more details.
2.Calculated using MIL-HDBK-217 FN2 and Telcordia SR-332 calculation model with nominal input voltage at full load.

INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage range	5V input types	4.5	5	9	V
	12V input types	9	12	18	
	24V input types	18	24	36	
Under voltage lock out	Turn on threshold MGJ6D05		4.1		V
	Turn off threshold MGJ6D05		3.0		
	Turn on threshold MGJ6D12		8.1		
	Turn off threshold MGJ6D12		7.5		
	Turn on threshold MGJ6D24		16.7		
	Turn off threshold MGJ6D24		16.3		
Input ripple current	5V input types		20		mA p-p
	12V input types		50		
	24V input types		38		

OUTPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Minimum load	Below 10% load, 5V and 15V outputs are clamped to 6V and 17V respectively	10			%
Voltage set point accuracy	Output 1		±3		%
	Output 2		±5		%
Line regulation	Low line to high line			2	%
Total Regulation				15	%
Transient response	Peak deviation (50-100% & 100-50% load swing)		0.4		$\%V_{out}$
	Settling time		0.1		ms

GENERAL CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Switching frequency			100		kHz

ISOLATION CHARACTERISTICS

Parameter		Conditions		Min.	Typ.	Max.	Units
Isolation test voltage		Production tested for 1 second		5700			VDC
		Qualification tested for 1 minute		5700			
Resistance		Viso = 1kVDC		100			GΩ
Continuous barrier withstand voltage		Non-safety barrier application				3000	VDC
Safety standard	UL60950-1	Reinforced	Creepage and clearance 8mm			250	Vrms
	ANSI/AAMI ES60601-1	2 MOPP				250	

TEMPERATURE CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Operation	See derating graphs	-40		105	°C
Storage		-50		125	
Product temperature rise above ambient	100% Load, Nom V_{IN}, Still Air		30		

ABSOLUTE MAXIMUM RATINGS

Short-circuit protection	Continuous
Lead temperature 1.0mm from case for 10 seconds (to JEDEC JESD22-B106)	260°C
Input voltage, MGJ6 5V input types	12V
Input voltage, MGJ6 12V input types	20V
Input voltage, MGJ6 24V input types	40V
Wave Solder	Wave Solder profile not to exceed the profile recommended in IEC 61760-1 Section 6.1.3. Please refer to application notes for further information.

TECHNICAL NOTES

ISOLATION VOLTAGE

'Hi Pot Test', 'Flash Tested', 'Withstand Voltage', 'Proof Voltage', 'Dielectric Withstand Voltage' & 'Isolation Test Voltage' are all terms that relate to the same thing, a test voltage, applied for a specified time, across a component designed to provide electrical isolation, to verify the integrity of that isolation.
Murata Power Solutions MGJ6 series of DC-DC converters are all 100% production tested at 5.7kVDC for 1 second and have been qualification tested at 5.7kVDC for 1 minute.

The MGJ6 series is recognised by Underwriters Laboratory, please see safety approval section for more information. When the insulation in the MGJ6 series is not used as a safety barrier, i.e. provides functional isolation only, continuous or switched voltages across the barrier up to 3kV are sustainable. This is established by measuring the partial discharge Inception voltage in accordance with IEC 60270. Please contact Murata for further information.

REPEATED HIGH-VOLTAGE ISOLATION TESTING

It is well known that repeated high-voltage isolation testing of a barrier component can actually degrade isolation capability, to a lesser or greater degree depending on materials, construction and environment. We therefore strongly advise against repeated high voltage isolation testing, but if it is absolutely required, that the voltage be reduced by 20% from specified test voltage.

SAFETY APPROVAL

ANSI/AAMI ES60601-1

The MGJ6 series has been recognised by Underwriters Laboratory (UL) to ANSI/AAMI ES60601-1 and provides 2 MOPP (Means Of Patient Protection) based upon a working voltage of 250 Vrms max., between Primary and Secondary.

UL 60950

The MGJ6 series has been recognised by Underwriters Laboratory (UL) to UL 60950 for reinforced insulation to a working voltage of 250Vrms with a maximum measured product operating temperature of 130°C.

Creepage and clearance 8mm.

FUSING

The MGJ6 Series of converters are not internally fused so to meet the requirements of UL an anti-surge input line fuse should always be used with ratings as defined below.
Input Voltage, 5V 4A
Input Voltage,12V 2A
Input Voltage,15V 1A
All fuses should be UL recognised, 125V rated.

RoHS COMPLIANCE, MSL, PSL AND SOLDERING INFORMATION

RoHS COMPLIANT

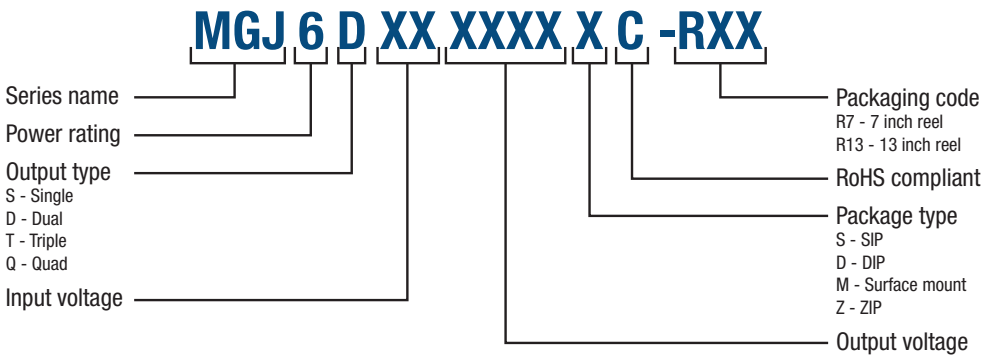
This series is compatible with RoHS soldering systems with a peak wave solder temperature of 260ºC for 10 seconds based on IEC 61760-1. Please refer to application notes for further information. The pin termination finish on this product series is Tin with Nickel Preplate. The series is backward compatible with Sn/Pb soldering systems.

ENVIRONMENTAL VALIDATION TESTING

The following tests have been conducted on this product series, please contact Murata if further information about the tests is required.

Test	Standard	Condition
Temperature cycling	MIL-STD-883 Method 1010, Condition B	10 cycles between two chambers set to achieve -55°C and +125°C.The dwell time shall not be less than 10min and the load shall reach the specified temperature in 15min.
HAST (Unbiased)	JEDEC JESD22-A118	96Hrs +2/-0Hrs at 130°C ± 2°C, 85% ± 5% R.H.
High Temperature Storage life	JEDEC JESD22-A103, Condition A	125°C +10/-0°C for ≥1000 hours
Vibration	BS EN 61373 with respect to BS EN 60068-2-64, Test Fh Category 1 Class B	5 – 150Hz. Level at each axis – Vertical, Traverse and Longitudinal: 5.72m/s2 rms. 5 hours in each axis. Crest factor: 3 Sigma. Device is secured via pins
Shock	BS EN 61373, Category 1 Class B	Test is 30ms duration, 3 shocks in each sense of 3 mutually perpendicular axis (18 shocks total). Level at each axis: Vertical, Traverse and Longitudinal: 50m/s2. Device is secured via pins.
Solderability	IPC/ECA J-STD-002D. Test A1	Parts are baked for 4 hours at a temperature of 155°C within 72 hours they are dipped in flux for 10 seconds. Followed by dipping in a solder pot at 255°C ± 5°C for 5 seconds (96SC tin/silver/copper)
Solvent cleaning	Resistance to cleaning agents	Solvent – Novec 71IPA & Topklean EL-20A. Pulsed ultrasonic immersion 45°C- 65°C
Solvent Resistance	MIL-STD-883 Method 2015	The parts and the bristle portion of the brush are immersed in Isopropanol for a minimum of 1 minute. The parts are brushed 3 times, after the third time the parts are blown dry and inspected.
Solder heat	JEDEC JESD22-B106	The test sample is subjected to a molten solder bath at 260 ±5°C for 10 +2/-0 seconds (96SC tin/silver/copper). The leads are dipped in the solder bath to within 1mm of the device body.
Lead Integrity (Adhesion)	MIL-STD 883 Method 2025	Leads are bent through 90º until a fracture occurs.
Lead Integrity (Fatigue)	MIL-STD 883 Method 2004, Condition B_2	The leads are bent to an angle of 15º. Each lead is subjected to 3 cycles.

PART NUMBER STRUCTURE



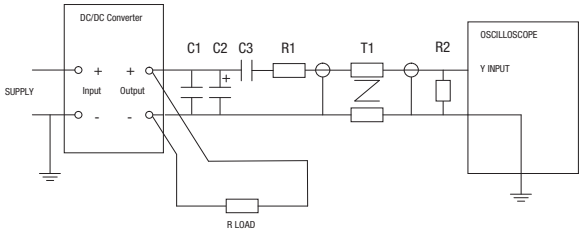
CHARACTERISATION TEST METHODS

Ripple & Noise Characterisation Method

Ripple and noise measurements are performed with the following test configuration.

C1	1µF X7R multilayer ceramic capacitor, voltage rating to be a minimum of 3 times the output voltage of the DC-DC converter
C2	10µF tantalum capacitor, voltage rating to be a minimum of 1.5 times the output voltage of the DC-DC converter with an ESR of less than 100mΩ at 100 kHz
C3	100nF multilayer ceramic capacitor, general purpose
R1	450Ω resistor, carbon film, ±1% tolerance
R2	50Ω BNC termination
T1	3T of the coax cable through a ferrite toroid
RLOAD	Resistive load to the maximum power rating of the DC-DC converter. Connections should be made via twisted wires
Measured values are multiplied by 10 to obtain the specified values.	

Differential Mode Noise Test Schematic



APPLICATION NOTES

Disable/Frequency synchronisation

Please refer to application notes for further information.

		Min	Typ	Max	Units
$\overline{\text{Disable}}$/Sync[1]	Pull Down Current		0.5		mA
	Input High	2		60	V
	Input Low	-0.6		0.8	V
Synchronisation	Frequency Range	90	100	110	kHz
	Duty Cycle	25		75	%

The $\overline{\text{Disable}}$/Synchronization pin has three modes:

1. When a DC logic low voltage is applied to this pin the MGJ6 SIP/DIP is disabled and enters a low quiescent current sleep mode.
2. When this pin is left floating or a DC logic high (CMOS/TTL compatible) voltage is applied the MGJ6 SIP/DIP is enabled and operates at the programmed frequency of 100kHz.
3. When a square wave of between 90kHz and 110kHz is applied to this pin, the switcher operates at the same frequency as the square wave. The falling edge of the square wave corresponds to the start of the switching cycle. If the signal is slower than 25Hz, it will be interpreted as enabling and disabling the part. If the MGJ6 SIP/DIP is disabled, it must be disabled for 7 clock cycles before being re-enabled.

Note: The $\overline{\text{Dis}}$/Sync pin is a high impedance TTL input and can be triggered by noise from external circuits if not treated carefully.

Please refer to "LAYOUT CONSIDERATIONS" and "SYNCHRONISATION CIRCUIT" for further details.

Click here for general guidance for gate drive applications.

LAYOUT CONSIDERATIONS

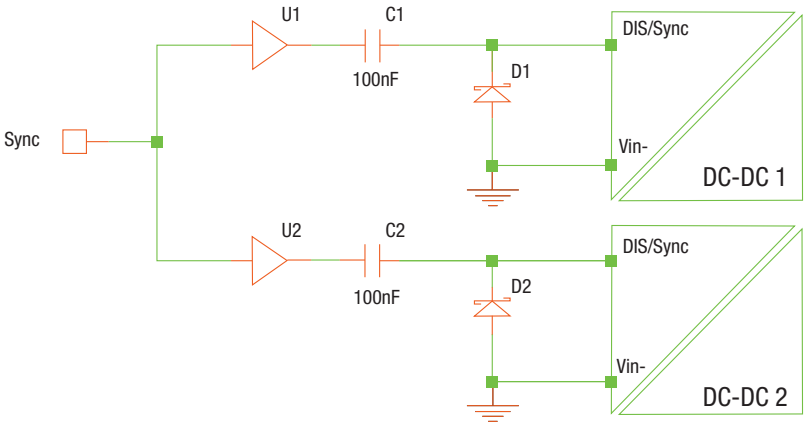
Unlike standard isolated DC-DC products the MGJ6 SIP/DIP series has been designed specifically for high side gate drive applications where the outputs are being driven to a high voltage at a very high dV/dT. This is possible due to minimum transformer isolation capacitance and considered circuit design regarding common mode transient immunity. It is important that these few simple pcb layout guidelines are implemented so as not to compromise the performance of the DC-DC and that of the overall system.

1. The keep clear area shown must not have any copper traces even on internal layers. This is not only to avoid compromising the creepage and clearance distance but also to minimise capacitive isolation between the noisy output circuits and input control circuits. In general it is good practice to maintain the same band of clearance area running directly through both the DC-DC and the gate drive isolators as shown so that input and output are kept separate and do not overlap or mesh together at any point.

2. A top layer ground plane copper area connected to –Vin can be used to create an effective screen to the underside of the MGJ6 SIP/DIP series and can also be used as a guard ring for the gate drive isolator inputs. If the $\overline{\text{Dis}}$/Synch pin is being used then it is imperative that it follows a route covered by this screen to avoid differential pick up. It should also be kept as short as possible.

Please refer to "PACKAGE SPECIFICATIONS" for recommended layout.

SYNCHRONISATION CIRCUIT



1. A suggested synchronisation circuit is shown. C1 and C2 are 100nF capacitors. D1 and D2 are schottky diodes. The capacitive isolation and close connected diode ensures that a transition from high to low is seen at the input pin even in a noisy environment or when there is a slight ground shift between devices.

2. If the $\overline{\text{Dis}}$/Sync pin is not used for synchronisation, then a 22nF capacitor can be added between the $\overline{\text{Dis}}$/Sync pin and –Vin pin to improve noise immunity. If the functionality of $\overline{\text{Dis}}$/Sync is not required, the $\overline{\text{Dis}}$/Sync pin can be connected directly to the +Vin pin to improve noise immunity.

3. One very effective method to reduce common mode transient interference is to add a common mode filter to the DC input. It may only be necessary to add one before splitting the supply to each DC-DC.

APPLICATION NOTES (Continued)

Start-up times

Typical start up times for this series, with no additional output capacitance are:

Part No.	Start-up times
	ms
MGJ6D051510DC	15
MGJ6D121510DC	15
MGJ6D241510DC	15
MGJ6D052005DC	15
MGJ6D122005DC	15
MGJ6D242005DC	15
MGJ6D051505DC	15
MGJ6D121505DC	15
MGJ6D241505DC	15
MGJ6D051510SC	15
MGJ6D121510SC	15
MGJ6D241510SC	15
MGJ6D052005SC	15
MGJ6D122005SC	15
MGJ6D242005SC	15
MGJ6D051505SC	15
MGJ6D121505SC	15
MGJ6D241505SC	15

Output capacitance must not exceed:

Output Voltage	Maximum output capacitance
V	µF
-5	470
-10	220
15	220
20	150

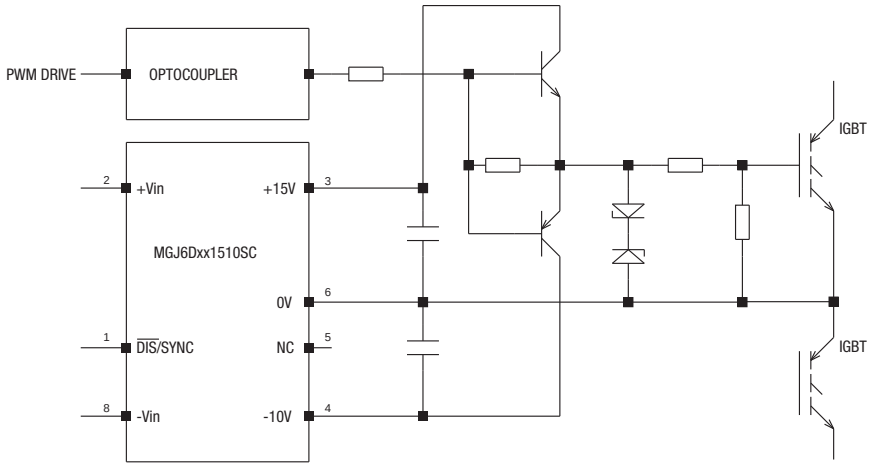
Output configurations for power switches

Terminal	Pin (SIP)	Pin (DIP)	IGBT	SIC	MOSFET
15V Output	3	5	+15V 0.24A	+20V 0.24A	+15V 0.3A
15V Return 5VA Output	6	4	0V	No connection	0V
5VA Return 5VB Output	5	3	No connection	0V	-5V 0.3A
5VB Return	4	2	-10V 0.24A	-5V 0.24A	No connection

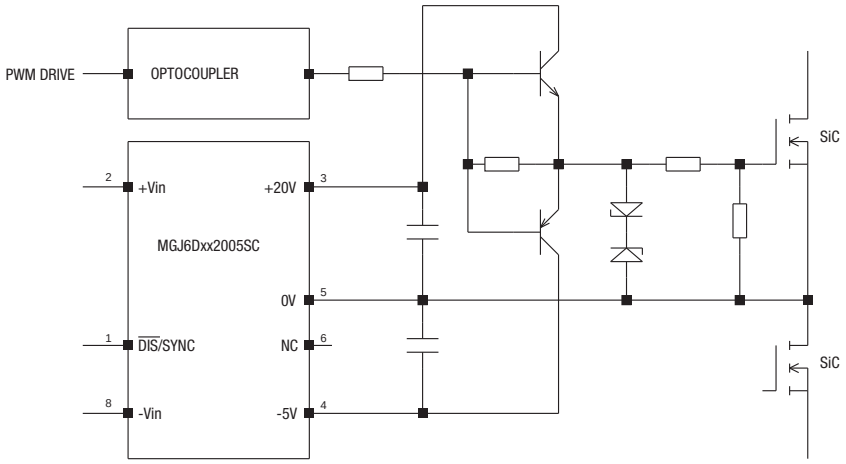
APPLICATION NOTES (Continued)

Schematic for driving IGBT, SiC & MOSFET (SIP)

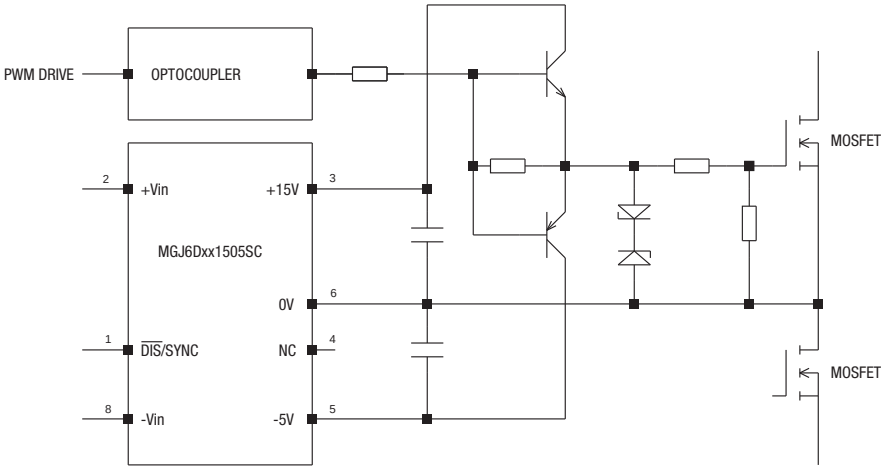
MGJ DC-DC CONNECTIONS FOR DRIVING IGBT DEVICES



MGJ DC-DC CONNECTIONS FOR DRIVING SiC DEVICES



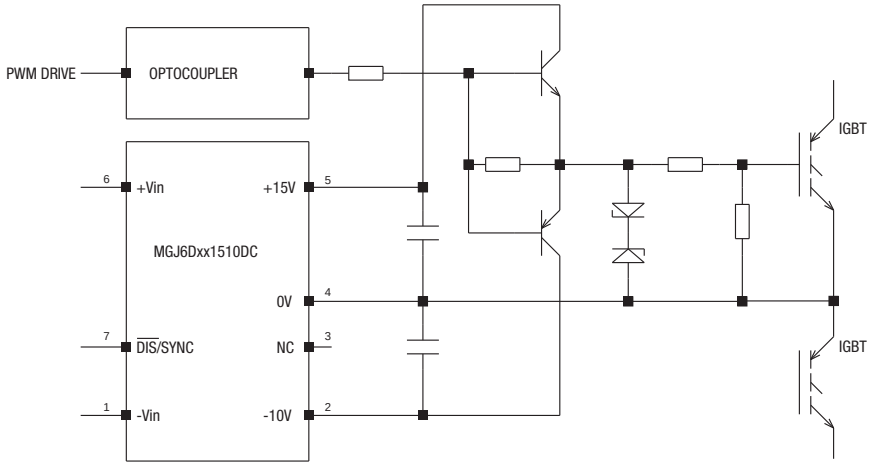
MGJ DC-DC CONNECTIONS FOR DRIVING MOSFET DEVICES



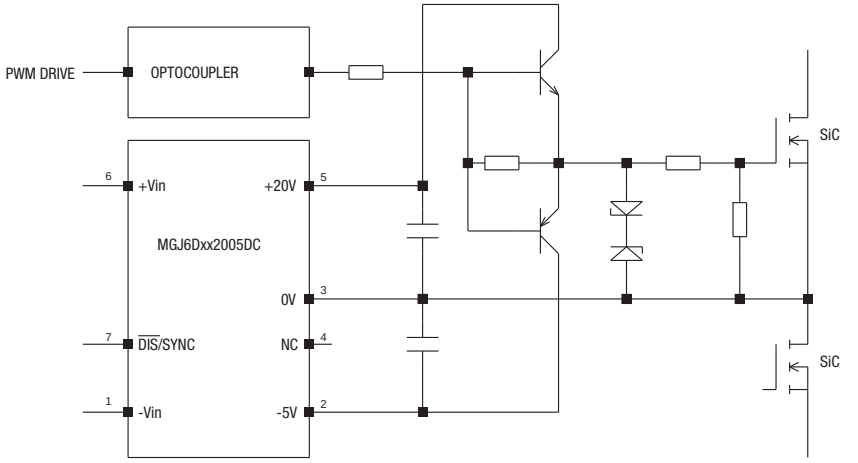
APPLICATION NOTES (Continued)

Schematic for driving IGBT, SiC & MOSFET (DIP)

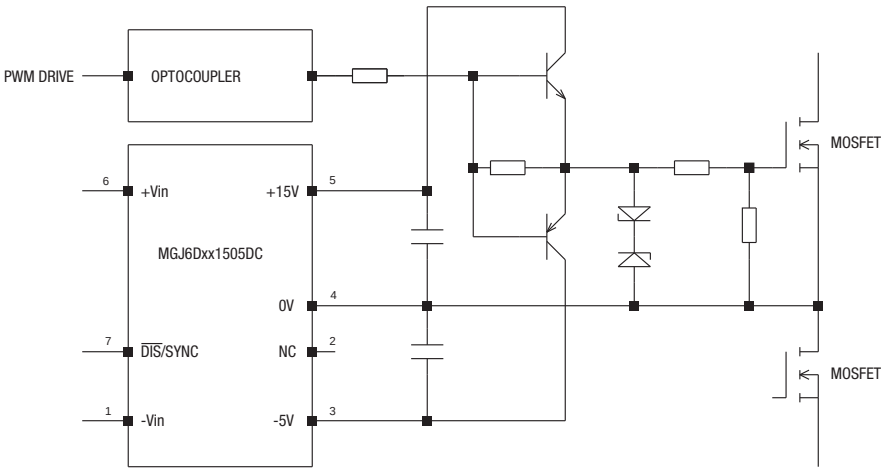
MGJ DC-DC CONNECTIONS FOR DRIVING IGBT DEVICES



MGJ DC-DC CONNECTIONS FOR DRIVING SiC DEVICES

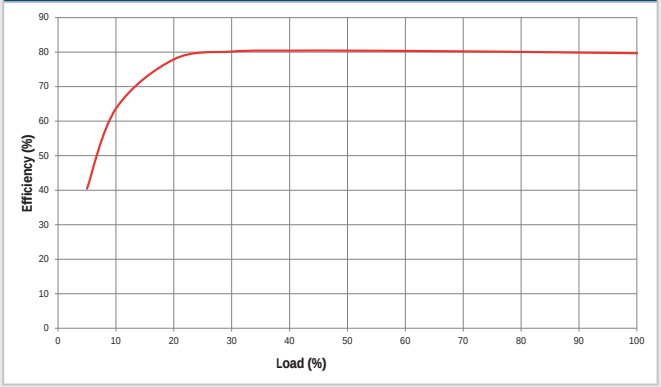


MGJ DC-DC CONNECTIONS FOR DRIVING MOSFET DEVICES

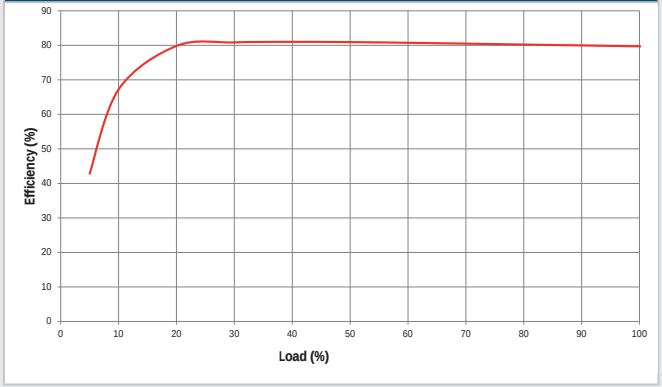


EFFICIENCY VS LOAD

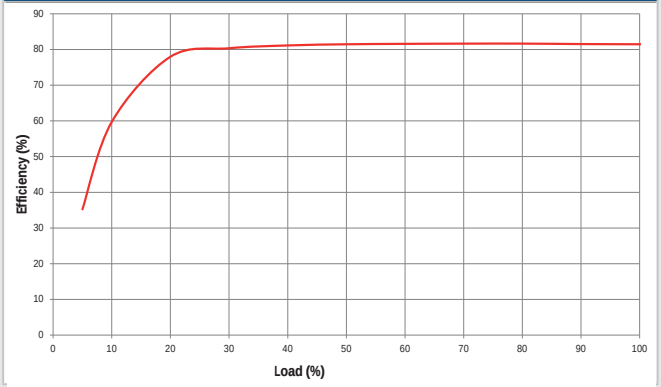
MGJ6D05xxxxDC



MGJ6D12xxxxDC



MGJ6D24xxxxDC



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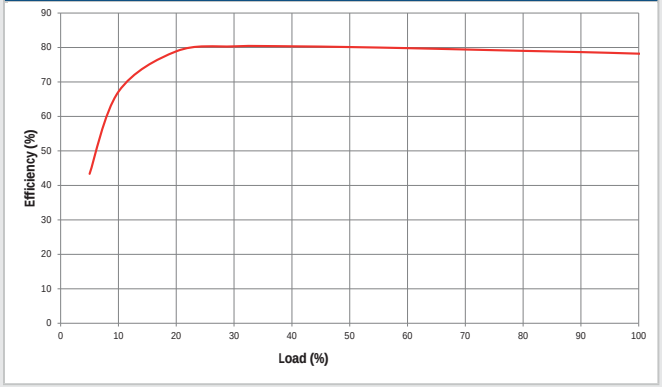

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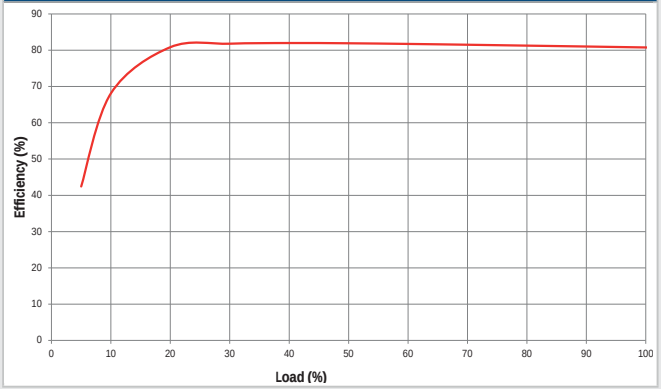

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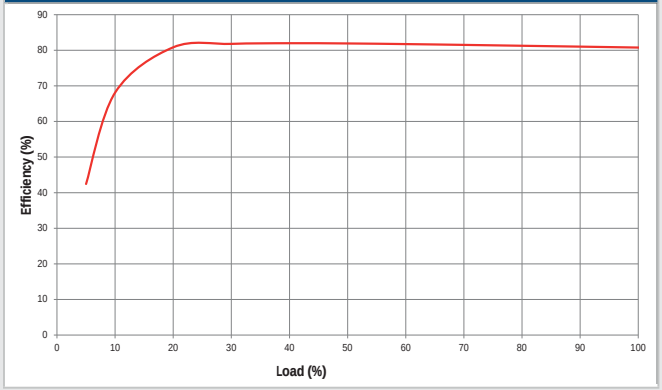
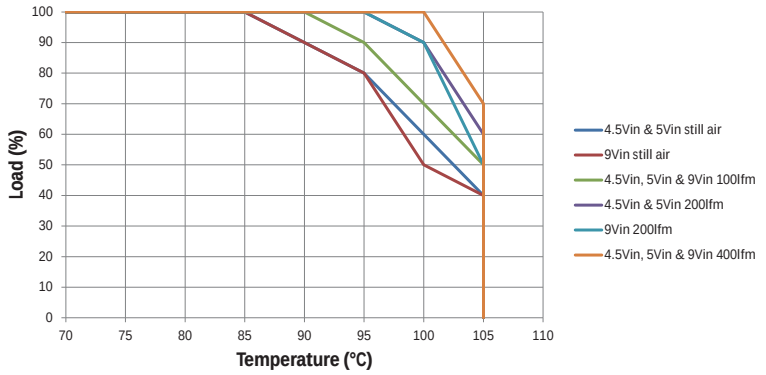


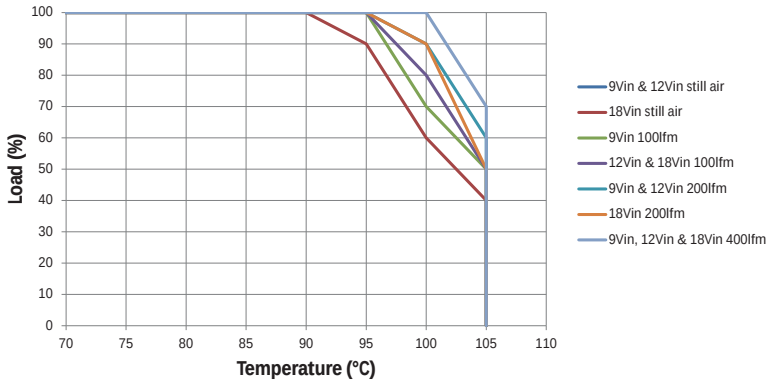
DERATING GRAPHS

Derating curves are based on IPC-9592. With no derating some components may be operating at the manufacturers maximum temperature ratings.

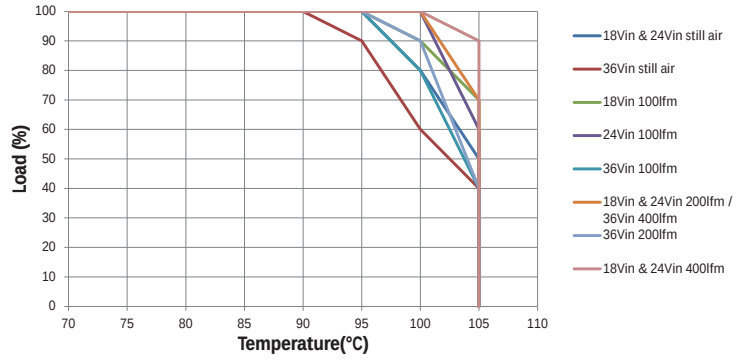
MGJ6 5V Input



MGJ6 12V Input



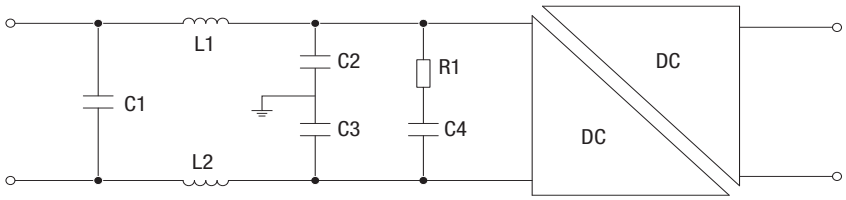
MGJ6 24V Input



EMC FILTERING AND SPECTRA

FILTERING

The following filter circuit and filter table shows the input filters typically required to meet EN 55022 Curve B, Quasi-Peak EMC limit, as shown in the following plots. The following plots show positive and negative quasi peak and CISPR22 Average Limit B (purple line) and Quasi Peak Limit B (pink line) adherence limits. If a high dv/dt above 80kV/us is expected from output to input it is advised that a common mode filter is used on the input without Y capacitors. This will reduce the common mode current and reduce interference with primary side circuits.

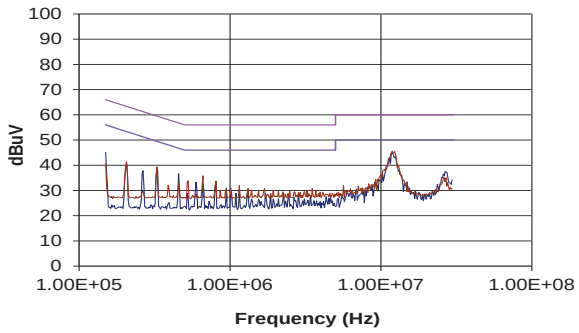


C1, C2 & C3 Polyester or ceramic capacitor

C4 Electrolytic capacitor (note R1 could be omitted if C4 has ESR >= R1)

TO MEET CURVE B						
Part Number	C1	L1&2	Through Hole	C2&3	R1	C4
MGJ6D05XXXXXC	3.3uF	10uH	47100SC	10nF	500mΩ	470uF
MGJ6D12XXXXXC	3.3uF	10uH	47100SC	10nF	500mΩ	470uF
MGJ6D24XXXXXC	3.3uF	10uH	47100SC	10nF	500mΩ	470uF

MGJ6D05xxxxDC



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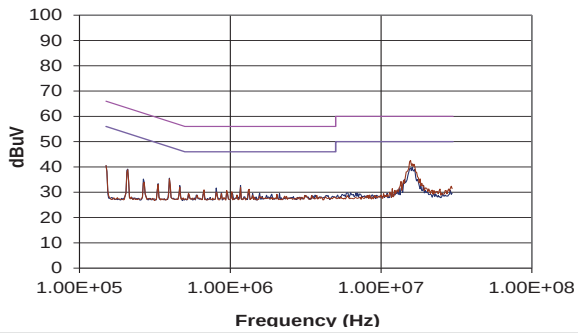

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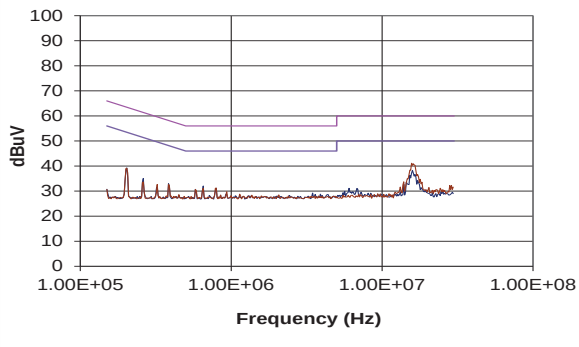

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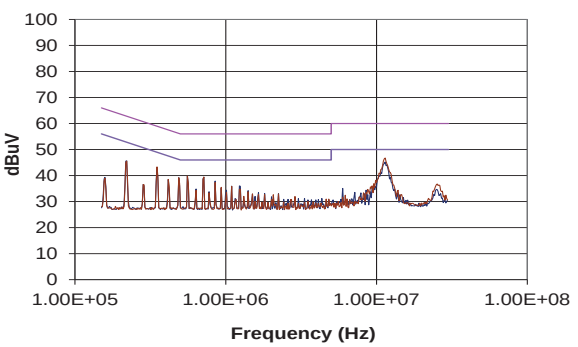
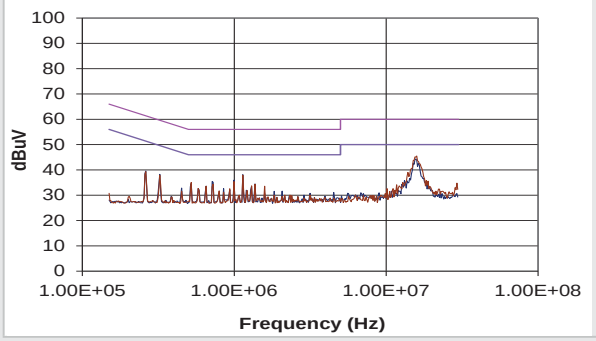


EMC FILTERING AND SPECTRA (Continued)

MGJ6D12xxxxSC



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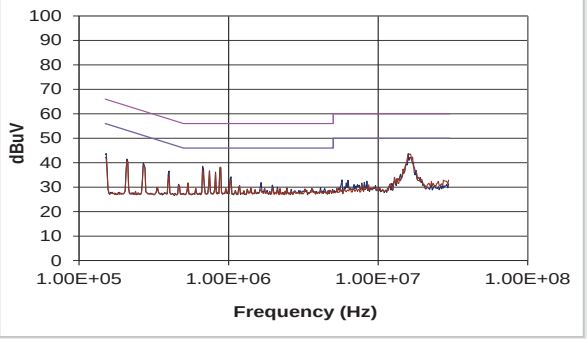
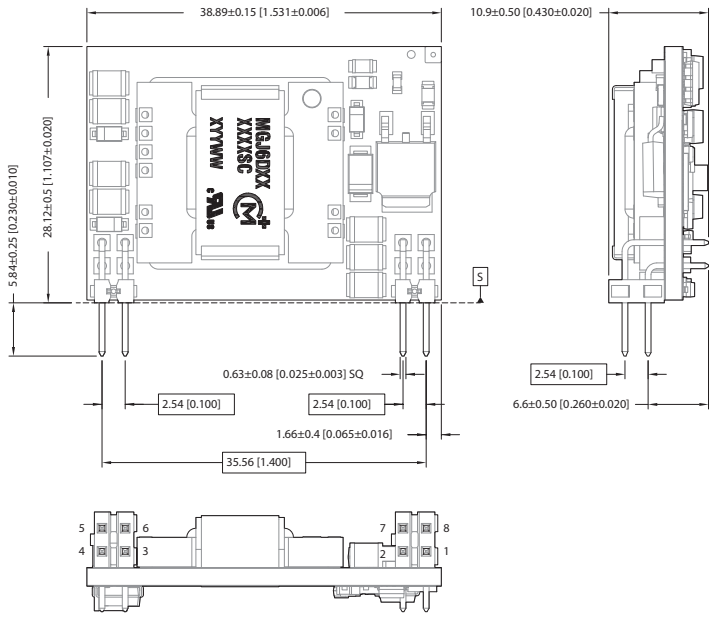


PACKAGE SPECIFICATIONS

MECHANICAL DIMENSIONS (SIP)



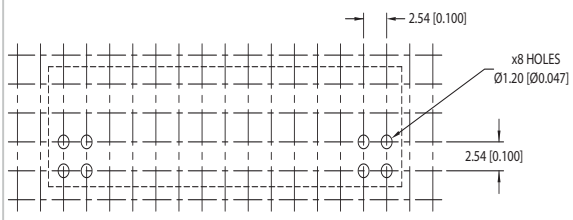
All dimensions in mm (inches), Controlling dimensions is mm.
All pins on a 2.54 (0.100) pitch and within ±0.1 (0.004) of true position from pin 1 at seating plane 'S'
Components shown for reference only

Weight: 12g

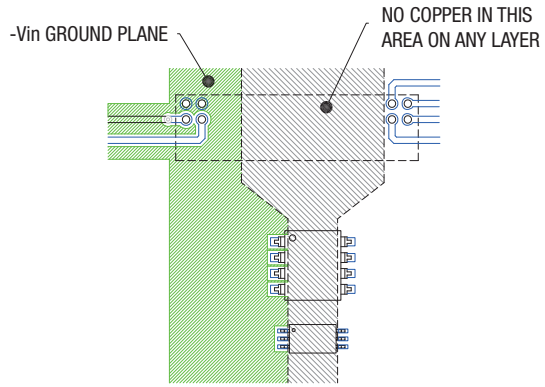
PIN CONNECTIONS (SIP)

Pin	Function
1	$\overline{\text{Dis}}$/Sync
2	+Vin
3	15Vout
4	5VB RTN
5	5VA RTN/5VB
6	15V RTN/5VA
7	-Vin
8	-Vin

RECOMMENDED FOOTPRINT DETAILS (SIP)



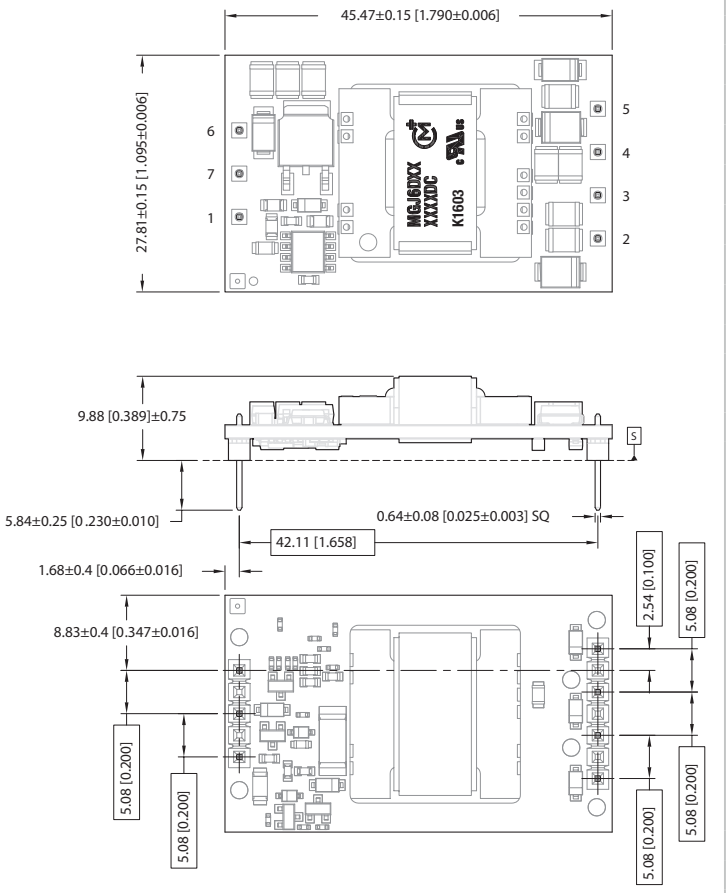
RECOMMENDED LAYOUT (SIP)



Please refer to "LAYOUT CONSIDERATIONS" for further details.

PACKAGE SPECIFICATIONS (Continued)

MECHANICAL DIMENSIONS (DIP)



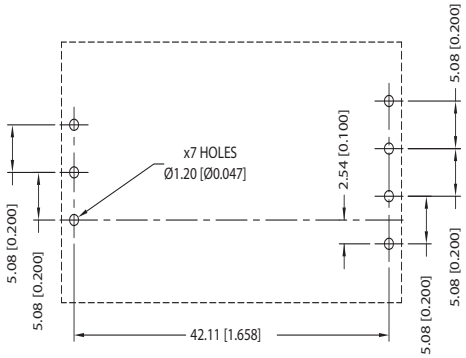
All dimensions in mm (inches), Controlling dimensions is mm.
All pins on a 2.54 (0.100) pitch and within ±0.1 (0.004) of true position from pin 1 at seating plane 'S'
Components shown for reference only

Weight: 12g

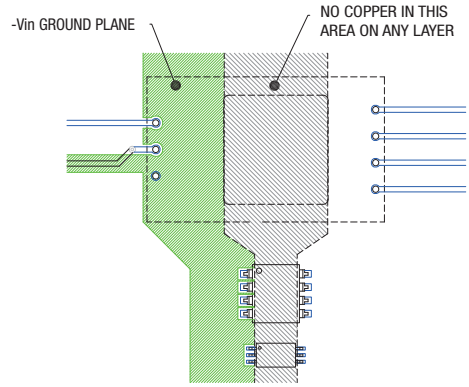
PIN CONNECTIONS (DIP)

Pin	Function
1	-Vin
2	5VB RTN
3	5VA RTN/5VB
4	15V RTN/5VA
5	15Vout
6	+Vin
7	$\overline{\text{Dis}}$/Sync

RECOMMENDED FOOTPRINT DETAILS (DIP)



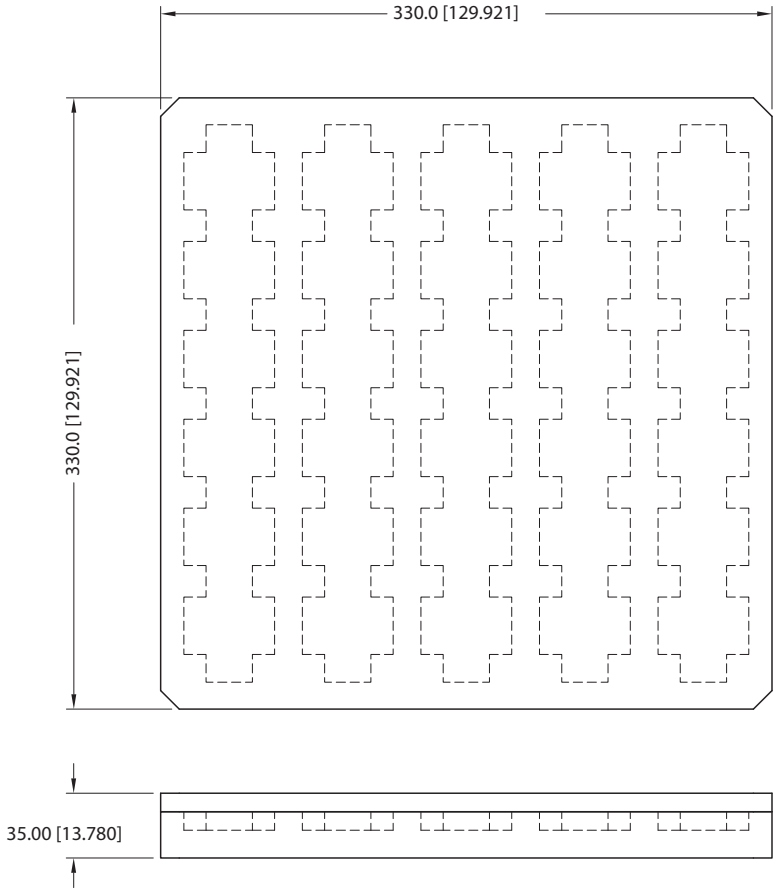
RECOMMENDED LAYOUT (DIP)



Please refer to "LAYOUT CONSIDERATIONS" for further details.

PACKAGING SPECIFICATIONS (Continued)

TRAY OUTLINE DIMENSIONS



Antistatic Tray
Quantity: 30

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