

CHIP MONOLITHIC CERAMIC CAPACITOR GRM0335C1HR40WD01_ (0201, C0G, 0.4pF, 50Vdc)

_: packaging code

Reference Sheet

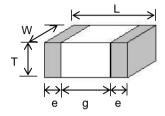
1.Scope

This product specification is applied to Chip Monolithic Ceramic Capacitor used for General Electronic equipment.

2.MURATA Part NO. System

(Ex.)	GRM	03	3	5C	1H	R40	W	D01	D	
		(1)L/W	(2)T	(3)Temperature	(4)DC Rated	(5)Nominal	(6)Capacitance	(7)Murata's	(8)Packaging	g
		Dimensions	Dimensions	Characteristics	Voltage	Capacitance	Tolerance	Control Code	Code	

3. Type & Dimensions



- 1	Ήl	nit:	mı	m١
,	(Oi	ш.	,,,,,	11)

(1)-1 L	(1)-2 W	(2) T	е	g
0.6±0.03	0.3±0.03	0.3±0.03	0.1 to 0.2	0.2 min.

4.Rated value

` '	e Characteristics Code):F(EIA)	(4) DC Rated	(5) Nominal	(6) Capacitance	Specifications and Test Methods (Operationg Temp. Range)	
Temp. coeff or Cap. Change	Temp. Range (Ref.Temp.)	Voltage	Capacitance	Tolerance		
0±30 ppm/°C	25 to 125 °C (25 °C)	50 Vdc	0.4 pF	±0.05 pF	-55 to 125 °C	

5.Package

	3-	
mark	(8) Packaging	Packaging Unit
D	φ180mm Reel PAPER	15000 pcs./Reel
J	φ330mm Reel PAPER	50000 pcs./Reel
В	Bulk Bag	1000 pcs./Bag
С	Bulk Case	50000 pcs./Case

Product specifications in this catalog are as of Aug.3,2011,and are subject to change or obsolescence without notice. Please consult the approval sheet before ordering.

Please read rating and !Cautions first.

				Spec	cification									
No.	lt	em	Temperature Compensating Ty	/pe	High Die	electric Typ	ре				Test M	lethod		
1	Operating T Range	emperature	-55°C to +125°C	R6:-55°C	to + 105°C	E4:10°C	to +125°C to + 85°C 5°C to +150°C	Refer	ence Temp	oerature	: 25°C			
	Rated Volta		See the previous pa	ges				The rated voltage is defined as the maximum voltage which applied continuously to the capacitor. When AC voltage is superimposed on DC voltage, V ^{P-P} or V ^{O-P} , whichever is large should be maintained within the rated voltage range. Visual inspection.				ge is		
	Appearance	9	No defects or abnor					_			aana (CDA	100 oizo	io boood o	n Mierocen
	Dimension Dielectric		Within the specified No defects or abnor											n Microscop
	Strength							to 7U applie charg	and 1X) of d betweer e/ discharg	r 250% o the terr ge curre	of the rated minations fo nt is less tha	voltage or 1 to 5 an 50m/	(R6, R7,C8 seconds, p A.	,E4 and F5) rovided the
	Insulation R		More than 10,000M (whichever is smalle	r)				excee minut	ding the rates of char	ated volt ging.	age at 25°C	and 7	75%RH ma:	C voltage n
	Q/ Dissipation		Within the specified 30pF and over : Q ≧ 1000	11/1/ /001/ 000= /0 000=							should be r hown in the		ed at 25°C	at the
	(D.F.)		30pF and below : Q ≧ 400+20C C:Nominal Capacitance (pF)	W.V.:25/50V W.V.:16/10V W.V.:6.3V/4V : [R9]W.V.:50V: [E4] W.V.:25Vi	:0.025max. :0.035max. :0.05max. (C :0.1max.(C 0.05max.	C < 3.3μF) C ≧ 3.3μF)	. ,	Item	Char. to 7 (1000	AC 'U,1X pF and (below)	ΔC to 7U,1X more than 10 R6,R7,C8, (C \leq 10	00pF) F5	R6,R7,F5 (C>10μF)	E4
			Capacitarice (pr.)	[F5] W.V.:25Vr	min.			Frequ	ency 1±0	.1MHz	1±0.1kH	z	120±24Hz	1±0.1kHz
				:0.05max. (C W.V.:16/10V			C ≧ 0.1μF) 0.15max.	Voltag	ge 0.5 to	5Vrms	1±0.2Vrn	ns 0	.5±0.1Vrms	0.5±0.05Vrn
	Temperature Character-ist ics	Citalige	tolerance. (Table A -1)	R6 -55°C R7 -55°C C8 -55°C L8 -55°C +125°C R9 -55°C	p. Range to +85°C to +125°C to +105°C to +125°C C to +150°C to +150°C C to +85°C	25°C W	Cap. Change Within ±15% Within ±15% Within ±22% Within ±15% Within ±15% Within+15/-40% Within ±15% Vithin+22/-56%	(1)Tel The mea sequ temp the s capa calu	temperatu sured in state that the sentially from the control of th	Comperre coeffice 3 as om step1 25°C to blerance as dividing	nsating Typicient is determined a reference of through 5 to +85°C to the temps Table A-1.	ermind u . Whe . Whe (\(\Delta C: +25\) ne capa perature The ca nces bet	n cycling the cycling the cycling the cycling the cycling pacitance dispersions the cycling the cyclinating the cyclinatin	e temperatu 5°C , other ould be within and
				F5 -30°C	to +85°C	W	Vithin+22/-82%		Step		Tem	peratur	e(°C)	
		Temperature	Within the specified	tolerance.			/	7	1			25±2		
		Coefficent	(Table A -1)		1		/					I/A V/D	S/R7/C8/L8/	(Ra)
			(12212111)						2		8(for∆C to 70 8(for F5), 10	±3(for	E4)	110)
			((2 3 4	-30±3		±3(for 25±2	E4)	
		Capacitance Drift	Within ±0.2% or ± (Whichever is large	er.)		/			3	-30±3	8(for F5), 10	±3(for 25±2 9),125=	E4) ±3(for ∆C/R 3(for other	27),
		Drift	Within ±0.2% or ± (Whichever is large *Not apply to 1X/25	ir.) 5V				The over the solution Performance	3 4 5 digh Dielerranges of the tempe specified rall measur an heat then set form the ini	-30±3 1 10 ctric Concapacitaerature ranges. ement for treatme r 24±2 tial meas	50±3(for F5), 10 50±3(for R 05±3(for C 05±3(1±3(for 25±2 9),125= 8),85±: 25±2 4 compa 4n in the ctric coll 1/-10°C com temp	E4) E3(for ΔC/R 3(for other Ted with the table should be should	27), FC) 9 25°C valud be within
10	Adhesive S Termination	Drift trength of	Within ±0.2% or ± (Whichever is large	ir.) 5V	ther defect s	should occur	г.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified real measur. form a heat then set for porm the init in the capara a eutectic 10±1 sec oldering slid and sho	tric Concapacita anges. ement for treatmer r 24±2 tital meas citor to tt solder.	stant Type nce changes show or high diele ent at 150+0 hours at roc surement. The test jig (g fhen apply done either onducted we cts such as *5N (i	±3(for 25±2 9),125= 8),85±: 25±2 companing the ctric con /-10°C com temporal companing the ctric con /-10°C com temporal companing the companing the ctric conditions are companing to the ctric conditions are companing to the ctric conditions are companing to the ctric conditions are conditional conditions are conditions are conditions are conditional conditional conditions are conditional conditions are conditional conditions are conditional conditional conditions are conditional conditional conditional conditional conditions are conditional conditional conditional conditional conditional conditional conditio	E4) E3(for ΔC/R 3(for other -	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/25	ir.) 5V	ther defect s	should occur	r.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified real measur. form a heat then set for porm the init in the capara a eutectic 10±1 sec oldering slid and sho	tric Concapacita anges. ement for treatmer r 24±2 tital meas citor to tt solder.	stant Type nce changes show or high diele ent at 150+0 hours at roc surement. The test jig (g fhen apply done either onducted we cts such as *5N (i	±3(for 25±2 9),125= 8),85±: 25±2 companing the ctric con /-10°C com temporal companing the ctric con /-10°C com temporal companing the companing the ctric conditions are companing to the ctric conditions are companing to the ctric conditions are companing to the ctric conditions are conditional conditions are conditions are conditions are conditional conditional conditions are conditional conditions are conditional conditions are conditional conditional conditions are conditional conditional conditional conditional conditions are conditional conditional conditional conditional conditional conditional conditio	red with the table shou nstant type. for one hoperature. Doxy board): ce in parall n iron or usi so that the ock, GRM18)	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	ir.) 5V	ther defect s	should occur	r.	The over the solution in the s	3 4 5 digh Dielectranges of the tempes pecified real measurorm a heat then set form the init of the capara a eutectic 10±1sec oldering slid and shom and free	tric Concapacita	stant Type nce change anges show or high diele nt at 150+0 Green tat 150+0 Gre	±3(for 25±2 9),125= 8),85±: 25±2 a compa an in the ctric con /-10°C om temp 10N for r with ar ith care heat sh GR□15 GR□03	red with the table shou enstant type. for one hoperature. Doxy board): ce in parall in iron or using so that the ock, GRM18),1N(GRIDO, 1),1N(GRIDO, 1),1N(GRIDO, 1)	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/25	ir.) 5V	ther defect s	should occur	r.	The over the solution in the s	3 4 5 digh Dielectranges of the tempes pecified real measur orm a heat then set for the tempe then set for the tempe then set for the then set for the set of the then set for the set of the then the the then the the then the the then the the then the then the	tric Concapacitaerature ranges. ement for treatme r24±2 tial measitor to the solder. Thould be confided by the	stant Type nce change anges show or high diele ent at 150+0 hours at roc surement. ne test jig (g fhen apply done eithe onducted w ats such as *5N (2N (a	±3(for 25±2 9),125= 8),85±: 25±2 e compa en in the ctric con /-10°C om temp 10N for r with ar ith care heat sh GR□15 GR□03	red with the table shou enstant type. for one hoperature. by board): ce in parall in iron or usi so that the ock, GRM18)),1N(GRIDO C	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	ir.) 5V	ther defect s	should occur	r.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ir al measur orm a heat then set footh measurement in the capaca a eutectic 10±1sec oldering slid and shom and free Type Type GR□02	tric Concapacita	stant Type nce change anges show or high diele ent at 150+0 hours at roc gurement. he test jig (g fhen apply) done eithe onducted w cts such as *5N (2N (a 0.2	±3(for 25±2 9),125= 8),85±: 25±2 companing the ctric con /-10°C companing the ctric con	red with the table shou nstant type. for one hoperature. Doxy board): ce in parall n iron or usi so that the ock, GRM18),1N(GRIDO 0.23	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	ir.) 5V	ther defect s	C	ro.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ir al measur orm a heat then set footh measurement in the capaca a eutectic 10±1sec oldering slid and shom and free GRII02 GRII03	tric Concapacita erature ranges. ement for treatme r 24±2 tial meas citor to the solder. The condition of th	stant Type nce change anges show or high diele ent at 150+0 for each of the control of the contr	±3(for 25±2 9),125= 8),85±: 25±2 25±2 companing the ctric con/-10°C commod temporal te	red with the table shou enstant type. for one hoperature. by board): ce in parall in iron or usi so that the ock, GRM18)),1N(GRIDO C. 0.23 0.3	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	erminations or ot		C C	īo.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ral measur orm a heat then set form the ini r the capa a eutectic 10±1sec oldering slid and shom and free Type Type GR□02 GR□03 GR□15	tric Concapacita erature ranges. ement for treatme r 24±2 tial meas citor to the solder. The condition of th	stant Type nce change anges show or high diele ent at 150+0 hours at roc surement. ne test jig (g Then apply done eithe onducted w cts such as *5N (2N (a 0.2 0.3 0.4	±3(for 25±2 9),125= 8),85±: 25±2 25±2 companing the ctric con/-10°C common temporal te	red with the table shou histant type, for one hoperature. Doxy board): oxy board)	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	ir.) 5V		C	īo.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ral measur orm a heat then set form the ini r the capar a eutectic 10±1sec oldering st d and shom and free GRII03 GRII03 GRII15 GRM18 GRM21 GRM31	tric Concapacita erature ranges. ement for treatme r 24±2 tial meas citor to the solder. Tould be confident of the solder of the	stant Type nce change anges show or high diele ent at 150+0 hours at roc surement. ne test jig (g Then apply) done eithe onducted w cts such as *5N (a 0.2 0.3 0.4 1.0 1.2 2.2	±3(for 25±2 9),125=8),85±3 25±2 25±2 companing the ctric con/-10°C companing the ctric con	red with the table shou histant type. for one hoperature. by board): ce in parall in iron or usi so that the ock, GRM18) 1,1N(GRIDO 0.23 0.3 0.5 1.2 1.65 2.0	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	erminations or ot		C Solder resis	īo.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ra land measur orm a heat them to the tempe specified ra a eutectic 10±1sec oldering slid and shom and free GRII03 GRII03 GRII15 GRM18 GRM31 GRM31	tric Concapacita erature ranges. ement for treatme r 24±2 tial meas citor to the solder. The condition of th	stant Type nce change anges show or high diele ent at 150+0 hours at roc surement. ne test jig (g Then apply) done eithe onducted w cts such as *5N (a 0.2 0.3 0.4 1.0 1.2 2.2	#±3(for 25±2 9),125= 8),85±3 25±2 • companie the co	red with the table shou histant type. for one hoperature. by board): ce in parall in iron or usi so that the ock, GRM18) 1,1N(GRIDO 0.23 1.2 1.65 2.0 2.9	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	erminations or ot		C Solder resis	īo.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ra la measur orm a heat them to the tempe specified ra a eutectic 10±1 sec oldering stod and shom and free GRII03 GRII03 GRII15 GRM18 GRM21 GRM31 GRM32 GRM43	ctric Concapacita rature ranges. ement for treatme r 24±2 tial meas citor to the solder. The condition of th	stant Type nce change anges show or high diele ent at 150+0 hours at roc surement. ne test jig (g Then apply) done eithe onducted w cts such as *5N (a 0.2 0.3 0.4 1.0 1.2 2.2 2.2 3.5	### 3(for 25±2 9),125=8),85±3 (25±2 25±2 4 compare in the ctric con/-10°C com temp 1 lass eper 10N for r with arrith care heat sh GR□15 GR□03 b 0.56 0.9 1.5 3.0 4.0 5.0 5.0 7.0	red with the table shou histant type, for one hoperature. Doxy board): ce in parall in iron or using that the ock, GRM18) 1,1N(GRIDO 0.23 0.3 0.5 1.2 1.65 2.0 2.9 3.7	25°C valued be within shown in Figel with the teng the reflow soldering is
10		Drift trength of	Within ±0.2% or ± (Whichever is large *Not apply to 1X/2!	erminations or ot		C Solder resis	īo.	The over the solution in the s	3 4 5 digh Dielectranges of the tempe specified ra land measur orm a heat them to the tempe specified ra a eutectic 10±1sec oldering slid and shom and free GRII03 GRII03 GRII15 GRM18 GRM31 GRM31	ctric Concapacita rature ranges. ement for treatme r 24±2 tial meas citor to the solder. The condition of th	stant Type nce change anges show or high diele ent at 150+0 hours at roc surement. ne test jig (g Then apply) done eithe onducted w cts such as *5N (a 0.2 0.3 0.4 1.0 1.2 2.2	#±3(for 25±2 9),125= 8),85±3 25±2 • companie the co	red with the table shou histant type. for one hoperature. by board): ce in parall in iron or usi so that the ock, GRM18) 1,1N(GRIDO 0.23 1.2 1.65 2.0 2.9	25°C valued be within shown in Figel with the teng the reflow soldering is

				Sp	pecification					
No.	lt	tem	Temperatur			1		Test Metho	od	
		,	Compensating		High Dielectric Type					
	Vibration		No defects or abnormali					capacitor on the test jig (gla		
ŀ	Resistance	Capacitance						ner and under the same cor		
		Q/D.F.	30pF and over : Q ≥ 1000 30pF and below: Q ≥ 400+20C C:Nominal Capacitance (pF)	W.V.:16/10 W.V.:6.3V/ [R9]W.V.:5 [E4] W.V.:2 [F5] W.V.:2	(C < 0.025max. (C < 0.068μF) : 0.05max.(C ≥ 0.068μF) : 0.025max. : 0.035max. (4V : 0.035max. (C < 3.3μF) : 0.1max.(C ≥ 3.3μF) : 0.05max. (25Vmin.: 0.025max	hav unit frec trav app	ring a tot formly be quency r rersed in blied for	hould be subjected to a sim tal amplitude of 1.5mm, the etween the approximate lim range, from 10 to 55Hz and n approximately 1 minute. T a period of 2 hours in each otal of 6 hours).	frequency be nits of 10 and return to 10F This motion sh	eing varied 55Hz. The Iz, should b nould be
				W.V.:16/	/10V:0.125max. W.V.:6.3V:0.15max.	╙				
12	Deflection	Capacitance	No defects or abnormalities. Within ± 5% or ± Within ±10%		Fig. sho refl	.2 using own in Fi ow meth	capacitor on the test jig (gla a eutectic solder. Then app ig 3 for 5±1sec. The solder nod and should be conducte	oly a force in ring should be ed with care s	the direction do not be the done by the	
	l	Change	0.5pF (Whichever is larger)			solo	dering is	uniform and free of defects	s such as hea	at shock.
12	Caldarahiji	no of	4	s F F Ipacitance IS 45	<u>. </u>		Tyy GRI GRI GRI GRN GRN GRN GRN	Pe a b DO2 0.2 0.56 DO3 0.3 0.9 DI5 0.4 1.5 NM81 1.0 3.0 M21 1.2 4.0 M31 2.2 5.0 M32 2.2 5.0 M43 3.5 7.0 M55 4.5 8.0	t:1.6m 02/03,GR□15:0 c 0.23 0.3 0.5 1.2 1.65 2.0 2.9 3.7 5.6	0.8mm) (in:mm)
	Solderabilit	•	75% of the terminations	is to be sold	dered evenly and continuously			e capacitor in a solution of		
	Termination	n				80 1	to 120°C in eutect	(4.5902) (25% rosin in weight for 10 to 30 seconds. Aftic solder solution for 2 ± 0.8	ter preheating 5 seconds at	g , immerse 230±5°C (
						Sn- 5°C).	0.5Cu solder solution for 2±		
	Resistance Soldering H		The measured and obsethe following table	erved charac	cteristics should satisfy the specifications in	Sn- 5°C Pre the	heat the	e capacitor at *120 to 150°C or in an eutectic solder solu	for 1 minu	te. Immerse
		Heat			cteristics should satisfy the specifications in	Sn- 5°C Pre the	heat the capacitoder solut	e capacitor at *120 to 150°C or in an eutectic solder solu tion at 270±5°C for 10±0	ofor 1 minustrion* or Sn-3.0.5 seconds.	te. Immerse
		Heat Appearance	the following table No defects or abnormali	ties		Sn- 5°C n Pre the sold terr	heat the capacitoder solut perature	e capacitor at *120 to 150°C or in an eutectic solder solu tion at 270±5°C for 10±0 e for 24±2 hours, then mea	ofor 1 minustrion* or Sn-3.0.5 seconds.	te. Immerse
		Heat Appearance	the following table	ties	R6,R7,C8,L8,R9:Within ±7.5% E4,F5:Within ±20%	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacito der solut inperature of apply fittal mea form a hin set at form the	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±6 e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 e initial measurement.	of for 1 minuition* or Sn-3. 0.5 seconds. asure. c constant typ	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance	the following table No defects or abnormali Within ±2.5% or ±0.2 (Whichever is larger) 30pF and over:	tities 5pF [R6,R7,C8	R6,R7,C8,L8,R9:Within ±7.5% E4,F5:Within ±20%	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacito der solut inperature of apply fittal mea form a hin set at form the	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±0 e for 24±2 hours, then meat to GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2	of for 1 minuition* or Sn-3. 0.5 seconds. asure. c constant typ	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance Change	the following table No defects or abnormali Within ±2.5% or ±0.2 (Whichever is larger)	ities 5pF	R6,R7,C8,L8,R9:Within ±7.5% E4,F5:Within ±20% ,L8] : 0.025max.(C < 0.068μF)	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacito der solut inperature of apply fittal mea form a hin set at form the	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±6 e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 e initial measurement.	of for 1 minuition* or Sn-3. 0.5 seconds. asure. c constant typ	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance Change	the following table No defects or abnormali Within ±2.5% or ±0.2 (Whichever is larger) 30pF and over: Q ≧ 1000	[R6,R7,C8 W.V.:100V	R6,R7,C8,L8,R9:Within $\pm 7.5\%$ E4,F5:Within $\pm 20\%$ L8] $: 0.025 \text{max.} (C < 0.068 \mu\text{F}) \\ : 0.05 \text{max.} (C \ge 0.068 \mu\text{F})$	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacitr der solut aperature of apply the itial mea form a han set at form the	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±1 e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 e initial measurement.	C for 1 minuition* or Sn-3. 0.5 seconds. asure. c constant typ °C for one I 2 hours.	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance Change	the following table $\label{eq:continuous} No \ defects \ or \ abnormality and the following table \label{eq:continuous} Within \ \pm 2.5\% \ or \ \pm 0.2 \ (Whichever is larger) \label{eq:continuous} 30pF \ and \ over: \ Q \ \ge \ 1000 \ 30pF \ and \ below: \ Q \ \ge \ 400+20C \ C:Nominal$	[R6,R7,C8 W.V.:100V W.V.:25/50	R6,R7,C8,L8,R9:Within $\pm 7.5\%$ E4,F5:Within $\pm 20\%$ $\begin{array}{c} \text{L8} \\ \text{: } 0.025\text{max.}(\text{C} < 0.068\mu\text{F}) \\ \text{: } 0.05\text{max.}(\text{C} \ge 0.068\mu\text{F}) \\ \text{: } 0.025\text{max.}(\text{C} \ge 0.068\mu\text{F}) \\ \text{: } 0.025\text{max.}(\text{C} \ge 0.068\mu\text{F}) \\ \text{: } 0.025\text{max.}(\text{C} \le 0.068\mu\text{F}) \\ \text{: } 0.025\text{max.}(\text{C} \ge 0.068\mu\text{F}) \\ \text{: } 0.025\text{max.}(\text$	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacite der solution perature of apply the capply the c	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±1 e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 e initial measurement.	C for 1 minuition* or Sn-3 0.5 seconds. asure. c constant typ c for one I 2 hours.	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance Change	the following table No defects or abnormali Within $\pm 2.5\%$ or ± 0.2 (Whichever is larger) $30pF \text{ and over:} \qquad Q \geq 1000$ $30pF \text{ and below:} \qquad Q \geq 400+20C$	[R6,R7,C8 W.V.:100V W.V.:25/50 W.V.:6.3V/ [R9]W.V.:5 [E4] W.V.:2 [F5] W.V.:2	R6,R7,C8,L8,R9:Within $\pm 7.5\%$ E4,F5:Within $\pm 20\%$ ' : 0.025max.(C < 0.068μF) : 0.05max. (C \ge 0.068μF) OV : 0.025max. VV : 0.035max. V4V : 0.05max. (C < 3.3μF) : 0.1max.(C \ge 3.3μF) 50V: 0.05max.	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacito der solut peraturent apply to tapply	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±(e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 initial measurement. In for GRM32/43/55 Temperature 100°C to 120°C	C for 1 minuition* or Sn-3 0.5 seconds. asure. c constant typ °C for one I 2 hours. Time 1 min.	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance Change	the following table $\label{eq:continuous} No \ defects \ or \ abnormality and the following table \label{eq:continuous} Within \ \pm 2.5\% \ or \ \pm 0.2 \ (Whichever is larger) \label{eq:continuous} 30pF \ and \ over: \ Q \ \ge \ 1000 \ 30pF \ and \ below: \ Q \ \ge \ 400+20C \ C:Nominal$	[R6,R7,C8 W.V.:100V W.V.:25/50 W.V.:16/10 W.V.:6.3V/ [R9]W.V.:5 [E4] W.V.:2 :0.05ma: W.V.:16/	R6,R7,C8,L8,R9:Within $\pm 7.5\%$ E4,F5:Within $\pm 20\%$ $\begin{array}{c} \text{L8} \\ \text{C} : 0.025\text{max.}(\text{C} < 0.068\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} \geq 0.068\mu\text{F}) \\ \text{C} : 0.025\text{max.}(\text{C} \geq 0.068\mu\text{F}) \\ \text{C} : 0.025\text{max.}(\text{C} \geq 3.3\mu\text{F}) \\ \text{C} : 0.035\text{max.}(\text{C} < 3.3\mu\text{F}) \\ \text{C} : 0.1\text{max.}(\text{C} \geq 3.3\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} < 3.3\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} < 3.3\mu\text{F}) \\ \text{C} : 0.1\text{max.}(\text{C} \geq 0.1\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} < 0.15\text{max.}(\text{C} < 0.15m$	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacito der solut peraturent apply to tapply	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±(e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 initial measurement. In for GRM32/43/55 Temperature 100°C to 120°C	C for 1 minuition* or Sn-3 0.5 seconds. asure. c constant typ °C for one I 2 hours. Time 1 min.	te. Immerse .0Ag-0.5Cu Set at roon
		Appearance Capacitance Change	the following table No defects or abnormali Within ±2.5% or ±0.2 (Whichever is larger) 30pF and over: Q ≥ 1000 30pF and below: Q ≥ 400+20C C:Nominal Capacitance (pF)	[R6,R7,C8 W.V.:100V W.V.:25/50 W.V.:16/10 W.V.:6.3V/ [R9]W.V.:5 [E4] W.V.:2 :0.05ma: W.V.:16/	R6,R7,C8,L8,R9:Within $\pm 7.5\%$ E4,F5:Within $\pm 20\%$ $\begin{array}{c} \text{L8} \\ \text{C} : 0.025\text{max.}(\text{C} < 0.068\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} \geq 0.068\mu\text{F}) \\ \text{C} : 0.025\text{max.}(\text{C} \geq 0.068\mu\text{F}) \\ \text{C} : 0.025\text{max.}(\text{C} \geq 3.3\mu\text{F}) \\ \text{C} : 0.035\text{max.}(\text{C} < 3.3\mu\text{F}) \\ \text{C} : 0.1\text{max.}(\text{C} \geq 3.3\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} < 3.3\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} < 3.3\mu\text{F}) \\ \text{C} : 0.1\text{max.}(\text{C} \geq 0.1\mu\text{F}) \\ \text{C} : 0.05\text{max.}(\text{C} < 0.15\text{max.}(\text{C} < 0.15m$	Sn-5°C Pre the sold tem *No Ini Per thei Per	cheat the capacito der solut peraturent apply to tapply	e capacitor at *120 to 150°C or in an eutectic solder solution at 270±5°C for 10±(e for 24±2 hours, then meator GRM02 asurement for high dielectric neat treatment at 150+0/-10 room temperature for 24±2 initial measurement. In for GRM32/43/55 Temperature 100°C to 120°C	C for 1 minuition* or Sn-3 0.5 seconds. asure. c constant typ °C for one I 2 hours. Time 1 min.	te. Immerse .0Ag-0.5Cu Set at roon

It			Spec	ITICATION							
Com		Temperature Compensating		High Dielectric Type		Tes	t Metho	od			
Temperatu	Appearance	The measured and observathe following table No defects or abnormalities	ved character	istics should satisfy the specifications in	under the sa according to	me conditions a the four heat tr	as (10). Pe eatments		cles owing		
	Change	(Whichever is larger)			Step	1	2	3	4		
	Q/D.F.	0 > 4000		: 0.025max. (C < 0. 068μF)	Temp.(°C)	Operating Temp. +0/-3	Room Temp.	Operating Temp. +3/-0	Room Temp.		
		$0 \ge 400 + 200$:0.025max.	(min.)	30±3	2 to 3 h dielectri	30±3	2 to 3		
	$\begin{array}{c} \text{C:Nominal} \\ \text{Capacitance (pF)} \\ \end{array} & \begin{array}{c} W.V.:6.3V/4V:0.05\text{max. } (C < 3.3\mu\text{F}) \\ :0.1\text{max. } (C \geqq 3.3\mu\text{F}) \\ [R9]W.V.:55V:0.05\text{max.} \\ [E4]W.V.:25V\text{min.} :0.025\text{max} \\ [F5]W.V.:25V\text{min.} :0.025\text{max} \\ :0.05\text{max.} (C < 0.1\mu\text{F}) :0.09\text{max.} (C \geqq 0.1\mu\text{F}) \\ W.V.:16/10V:0.125\text{max.} W.V.:6.3V:0.15\text{max.} \\ \end{array}$		Perform a heat treatment at 150+0/-10°C for one hour and then set at room temperature for 24±2 hours. Perform the measurement								
11	Strength				0.11		2	00 (050/)			
		the following table		istics should satisfy the specifications in	500±12 hou	ırs.			,		
	- ' '	Within ±5% or ±0.5pF (Whichever is larger)		R6,R7,C8,L8,R9:Within ±12.5% E4,F5:Within ±30%	measure.				,		
	Q/D.F.	30pF and over : $Q \ge 350$ 10pF and over, 30pF and below: $Q \ge 275 + \frac{5}{2}C$	W.V.:100'	V : 0.05max. (C < 0.068μF) : 0.075max. (C \ge 0.068μF) :00V :0.05max.							
		10pF and below: Q ≥ 200+10C C:Nominal Capacitance(pF)	W.V.:6.3\ [R9]W.V.: [E4] W.V. [F5] W.V.: :0.075ma	$\begin{array}{ll} W.V.:6.3V/4V:0.075 max. \ (C < 3.3 \mu F) \\ :0.125 max. \ (C \geqq 3.3 \mu F) \\ [R9]W.V.:50V: 0.075 max. \\ [E4] W.V.:25V min.:0.05 max. \\ [F5] W.V.:25V min. \end{array}$							
	I.R.										
Humidity Lo	Strength		red character	ristics should satisfy the specifications in	Apply the rated voltage at 40±2°C and 90 to 95% humidity f						
	Annogranos	the following table	the following table					500±12 hours. Remove and set for 24±2 hours at room temprature, then			
				R6,R7,C8,L8,R9:Within ±12.5% E4:Within ±30% F5:Within ±30% (W.V.>10V) F5:Within +30/-40% (W.V. ≦10V)	Initial meason	urement for F5/ ted DC voltage	16Vmax. for 1 hour	at 40±2°C .			
	Q/D.F.	30pF and over : Q ≥ 200 30pF and below: Q≥100 + 10/3 C C:Nominal Capacitance(pF)	W.V.:100' W.V.:25/5 W.V.:16/1 W.V.:6.3\ [R9]W.V.: [E4] W.V. [F5] W.V.: :0.075ma	V : 0.05max. (C < 0.068μF) : 0.075max. (C ≥ 0.068μF) :00 : 0.05max. 0V : 0.05max. //4V:0.075max. (C < 3.3μF) :0.125max. (C ≥ 3.3μF) 50V: 0.075max. :25Vmin.:0.05max. :25Vmin. x. (C<0.1μF) :0.125max. (C≥0.1μF)				om temperature			
	I.R.	More than 500M Ω or 25 Ω									
	Dielectric Strength	No defects									
		I.R. Dielectric Strength Humidity Steady State Appearance Change Q/D.F. I.R. Dielectric Strength Humidity Steady State Appearance Change Q/D.F. I.R. Dielectric Strength Humidity Load Appearance Capacitance Change Q/D.F. I.R. Dielectric Strength Humidity Load	Capacitance (Within ±2.5% or ±0.25g (Whichever is larger) Q/D.F. 30pF and over: Q ≥ 1000 30pF and below: Q ≥ 400+20C C:Nominal Capacitance (pF) Humidity The measured and observate following table Appearance No defects or abnormalitie Capacitance (Within ±5% or ±0.5pF (Whichever is larger) Q/D.F. 30pF and over: Q ≥ 350 (10pF and over) Q/D.F. 30pF and over: Q ≥ 350 (10pF and below: Q ≥ 275 + ½ C 10pF and below: Q ≥ 275 + ½ C 10pF and below: Q ≥ 200+10C C:Nominal Capacitance (pF) I.R. More than 1,000MΩor 500 (10pF) LR. More than 1,000MΩor 500 (10pF) Appearance No defects or abnormalitie Capacitance (Capacitance (Whichever is larger) Q/D.F. 30pF and over: Q ≥ 200 (10pF) Capacitance (Whichever is larger) Appearance No defects or abnormalitie (Capacitance (Within ±7.5% or ±0.75g (Whichever is larger)) Q/D.F. 30pF and over: Q ≥ 200 (10pF) Capacitance (Change (Whichever is larger)) Appearance No defects or abnormalitie (Capacitance (Change (Whichever is larger)) Q/D.F. 30pF and over: Q ≥ 200 (10pF) Appearance No defects or abnormalitie (Capacitance (Change (Whichever is larger))	Capacitance Within ±2.5% or ±0.25pF Record Change (Whichever is larger) Record Q ≥ 1000 W.V.:100V	Capacitance Within ±2.5% or ±0.25pF R6,R7,C8,L8,R9.Within ±7.5% E4,F5.Within ±20%	Capacitance Change Within ±2.5% or ±0.25pF R6.R7.C8.L8,R9.Within ±2.75% Step.	Capacitance Within ±2.5% or ±0.25pF R6,R7.C8,L8,R9.Within ±2.5% Siep 1	Capacitance Within ±2.5% or ±0.25pF R6.R7.C8.L8,R9.Within ±2.0% Sigh and over: (R6.R7.C8.L8) W.V.100V : 0.025max. (C < 0.088μF) W.V.100V : 0.05max. (C < 0.05max. (Capacidance Change Chan		

				Spec	cification				
No.	Iter	n	Temperatu Compensating		High Dielectric Type	Test Method			
18	8 High Temperature Load		The measured and observed characteristics should satisfy the specifications in the following table			temperature ±3°C for 1000±12 hours . Set for 24±2 hour			
		Appearance	No defects or abnormal	ities		room temperature, then measure. The charge/discharge current is less than 50mA.			
	1	Capacitance Change	Within ±3% or ±0.3p (Whichever is larger)	F	R6,R7,C8,L8,R9:Within $\pm 12.5\%$ E4:Within $\pm 30\%$ F5:Within $\pm 30\%$ (Cap<1.0μF) F5:Within +30/-40% (Cap \ge 1.0μF)	Initial measurement for high dielectric constant type. Apply 200% of the rated DC voltage at the maximun operating temperature ±3°C for one hour. Remove and set for 24±2 hours at room temperature.Perform initial measurement.			
		$\begin{array}{c} Q \geqq 350 \\ 10 pF \text{ and over,} \\ 30 pF \text{ and below:} \\ Q \geqq 275 + \frac{5}{2} C \\ \\ \end{array} \begin{array}{c} W.V.:100V \\ W.V.:25/50V \\ W.V.:6.3V/4 \\ \\ \end{array}$ $\begin{array}{c} Q \geqq 275 + \frac{5}{2} C \\ & W.V.:6.3V/4 \\ \end{array}$ $\begin{array}{c} [R9]W.V.:50 \\ [E4] W.V.:25 \\ [F5] W.V.:25 \\ \end{array}$		W.V.:25/50V W.V.:16/10V W.V.:6.3V/4 [R9]W.V.:50 [E4] W.V.:25 [F5] W.V.:25 :0.075max. (: 0.05max. (C < 0.068μF) : 0.075max. (C ≥ 0.068μF) /: 0.05max. /: 0.05max. V: 0.075max. (C < 3.3μF) :0.125max. (C ≥ 3.3μF) V: 0.075max.	Todas at 1997, competation offern milital measurement.			
	†	I.R.	More than 1,000MΩor	50Ω·F(Which	ever is smaller)				
	1	Dielectric Strength	No defects	·					

Table A-1

	Nominal Values	Capacitance Change from 25 °C (%)							
Char.	(ppm/°C) Note 1	-55		-	30	-10			
	(ppin/-c) Note i	Max.	Min.	Max.	Min.	Max.	Min.		
5C	0± 30	0.58	-0.24	0.40	-0.17	0.25	-0.11		
6C	0± 60	0.87	-0.48	0.59	-0.33	0.38	-0.21		
6P	-150± 60	2.33	0.72	1.61	0.50	1.02	0.32		
6R	-220± 60	3.02	1.28	2.08	0.88	1.32	0.56		
6S	-330± 60	4.09	2.16	2.81	1.49	1.79	0.95		
6T	-470± 60	5.46	3.28	3.75	2.26	2.39	1.44		
7U	-750±120	8.78	5.04	6.04	3.47	3.84	2.21		
1X	+350~-1000	-	-	-	-	-	-		

Note 1: Nominal values denote the temperature coefficient within a range of 25 °C to 125°C (for Δ C)/85°C (for other TC).

PACKAGING GRM/F Type

There are three type of packaging for chip monolithic ceramic capacitor.

Please specify the packaging code.

1.Bulk Packaging(Packaging Code=B):In a bag.

Minimum Quantity: 1000(pcs./bag), Only GR□43S, GR□55E/F: 500(pcs./bag)

2.Tape Carrier Packaging(Packaging Code:D/E/F/L/J/K)

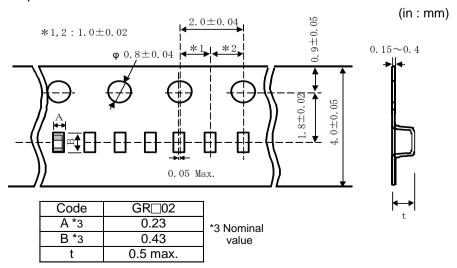
2.1 Minimum Quantity(pcs./reel)

		ф180	reel	ф330	reel
T	ype	Paper Tape	Plastic Tape	Paper Tape	Plastic Tape
		Code:D/E	Code:L	Code:J /F	Code:K
GR□02			40000 *		
GR□03		15000		50000	
GR□15		10000		50000	
GR□18		4000		10000	
GR□21	5/6/9	4000		10000	
GK <u></u> ∠Z I	A/B		3000		10000
	6/9	4000		10000	
GR□31	M/X		3000		10000
	С		2000		6000
	5/6/9	4000		10000	
	A/M		3000		10000
GR <u></u> 32	N		2000		8000
	С		2000		6000
	R/D/E		1000		4000
	М		1000		5000
	N/C/R		1000		4000
GR□43	D		1000		4000
	E		500		2000
	S		500		1500
	М		1000		5000
	N/C/R		1000		4000
GR□55	D		1000		4000
	Е		500		
	F/X		300		1500

^{* 4}mm width 1mm pitch Plastic Taping.

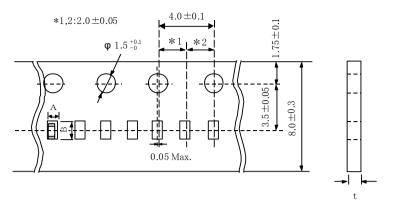
2.2 Dimensions of Tape

(1)GR□02



2.2 Dimensions of Tape

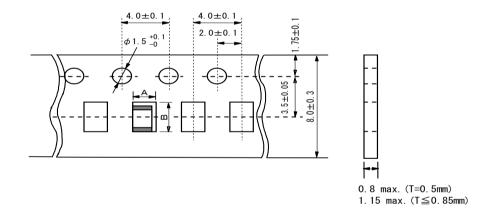
(2)GR□03/15 (in : mm)



Code	GR□03	GR□15
A *3	0.37	0.65
B *3	0.67	1.15
t	0.5 max.	0.8 max.

*3 Nominal value

(3) GR□18/21/31/32 T:0.85 max.



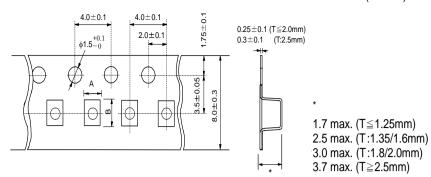
Code	GR□18	GR□21	GR□31	GR∐32
Α	1.05±0.1	1.55±0.15	2.0±0.2	2.8±0.2
В	1.85±0.1	2.3±0.15	3.6±0.2	3.6±0.2

PACKAGING GRM/F Type

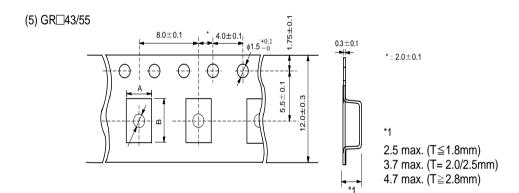
(4) GR 21/31/32

T:1.0 min.

(in:mm)



		GR□31	GR□31	
Code	GR□21	(Dimensions Tolerance	(Dimensions Tolerance	GR□32
		:±0.2within)	:±0.3)	
Α	1.45±0.2	1.9±0.2	2.1±0.2	2.8±0.2
В	2.25±0.2	3.5±0.2	3.6±0.2	3.5±0.2



Code	GR□43	GR□55
A *2	3.6	5.2
B *2	49	6.1

*2Nominal value

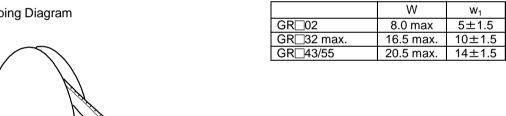
Fig.1 Package Chips

Fig.2 Dimensions of Reel

φ21±0.8

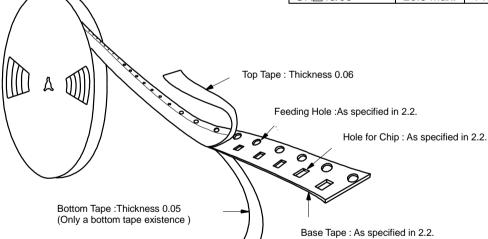
(in: mm)

Fig.3 Taping Diagram



4 180+0/-3.04 330±2.0

ф 50 min.



PACKAGING GRM/F Type

2.3 Tapes for capacitors are wound clockwise shown in Fig.3.

(The sprocket holes are to the right as the tape is pulled toward the user.)

2.4 Part of the leader and part of the vacant section are attached as follows.

Tail vacant Section Chip-mounting Unit Leader vacant Section

(in : mm)

Leader Unit
(Top Tape only)

Direction of Feed

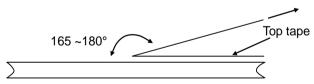
160 Min.

210 Min.

- 2.5 Accumulate pitch: 10 of sprocket holes pitch = 40 ± 0.3 mm
- 2.6 Chip in the tape is enclosed by top tape and bottom tape as shown in Fig.1.
- 2.7 The top tape and base tape are not attached at the end of the tape for a minimum of 5 pitches.
- 2.8 There are no jointing for top tape and bottom tape.
- 2.9 There are no fuzz in the cavity.
- 2.10 Break down force of top tape: 5N min.

Break down force of bottom tape : $5N \ min. \ (Only \ a \ bottom \ tape \ existence)$

- 2.11 Reel is made by resin and appeaser and dimension is shown in Fig 2. There are possibly to change the material and dimension due to some impairment.
- 2.12 Peeling off force : 0.1 to 0.6N $\!\!^{\star}$ in the direction as shown below.
 - * GR 02,03:0.05N~0.5N

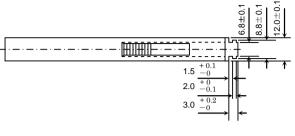


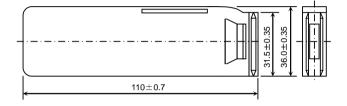
2.13 Label that show the customer parts number, our parts number, our company name, inspection number and quantity, will be put in outside of reel.

(in: mm)

3.Bulk Case Packaging (Packaging Code=C)

Fig.4 Dimensions of Bulk case





3.1 Minimum Quantity(pcs./case)

GR□15		50000	
GR□18		15000 *	
GR□21 6		10000	
	В	5000 *	

^{*} There are parts number without bulk case.

3.2 Case is made by resin of transparence or semitransparency, and appeaser and dimension is shown in Fig.4.

There are possibility to change the material and dimension due to some impairment.

3.3 Case must be marked in Customer 's part number, MURATA part number, MURATA name, Inspection number and quantity(pcs).



△Caution

■ Limitation of use

Please contact our sales representatives or product engineers before using our products for the applications listed below which require of our products for other applications than specified in this product.

- ①Aircraft equipment ②Aerospace equipment ③Undersea equipment ④Power plant control equipment
- ⑤Medical equipment ⑥Transportation equipment(vehicles,trains,ships,etc.) ⑦Traffic signal equipment
- (8) Disaster prevention / crime prevention equipment (9) Data-processing equipment
- (II) Application of similar complexity and/or requirements to the applications listed in the above

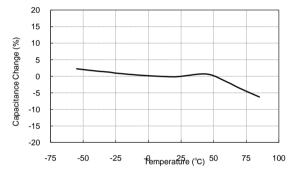
■ Storage and Operation condition

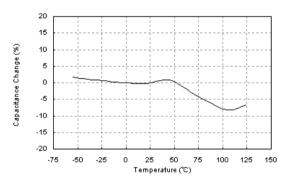
- 1. The performance of chip monolithic ceramic capacitors may be affected by the storage conditions.
- 1-1. Store capacitors in the following conditions: Temperature of +5°C to +40°C and a Relative Humidity of 20% to 70%.
- (1) Sunlight, dust, rapid temperature changes, corrosive gas atmosphere or high temperature and humidity conditions during storage may affect the solderability and the packaging performance Please use product within six months of receipt.
- (2) Please confirm solderability before using after six months. Store the capacitors without opening the original bag. Even if the storage period is short, do not exceed the specified atmospheric conditions.
- 1-2. Corrosive gas can react with the termination (external) electrodes or lead wires of capacitors, and result in poor solderability. Do not store the capacitors in an atmosphere consisting of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.).
- 1-3. Due to moisture condensation caused by rapid humidity changes, or the photochemical change caused by direct sunlight on the terminal electrodes and/or the resin/epoxy coatings, the solderability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or in high huimidity conditions

■ Rating

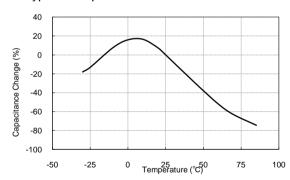
1.Temperature Dependent Characteristics

- 1. The electrical characteristics of the capacitor can change with temperature.
- 1-1. For capacitors having larger temperature dependency, the capacitance may change with temperature changes.
 - The following actions are recommended in order to insure suitable capacitance values.
- (1) Select a suitable capacitance for the operating temperature range.
- (2) The capacitance may change within the rated temperature.
 - When you use a high dielectric constant type capacitors in a circuit that needs a tight (narrow) capacitance tolerance.
 - Example: a time constant circuit., please carefully consider the characteristics of these capacitors, such as their aging, voltage, and temperature characteristics.
 - And check capacitors using your actual appliances at the intended environment and operating conditions.
- ☐ Typical temperature characteristics Char.R6 (X5R)
- ☐ Typical temperature characteristics Char.R7 (X7R)





☐ Typical temperature characteristics Char.F5 (Y5V)

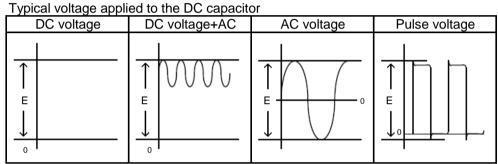


2.Measurement of Capacitance

- 1. Measure capacitance with the voltage and the frequency specified in the product specifications.
- 1-1. The output voltage of the measuring equipment may decrease when capacitance is high occasionally. Please confirm whether a prescribed measured voltage is impressed to the capacitor.
- 1-2. The capacitance values of high dielectric constant type capacitors change depending on the AC voltage applied.
 - Please consider the AC voltage characteristics when selecting a capacitor to be used in a AC circuit.

3.Applied Voltage

- 1. Do not apply a voltage to the capacitor that exceeds the rated voltage as called-out in the specifications.
- 1-1. Applied voltage between the terminals of a capacitor shall be less than or equal to the rated voltage.
 - (1) When AC voltage is superimposed on DC voltage, the zero-to-peak voltage shall not exceed the rated DC voltage.
 - When AC voltage or pulse voltage is applied, the peak-to-peak voltage shall not exceed the rated DC voltage.
 - (2) Abnormal voltages (surge voltage, static electricity, pulse voltage, etc.) shall not exceed the rated DC voltage.



(E: Maximum possible applied voltage.)

1-2. Influence of overvoltage

Overvoltage that is applied to the capacitor may result in an electrical short circuit caused by the breakdown of the internal dielectric layers .

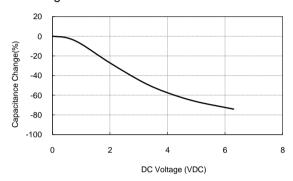
The time duration until breakdown depends on the applied voltage and the ambient temperature.

4. Applied Voltage and Self-heating Temperature

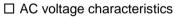
- 1. When the capacitor is used in a high-frequency voltage, pulse voltage, application, be sure to take into account self-heating may be caused by resistant factors of the capacitor.
- 1-1. The load should be contained to the level such that when measuring at atomospheric temperature of 25°C, the product's self-heating remains below 20°C and surface temperature of the capacitor in the actual circuit remains wiyhin the maximum operating temperature.

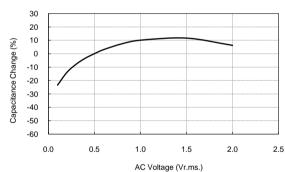
5. DC Voltage and AC Voltage Characteristic

- 1. The capacitance value of a high dielectric constant type capacitor changes depending on the DC voltage applied.
 - Please consider the DC voltage characteristics when a capacitor is selected for use in a DC circuit.
- 1-1. The capacitance of ceramic capacitors may change sharply depending on the applied voltage. (See figure) Please confirm the following in order to secure the capacitance.
- (1) Whether the capacitance change caused by the applied voltage is within the range allowed or not.
- □ DC voltage characteristics
- (2) In the DC voltage characteristics, the rate of capacitance change becomes larger as voltage increases. Even if the applied voltage is below the rated voltage. When a high dielectric constant type capacitor is in a circuit that needs a tight (narrow) capacitance tolerance. Example: a time constant circuit., please carefully consider the characteristics of these capacitors, such as their aging, voltage, and temperature characteristics. And check capacitors using your actual appliances at the intended environment and operating conditions.



2. The capacitance values of high dielectric constant type capacitors change depending on the AC voltage applied. Please consider the AC voltage characteristics when selecting a capacitor to be used in a AC circuit.



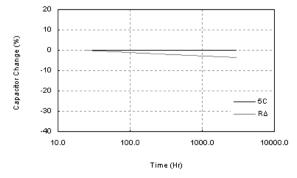


6. Capacitance Aging

1. The high dielectric constant type capacitors have the characteristic in which the capacitance value decreases with passage of time.

When you use a high dielectric constant type capacitors in a circuit that needs a tight (narrow) capacitance tolerance. Example: a time constant circuit., please carefully consider the characteristics of these capacitors, such as their aging, voltage, and temperature characteristics.

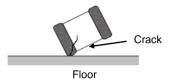
And check capacitors using your actual appliances at the intended environment and operating conditions.



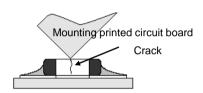
7. Vibration and Shock

- 1. Please confirm the kind of vibration and/or shock, its condition, and any generation of resonance.

 Please mount the capacitor so as not to generate resonance, and do not allow any impact on the terminals.
- 2. Mechanical shock due to falling may cause damage or a crack in the dielectric material of the capacitor. Do not use a fallen capacitor because the quality and reliability may be deteriorated.



3. When printed circuit boards are piled up or handled, the corners of another printed circuit board should not be allowed to hit the capacitor in order to avoid a crack or other damage to the capacitor.

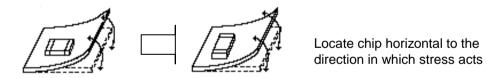


■ Soldering and Mounting

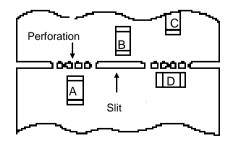
1.Mounting Position

- 1. Confirm the best mounting position and direction that minimizes the stress imposed on the capacitor during flexing or bending the printed circuit board.
- 1-1. Choose a mounting position that minimizes the stress imposed on the chip during flexing or bending of the board.

[Component Direction]



[Chip Mounting Close to Board Separation Point]



Chip arrangement Worst A-C-(B~D) Best

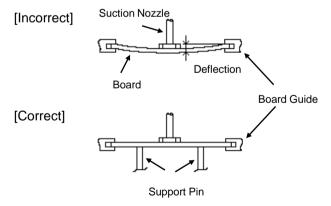
2.Information before mounting

- 1. Do Not re-use capacitors that were removed from the equipment.
- 2. Confirm capacitance characteristics under actual applied voltage.
- 3. Confirm the mechanical stress under actual process and equipment use.
- 4. Confirm the rated capacitance, rated voltage and other electrical characteristics before assembly.
- 5. Prior to use, confirm the Solderability for the capacitors that were in long-term storage.
- 6. Prior to measuring capacitance, carry out a heat treatment for capacitors that were in long-term storage.
- 7.The use of Sn-Zn based solder will deteriorate the reliability of the MLCC.

 Please contact our sales representative or product engineers on the use of Sn-Zn based solder in advance.

3. Maintenance of the Mounting (pick and place) Machine

- 1. Make sure that the following excessive forces are not applied to the capacitors.
- 1-1. In mounting the capacitors on the printed circuit board, any bending force against them shall be kept to a minimum to prevent them from any bending damage or cracking. Please take into account the following precautions and recommendations for use in your process.
- (1) Adjust the lowest position of the pickup nozzle so as not to bend the printed circuit board.
- (2) Adjust the nozzle pressure within a static load of 1N to 3N during mounting.



2.Dirt particles and dust accumulated between the suction nozzle and the cylinder inner wall prevent the nozzle from moving smoothly. This imposes greater force upon the chip during mounting, causing cracked chips. Also the locating claw, when worn out, imposes uneven forces on the chip when positioning, causing cracked chips. The suction nozzle and the locating claw must be maintained, checked and replaced periodically.

4-1.Reflow Soldering

- 1. When sudden heat is applied to the components, the mechanical strength of the components will decrease because a sudden temperature change causes deformation inside the components. In order to prevent mechanical damage to the components, preheating is required for both the components and the PCB board. Preheating conditions are shown in table 1. It is required to keep the temperature differential between the solder and the components surface (ΔT) as small as possible.
- Solderability of Tin plating termination chips might be deteriorated when a low temperature soldering profile where the peak solder temperature is below the melting point of Tin is used. Please confirm the Solderability of Tin plated termination chips before use.
- 3. When components are immersed in solvent after mounting, be sure to maintain the temperature difference (ΔT) between the component and the solvent within the range shown in the table 1.

Table 1

Part Number	Temperature Differential
GR□02/03/15/18/21/31	ΔΤ≦190°C
GR□32/43/55	ΔΤ≦130°C

Recommended Conditions

	Pb-Sn	Lead Free Solder	
Infrared Reflow Vapor Reflow		Lead Free Solder	
Peak Temperature	230~250°C	230~240°C	240~260°C
Atmosphere	Air	Air	Air or N2

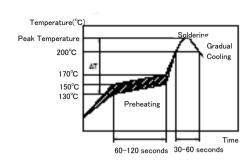
Pb-Sn Solder: Sn-37Pb

Lead Free Solder: Sn-3.0Ag-0.5Cu

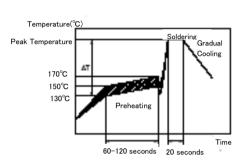
- 4. Optimum Solder Amount for Reflow Soldering
- 4-1. Overly thick application of solder paste results in a excessive solder fillet height. This makes the chip more susceptible to mechanical and thermal stress on the board and may cause the chips to crack.
- 4-2. Too little solder paste results in a lack of adhesive strength on the outer electrode, which may result in chips breaking loose from the PCB.

[Standard Conditions for Reflow Soldering]

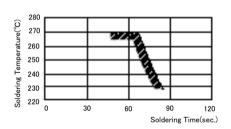
Infrared Reflow



Vapor Reflow



[Allowable Soldering Temperature and Time]



In case of repeated soldering, the accumulated soldering time must be within the range shown above.



* GRM02/03: 1/3 of Chip Thickness min.

in section

4-3. Make sure the solder has been applied smoothly to the end surface to a height of 0.2mm* min.

Inverting the PCB Make sure not to impose any abnormal mechanical shocks to the PCB.



4-2.Flow Soldering

- 1. When sudden heat is applied to the components, the mechanical strength of the components will decrease because a sudden temperature change causes deformation inside the components. In order to prevent mechanical damage in the components, preheating should be required for both of the components and the PCB board. Preheating conditions are shown in table 2. It is required to keep temperature differential between the solder and the components surface (ΔT) as small as possible.
- Excessively long soldering time or high soldering temperature can result in leaching of the outer electrodes, causing poor adhesion or a reduction in capacitance value due to loss of contact between electrodes and end termination.
- 3. When components are immersed in solvent after mounting, be sure to maintain the temperature difference (ΔT) between the component and solvent within the range shown in the table 2.
- 4. Do not apply flow soldering to chips not listed in Table 2.

Table 2

Part Number	Temperature Differential
GR□18/21/31	ΔΤ≦150°C

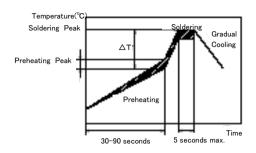
Recommended Conditions

	Pb-Sn Solder	Lead Free Solder
Preheating Peak Temperature	90~110°C	100∼120°C
Soldering Peak Temperature	240~250°C	250~260°C
Atmosphere	Air	N2

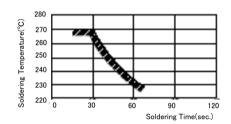
Pb-Sn Solder: Sn-37Pb Lead Free Solder: Sn-3.0Ag-0.5Cu

- 5. Optimum Solder Amount for Flow Soldering
- 5-1. The top of the solder fillet should be lower than the thickness of components. If the solder amount is excessive, the risk of cracking is higher during board bending or any other stressful condition.

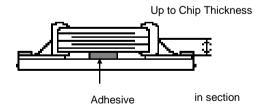
[Standard Conditions for Flow Soldering]



[Allowable Soldering Temperature and Time]



In case of repeated soldering, the accumulated soldering time must be within the range shown above.



4-3. Correction with a Soldering Iron

- 1. When sudden heat is applied to the components when using a soldering iron, the mechanical strength of the components will decrease because the extreme temperature change can cause deformations inside the components. In order to prevent mechanical damage to the components, preheating is required for both the components and the PCB board. Preheating conditions, (The "Temperature of the Soldering Iron tip", "Preheating Temperature", "Temperature Differential" between the iron tip and the components and the PCB), should be within the conditions of table 3. It is required to keep the temperature differential between the soldering Iron and the component surfaces (ΔT) as small as possible.
- 2. After soldering, do not allow the component/PCB to rapidly cool down.
- 3. The operating time for the re-working should be as short as possible. When re-working time is too long, it may cause solder leaching, and that will cause a reduction in the adhesive strength of the terminations.

Table 3

Part Number	Temperature of Soldering Iron tip	Preheating Temperature	Temperature Differential (ΔT)	Atmosphere
GR□03/15/18/21/31	350°C max.	150°C min.	ΔT≦190°C	Air
GR□32/43/55	280°C max.	150°C min.	ΔT≦130°C	Air

^{*}Applicable for both Pb-Sn and Lead Free Solder Pb-Sn Solder: Sn-37Pb

Lead Free Solder: Sn-3.0Ag-0.5Cu

- 4. Optimum Solder amount when re-working with a Soldering Iron
- 4-1. In case of sizes smaller than 0603, (GR □03/15/18), the top of the solder fillet should be lower than 2/3's of the thickness of the component or 0.5mm whichever is smaller. In case of 0805 and larger sizes, (GR □21/31/32/43/55), the top of the solder fillet should be lower than 2/3's of the thickness of the component. If the solder amount is excessive, the risk of cracking is higher during board bending or under any other stressful condition.



in section

- 4-2. A Soldering iron with a tip of ø3mm or smaller should be used. It is also necessary to keep the soldering iron from touching the components during the re-work.
- 4-3. Solder wire with Ø0.5mm or smaller is required for soldering.

4-4.Leaded Component Insertion

 If the PCB is flexed when leaded components (such as transformers and ICs) are being mounted, chips may crack and solder joints may break.
 Before mounting leaded components, support the PCB using backup pins or special jigs to prevent warping.

5.Washing

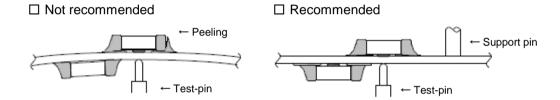
Excessive ultrasonic oscillation during cleaning can cause the PCBs to resonate, resulting in cracked chips or broken solder joints. Take note not to vibrate PCBs.

6.Electrical Test on Printed Circuit Board

- 1. Confirm position of the support pin or specific jig, when inspecting the electrical performance of a capacitor after mounting on the printed circuit board.
- 1-1. Avoid bending printed circuit board by the pressure of a test pin, etc.

 The thrusting force of the test probe can flex the PCB, resulting in cracked chips or open solder joints.

 Provide support pins on the back side of the PCB to prevent warping or flexing.
- 1-2. Avoid vibration of the board by shock when a test pin contacts a printed circuit board.



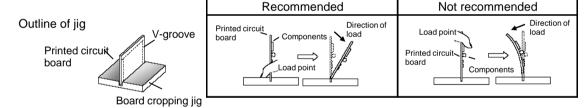
7.Printed Circuit Board Cropping

- 1. After mounting a capacitor on a printed circuit board, do not apply any stress to the capacitor that is caused by bending or twisting the board.
- 1-1. In cropping the board, the stress as shown right may cause the capacitor to crack. Try not to apply this type of stress to a capacitor.



- 2. Check of the cropping method for the printed circuit board in advance.
- 2-1. Printed circuit board cropping shall be carried out by using a jig or an apparatus to prevent the mechanical stress which can occur to the board.
 - (1) Example of a suitable jig

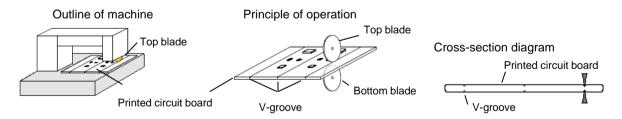
Recommended example: the board should be pushed as close to the near the cropping jig as possible and from the back side of board in order to minimize the compressive stress applied to capacitor. Not recommended example* when the board is pushed at a point far from the cropping jig and from the front side of board as below, the capacitor may form a crack caused by the tensile stress applied to capacitor.

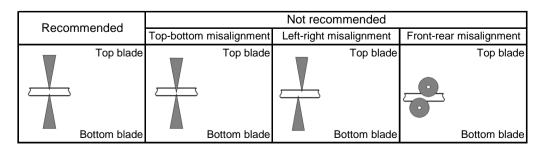


(2) Example of a suitable machine

An outline of a printed circuit board cropping machine is shown as follows. Along the lines with the V-grooves on printed circuit board, the top and bottom blades are aligned to one another when cropping the board.

The misalignment of the position between top and bottom blades may cause the capacitor to crack.





Others

1. Under Operation of Equipment

- 1-1. Do not touch a capacitor directly with bare hands during operation in order to avoid the danger of a electric shock.
- 1-2. Do not allow the terminals of a capacitor to come in contact with any conductive objects (short-circuit). Do not expose a capacitor to a conductive liquid, inducing any acid or alkali solutions.
- 1-3. Confirm the environment in which the equipment will operation is under the specified conditions. Do not use the equipment under the following environment.
 - (1) Being spattered with water or oil.
 - (2) Being exposed to direct sunlight.
 - (3) Being exposed to Ozone, ultraviolet rays or radiation.
 - (4) Being exposed to toxic gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)
 - (5) Any vibrations or mechanical shocks exceeding the specified limits.
 - (6) Moisture condensing environments.
- 1-4. Use damp proof countermeasures if using under any conditions that can cause condensation.

2. Others

2-1. In an Emergency

- (1) If the equipment should generate smoke, fire or smell, immediately turn off or unplug the equipment. If the equipment is not turned off or unplugged, the hazards may be worsened by supplying continuous power.
- (2) In this type of situation, do not allow face and hands to come in contact with the capacitor or burns may be caused by the capacitors high temperature.

2-2. Disposal of waste

When capacitors are disposed, they must be burned or buried by the industrial waste vender with the appropriate licenses.

2-3. Circuit Design

GRM Series capacitors in this catalog are not safety recognized products.

2-4. Remarks

Failure to follow the cautions may result, worst case, in a short circuit and smoking when the product is used.

The above notices are for standard applications and conditions. Contact us when the products are used in special mounting conditions.

Select optimum conditions for operation as they determine the reliability of the product after assembly. The data herein are given in typical values, not guaranteed ratings.

Rating

1. Operating Temperature

- 1. The operating temperature limit depends on the capacitor.
- 1-1.Do not apply temperatures exceeding the upper operating temperature.
 - It is necessary to select a capacitor with a suitable rated temperature which will cover the operating temperature range.
 - Also it is necessary to consider the temperature distribution in equipment and the seasonal temperature variable factor.
- 1-2. Consider the self-heating of the capacitor
 - The surface temperature of the capacitor shall be the upper operating temperature or less when including the self-heating factors.

2. Atmosphere surroundings (gaseous and liquid)

- 1. Restriction on the operating environment of capacitors.
- 1-1. The capacitor, when used in the above, unsuitable, operating environments may deteriorate due to the corrosion of the terminations and the penetration of moisture into the capacitor.
- 1-2. The same phenomenon as the above may occur when the electrodes or terminals of the capacitor are subject to moisture condensation.
- 1-3. The deterioration of characteristics and insulation resistance due to the oxidization or corrosion of terminal electrodes may result in breakdown when the capacitor is exposed to corrosive or volatile gases or solvents for long periods of time.

3.Piezo-electric Phenomenon

1. When using high dielectric constant type capacitors in AC or pulse circuits, the capacitor itself vibrates at specific frequencies and noise may be generated.

Moreover, when the mechanical vibration or shock is added to capacitor, noise may occur.

■ Soldering and Mounting

1.PCB Design

- 1. Notice for Pattern Forms
- 1-1. Unlike leaded components, chip components are susceptible to flexing stresses since they are mounted directly on the substrate.

They are also more sensitive to mechanical and thermal stresses than leaded components. Excess solder fillet height can multiply these stresses and cause chip cracking. When designing substrates, take land patterns and dimensions into consideration to eliminate the possibility of excess solder fillet height.

1-2. There is a possibility of chip crack caused by PCB expansion/contraction with heat. Because stress for chip is different depend on PCB material and structure. Especially metal PCB such as alumina has a greater risk of chip crack because of large difference of thermal expansion coefficient. In case of chip below 0402 size, there is also the same possibility of crack with a single-layered glass epoxy board.

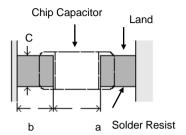
Pattern Forms

Fallem Forms	Prohibited	Correct
Placing Close to Chassis	Chassis Solder (ground) Electrode Pattern	Solder Resist
Placing of Chip Components and Leaded Components	Lead Wire	Solder Resist
Placing of Leaded Components after Chip Component	Soldering Iron Lead Wire	Solder Resist
Lateral Mounting		Solder Resist

2. Land Dimensions

2-1. Chip capacitor can be cracked due to the stress of PCB bending / etc if the land area is larger than needed and has an e amount of solder.

Please refer to the land dimensions in table 1 for flow soldering, table 2 for reflow soldering.



Please confirm the suitable land dimension by evaluating of the actual SET / PCB.

Table 1 Flow Soldering Method

Table 1 Flow Soldering Method					
Dimensions Part Number	Chip (LxW)	а	b	С	
GR□18	1.6×0.8	0.6~1.0	0.8~0.9	0.6~0.8	
GR□21	2.0×1.25	1.0~1.2	0.9~1.0	0.8~1.1	
GR□31	3.2×1.6	2.2~2.6	1.0~1.1	1.0~1.4	
	_			(in mm)	

Table 2 Reflow Soldering Method

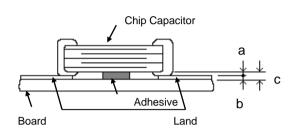
Dimensions Part Number	LxW (Dimensions Tolerance)	а	b	С
GR□02	0.4×0.2	0.16~0.2	0.12~0.18	0.2~0.23
GR□03	0.6×0.3	0.2~0.3	0.2~0.35	0.2~0.4
GR□15	1.0×0.5 (within ±0.10)	0.3~0.5	0.35~0.45	0.4~0.6
GR∐15	1.0×0.5 (±0.15/±0.20)	0.4~0.6	0.40~0.50	0.5~0.7
GR□18	1.6×0.8 (within ±0.10)	0.6~0.8	0.6~0.7	0.6~0.8
	1.6×0.8 (±0.15/±0.20)	0.7~0.9	0.7~0.8	0.8~1.0
GR□21	2.0×1.25	1.0~1.2	0.6~0.7	0.8~1.1
GR□31	3.2×1.6	2.2~2.4	0.8~0.9	1.0~1.4
GR□32	3.2×2.5	2.0~2.4	1.0~1.2	1.8~2.3
GR□43	4.5×3.2	3.0~3.5	1.2~1.4	2.3~3.0
GR□55	5.7×5.0	4.0~4.6	1.4~1.6	3.5~4.8
· · · · · · · · · · · · · · · · · · ·				(' \

(in mm)

2.Adhesive Application

 Thin or insufficient adhesive can cause the chips to loosen or become disconnected during flow soldering.
 The amount of adhesive must be more than dimension c, shown in the drawing at right, to obtain the correct bonding strength.

The chip's electrode thickness and land thickness must also be taken into consideration.



a=20~70μm b=30~35μm c=50~105μm

- 2. Low viscosity adhesive can cause chips to slip after mounting. The adhesive must have a viscosity of 5000Pa s (500ps) min. (at 25°C)
- 3. Adhesive Coverage

Part Number	Adhesive Coverage*
GR□18	0.05mg min.
GR□21	0.1mg min.
GR□31	0.15mg min.

*Nominal Value

3.Adhesive Curing

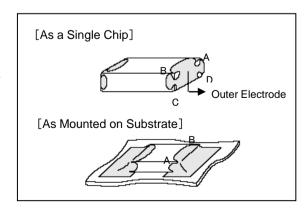
1. Insufficient curing of the adhesive can cause chips to disconnect during flow soldering and causes deterioration in the insulation resistance between the outer electrodes due to moisture absorption. Control curing temperature and time in order to prevent insufficient hardening.

4.Flux Application

- 1. An excessive amount of flux generates a large quantity of flux gas, which can cause a deterioration of Solderability.
 - So apply flux thinly and evenly throughout. (A foaming system is generally used for flow soldering).
- 2. Flux containing too a high percentage of halide may cause corrosion of the outer electrodes unless there is sufficient cleaning. Use flux with a halide content of 0.2% max.
- 3. Do not use strong acidic flux.
- Do not use water-soluble flux.
 (*Water-soluble flux can be defined as non rosin type flux including wash-type flux and non-wash-type flux.)

5.Flow Soldering

Set temperature and time to ensure that leaching of the outer electrode does not exceed 25% of the chip end area as a single chip (full length of the edge A-B-C-D shown right) and 25% of the length A-B shown below as mounted on substrate.



6.Washing

- 1. Please evaluate a capacitor by actual cleaning equipment and condition surely for confirming the quality and select the applicable solvent.
- 2. Unsuitable cleaning solvent may leave residual flux, other foreign substances, causing deterioration of electrical characteristics and the reliability of the capacitors.
- 3. Select the proper cleaning conditions.
- 3-1. Improper cleaning conditions (excessive or insufficient) may result in the deterioration of the performance of the capacitors.

7.Coating

1. A crack may be caused in the capacitor due to the stress of the thermal contraction of the resin during curing process.

The stress is affected by the amount of resin and curing contraction.

Select a resin with small curing contraction.

The difference in the thermal expansion coefficient between a coating resin or a molding resin and capacitor may cause the destruction and deterioration of the capacitor such as a crack or peeling, and lead to the deterioration of insulation resistance or dielectric breakdown.

Select a resin for which the thermal expansion coefficient is as close to that of capacitor as possible.

A silicone resin can be used as an under-coating to buffer against the stress.

2. Select a resin that is less hygroscopic.

Using hygroscopic resins under high humidity conditions may cause the deterioration of the insulation resistance of a capacitor.

An epoxy resin can be used as a less hygroscopic resin.

Others

1.Transportation

- 1. The performance of a capacitor may be affected by the conditions during transportation.
- 1-1. The capacitors shall be protected against excessive temperature, humidity and mechanical force during transportation.
- (1) Climatic condition
 - low air temperature : −40°C
 - change of temperature air/air : −25°C/+25°C
 - low air pressure: 30 kPa
 - change of air pressure : 6 kPa/min
- (2) Mechanical condition

Transportation shall be done in such a way that the boxes are not deformed and forces are not directly passed on to the inner packaging.

- 1-2. Do not apply excessive vibration, shock, and pressure to the capacitor.
- (1) When excessive mechanical shock or pressure is applied to a capacitor, chipping or cracking may occur in the ceramic body of the capacitor.
- (2) When a sharp edge of an air driver, a soldering iron, tweezers, a chassis, etc. impacts strongly on the surface of capacitor, the capacitor may crack and short-circuit.
- 1-3. Do not use a capacitor to which excessive shock was applied by dropping etc.

 The capacitor dropped accidentally during processing may be damaged.



∧ NOTE

- 1.Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.
- 2. Your are requested not to use our product deviating from this product specification.
- 3.We consider it not appropriate to include any terms and conditions with regard to the business transaction in the product specifications, drawings or other technical documents. Therefore, if your technical documents as above include such terms and conditions such as warranty clause, product liability clause, or intellectual property infringement liability clause, they will be deemed to be invalid.

单击下面可查看定价,库存,交付和生命周期等信息

>>Murata(村田)