DEVELOPMENT KIT
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TXC101

300-1000 MHz Transmitter

16-TSSOP package

- **Complies with Directive 2002/95/EC (RoHS)**

Product Overview

TXC101 is a highly integrated single chip, multi-channel, low power, high data rate RF transmitter designed to operate in the unlicensed 315/433/868 and 915 MHz frequency bands. All critical RF and baseband functions are completely integrated in the chip, thus minimizing external component count and simplifying design-ins. Its small size with low power consumption makes it ideal for various short range radio applications.

The TXC101 is a dual mode solution. In the Microcontroller mode, a generic 10MHz crystal and a low-cost microcontroller are the only requirements to create a complete Transmitter link.
In the EEPROM mode, the TXC101 can function as a complete data transmitter with any SPI compatible EEPROM and does not need a micro controller. This makes it an ideal solution for a variety of simple short range radio applications.

Key Features

- Modulation: OOK/FSK
- Frequency Hopping Spread Spectrum capability
- Operating frequency: 315/433/868/915 MHz
- Low current consumption (TX current ~ 10mA)
- Wide Operating supply voltage: 2.2 to 5.4V
- Low standby current (0.2uA)
- OOK Data rate up to 512kbps
- FSK Data rate up to 256kbps
- Support for Multiple Channels
- [315/433 Bands]: 95 Channels (100kHz)
- [868 Band]: 190 Channels (100kHz)
- [915 Band]: 285 Channels (100kHz)
- Generic 10MHz Xtal reference
- Processor or EEPROM Mode Operation
- Integrated PLL, IF & Baseband Circuitry
- Programmable Push Button Control
- Programmable Output RF Power
- Programmable, Positive/Negative FSK Deviation
- Programmable Clock Output Frequency
- Standard SPI interface
- Integrated, Programmable Low Battery Voltage Detector
- External Wake-up Events
- TTL/CMOS Compatible I/O pins
- Automatic Antenna tuning circuit
- Very few external components requirement
- No Manual Adjustment Needed for Production
- Small size plastic package: 16-pin TSSOP
- Standard 13 inch reel, 2000 pieces.

Popular applications

- Remote control applications
- Active RFID tags
- Wireless PC Peripherals
- Automated Meter reading
- Home & Industrial Automation
- Security systems
- Remote keyless entry
- Automobile Immobilizers
- Sports & Performance monitoring
- Wireless Toys
- Medical equipment
- Low power two way telemetry systems
- Wireless mesh sensors
- Wireless modules

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Table of Contents

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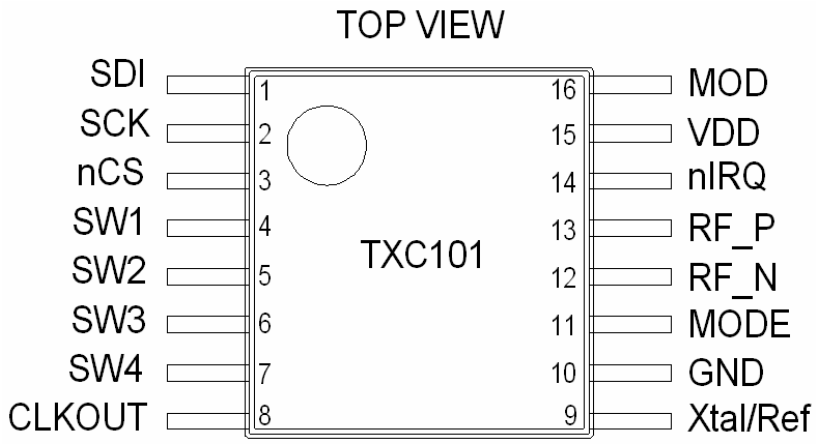
1.0 Pin Description

Processor Mode

Pin	Name	Description
1	SDI	**SPI Data In**
2	SCK	**SPI Data Clock**
3	nCS	**Chip Select Input**– Selects the chip for an SPI data transaction. The pin must be pulled 'low' for a 16-bit read or write function. See Figure 4 for timing specifications.
4	SW1	**Switch** or Push Button Input 1 with Internal pull-up resistor
5	SW2	**Switch** or Push Button Input 2 with Internal pull-up resistor
6	SW3	**Switch** or Push Button Input 3 with Internal pull-up resistor
7	SW4	**Switch** or Push Button Input 4 with Internal pull-up resistor
8	ClkOut	Optional host processor Clock Output
9	Xtal/Ref	**Xtal** - Connects to a 10MHz series crystal or an external oscillator reference. The circuit contains an integrated load capacitor (See *Configuration Register*) in order to minimize the external component count. The crystal is used as the reference for the PLL, which generates the local oscillator frequency. The accuracy requirements for production tolerance, temperature drift and aging can be determined from the maximum allowable local oscillator frequency error. Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. **Ext Ref** – An external reference, such as an oscillator, may be connected as a reference source. Connect through a .01uF capacitor.
10	GND	System Ground
11	MODE	**Mode Select –** Connect to VDD for Processor Mode.
12	RF_P	**RF Diff I/O**
13	RF_N	**RF Diff I/O**
14	nIRQ	**Interrupt Request** – Interrupt Request Output and Status Register Data Read Output.
15	VDD	Supply Voltage
16	MOD	**Modulation Input** – Serial data input for FSK or OOK modulation

1.1 Processor Mode Pin Configuration



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EEPROM Mode

Pin	Name	Description
1	SDI	**SPI Data In**
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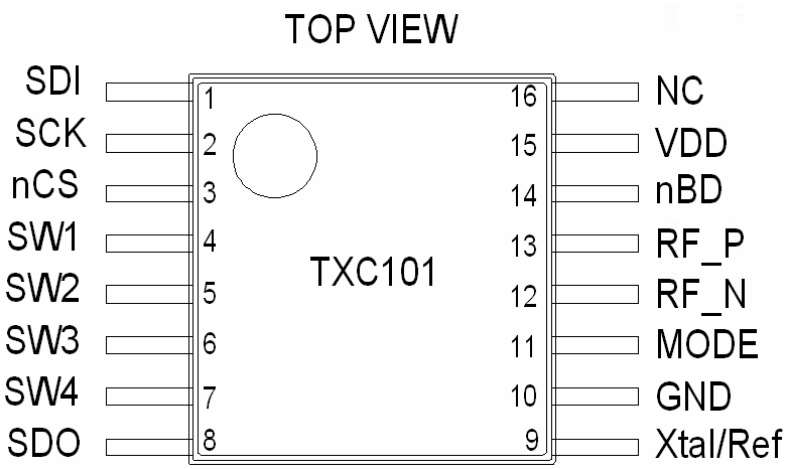
5	SW2	**Switch** or Push Button Input 2 with Internal pull-up resistor
6	SW3	**Switch** or Push Button Input 3 with Internal pull-up resistor
7	SW4	**Switch** or Push Button Input 4 with Internal pull-up resistor
8	SDO	**SPI Data Out**
9	Xtal/Ref	**Xtal** - Connects to a 10MHz series crystal or an external oscillator reference. The circuit contains an integrated load capacitor (See *Configuration Register*) in order to minimize the external component count. The crystal is used as the reference for the PLL, which generates the local oscillator frequency. The accuracy requirements for production tolerance, temperature drift and aging can be determined from the maximum allowable local oscillator frequency error. Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. **Ext Ref** – An external reference, such as an oscillator, may be connected as a reference source. Connect through a .01uF capacitor.
10	GND	System Ground
11	MODE	**Mode Select –** Connect to GND for EEPROM Mode.
12	RF_P	**RF Diff I/O**
13	RF_N	**RF Diff I/O**
14	nBD	**Low Battery Detect** – When the battery voltage falls below the programmed level this output goes "low". The voltage level is programmable through the *Battery Detect Threshold Register*.
15	VDD	Supply Voltage
16	NC	**Not used**. Tie to VDD or GND

1.2 EEPROM Mode Pin Configuration



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2.0 Functional Description

The TXC101 is a low power, frequency agile, multi-channel OOK/FSK transmitter for use in the 315, 433, 868, and 916 MHz bands. All RF transmit functions are completely integrated requiring only a single 10MHz crystal as a reference source. The TXC101 has two modes of operation: EEPROM mode and Processor mode. EEPROM mode is fully compatible with any standard SPI interface EEPROM. Functions include:

- PLL synthesizer
- Power Amp
- Crystal oscillator
- Sleep Timer
- OOK/FSK Modulation
- 4 Key/Switch Functions

The TXC101 is ideal for Frequency Hopping Spread Spectrum (FHSS) applications requiring frequency agility to meet FCC and ETSI requirements. Use of a low-cost microcontroller or SPI compatible EEPROM is all that is needed to create a complete transmitter. The TXC101 also incorporates different sleep modes to reduce overall current consumption and extend transmitter battery life. It is ideal for applications operating from typical lithium coin cells.

2.1 TXC101 Processor Mode and Application Circuit

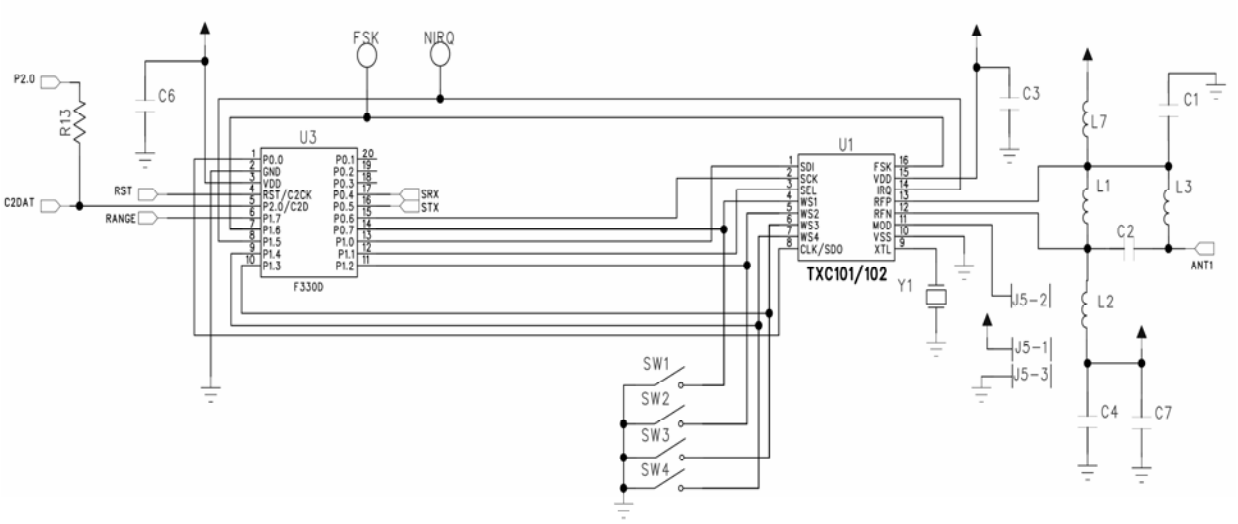

Figure 1. Typical Processor Mode Application Circuit for 50 Ohm Load

The TXC101 may be used with a typical low-cost microcontroller. All internal functions are accessible through the SPI interface. Figure 1 shows a typical connection for using a microcontroller to control the TXC101 functions.

RF Transmitter Matching

The RF pins are high impedance and differential. The optimum differential load for the RF port at a given frequency band is shown in Table 1.

TABLE 1.

	Admittance [S]	Impedance [Ohm]	Lantenna (nH)
315 MHz	9.4e-4 – j4.5e-3	43 + j214	112
433 MHz	8.4e-4 – j6.25e-3	21 + j157	59
868 MHz	1.15e-3 – j1.2e-2	7.9 + j83	15.3
916 MHz	1.2e-3 – j1.25e-2	7.6 + j79	13.9

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These values are what the RF port pins want to "see" as an antenna load for maximum power transfer. Antennas ideally suited for this would be a Dipole, Folded Dipole, and Loop. For all transmit antenna applications a bias or "choke" inductor must be included since the RF outputs are open-collector type. The TXC101 may also drive a single ended 50 Ohm load, such as a monopole antenna, using the matching circuit as shown in Figure 1. Use of a balun would provide an optimum power transfer, but the matching circuit of Figure 1 has been optimized for use with discrete components, reducing the cost associated with use of a balun.

The matching component values for a 50 Ohm load are given in Table 2.

Table 2.

Ref Des	315	433	868	916
C1	3.9pF	2.7 pF	1.8 pF	1.8 pF
C2	2.2 pF	1.5 pF	1 pF	1 pF
C4	.1uF	.1uF	.1uF	.1uF
C7	100pF	100pF	100pF	100pF
L1	72 nH	43 nH	10 nH	10 nH
L2	390nH	390nH	100nH	100nH
L3	110 nH	82 nH	27 nH	27 nH

Antenna Design Considerations

The TXC101 was designed to drive a differential output such as a Dipole or a Loop antenna. A loop antenna is recommended for applications where size is critical. The dipole is typically not an attractive option for compact designs based on its inherent size at resonance and distance needed away from a ground plane to be an efficient radiating antenna. A monopole is possible with addition of a balun or using the matching circuit in Figure 1.

PCB Layout Considerations

PCB layout is very critical. For optimal transmit and receive performance, the trace lengths at the RF pins must be kept as short as possible. Using small, surface mount components, like 0402, will yield the best performance and also keep the RF port compact. It is recommended that all RF connections are made short and direct. A good rule of thumb to adhere to is to add 1nH of series inductance to the path for every 0.1" of trace length. The crystal oscillator is also affected by additional trace length as it adds parasitic capacitance to the overall load of the crystal. To minimize this effect the crystal must be placed as close as possible to the chip and all connections must be made short and direct. This will minimize the effects of "frequency pulling" , that stray capacitance may introduce and allow the internal load capacitance of the chip to be more effective in properly loading the crystal oscillator circuit.

When an external processor is used, the TXC101 provides an on-chip clock. Even though this is an integrated function, long runs of the clock signal may radiate and cause interference. This can degrade receiver performance as well as add harmonics or unwanted modulation to the transmitter. Keep clock connections as short as possible and surround the clock trace with an adjacent ground plane pour where needed. This will help in reducing any radiation or crosstalk due to long runs of the clock signal.

Good power supply bypassing is also essential. Large decoupling capacitors should be placed at the point where power is applied to the PCB. Smaller value decoupling capacitors should then be placed at each power point of the chip as well as bias nodes for the RF port. Poor bypassing lends itself to conducted interference which can cause noise and spurious signals to couple into the RF sections, thus significantly reducing performance.

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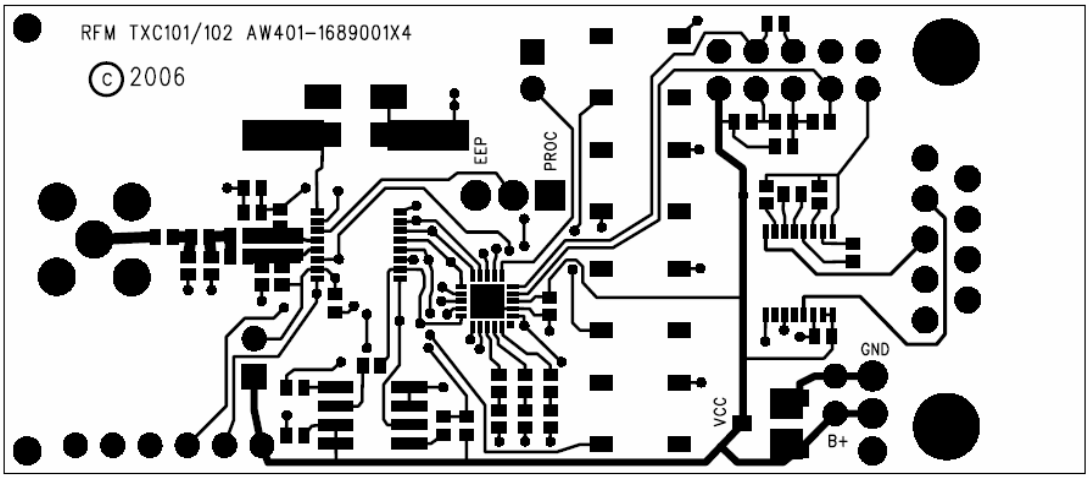
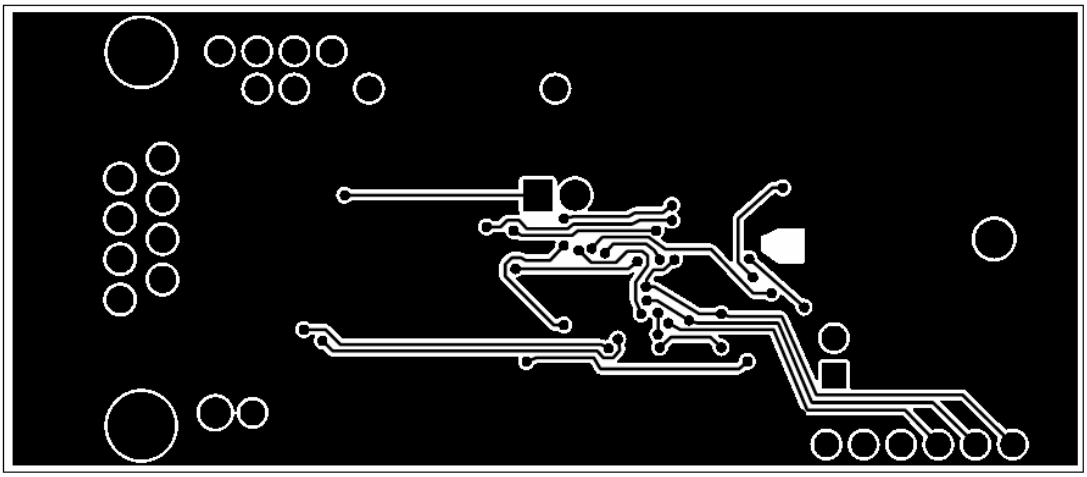


Top



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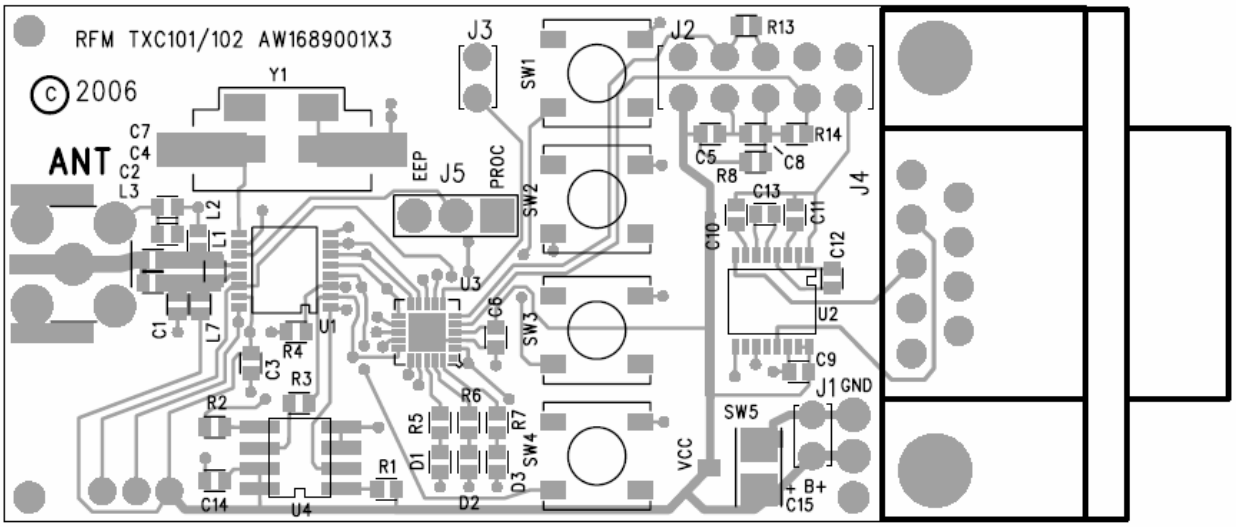

Top Assembly

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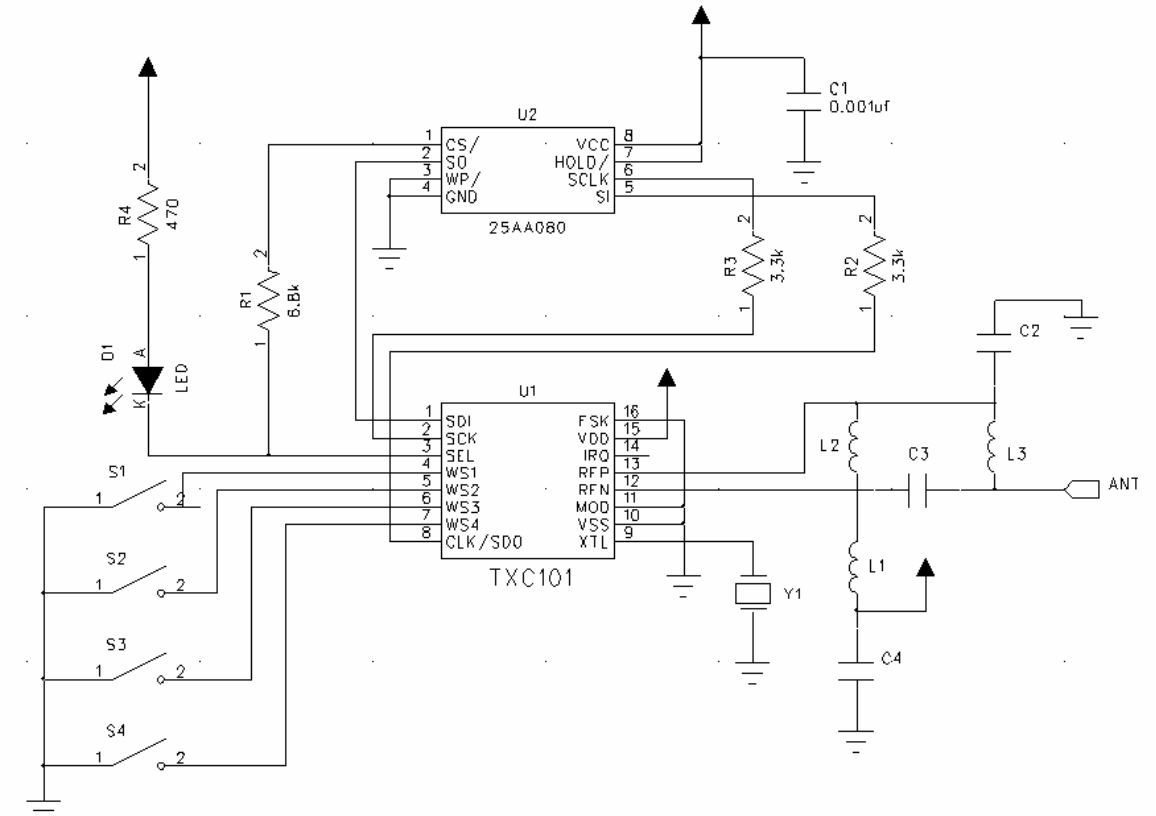
2.2 EEPROM Mode

Figure 2. Typical EEPROM Mode Application Circuit for 50 Ohm Load



The TXC101 can operate from a single, SPI compatible EEPROM by simply reading the sequential codes stored in memory. No external microcontroller is required. The codes are read out and processed as command and data. In this special mode, four pins are configured as inputs with an internal pull-up resistor. All that is needed are external key switches connected to GND to activate that key's code routine. When the key is pressed, the chip automatically begins executing code from a designated point within the EEPROM. When not in use, the last command of the code execution should be a sleep command so as to power down the device for maximum battery life. When the device is put into sleep one of the following seven (7) events can cause the device to wake up:

- Power-on Reset
- Low pulse on Key 1
- Low pulse on Key 2
- Low pulse on Key 3
- Low pulse on Key 4
- Low supply voltage output warning
- Wake-up timer timeout

For each wake-up event there is an internal address assigned as the starting point in EEPROM memory to begin executing code. These are defined in TABLE 3 as follows:

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TABLE 3.

Wake-up Event	EEPROM Address Entry
Power up	0000h
Low Pulse on SW1	0080h
Low Pulse on SW2	0100h
Low Pulse on SW3	0180h
Low Pulse on SW4	0200h
LBD Warning	0280h
Wake-up Timer Timeout	0300h

Another feature allows the use of two keys being pressed at the same time. For this, Bit7 in the *Button Command Register* controls whether SW4 is used as a single key press or SW1 and SW2 are used as simultaneous key presses. By setting Bit7 of the *Button Command Register,* the EEPROM Address Entry point of SW4 is used for simultaneous presses of SW1 and SW2. Clearing Bit7 sets the EEPROM to use SW4 as a single key press. It is also possible to detect multiple key presses and execute sequential routines. When multiple keys are pressed, all routines associated with the keys are executed in the same sequence of which the keys were pressed.

When a key is pressed, the chip looks to see if there is a debounce time to recognize before sampling the pin again. At this time the oscillator is turned on, independent of the state of Bit 5 of the *Power Management Register*, because it uses the crystal oscillator signal as a timing reference. After the debounce time has expired, it begins execution of the code from the EEPROM address entry point.

All sources used to transmit are internal when using EEPROM mode. All external pin functions, such as external FSK modulation, are disabled and the internal functions are used. During sleep mode, all internal configurations are maintained as long as power is not interrupted. If there is a supply interruption the chip reboots from the Power-up EEPROM Address Entry point and all configurations are re-written.

Example EEPROM Hex Code Contents:

Power-On Reset:

00000000	C0	C4	CA	1E	C8	23	C4	64	00	00	00	00	00	00	00	00
00000010	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000020	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000030	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000040	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000050	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000060	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

The example above configures the initial settings of the registers at power-up. Other parameters may be changed as needed when the chip recognizes a key press. The code ends in a sleep command C400h where 00h is the number of clocks to output before disabling the clock output pin. See *Sleep/Clock Command Register*.

Address	Command	Data	Related Register	Description
00–01	C0	C4	Power Management	Crystal– Synthesizer – Power Amplifier auto on/off mode enable
02–03	CA	1E	Button Command	Continuous execution for all keys
04–05	C8	23	Data Rate	DR=10M/29/(35+1)~9600 bps
06-07	C4	64	Sleep	Power down after 64h (100) clocks

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Example Code for Key Press 3:

00000180	88	72	A6	10	C6	60	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
00000190	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
000001A0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
000001B0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
000001C0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
000001D0	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA	AA
000001E0	AA	AA	AA	AA	AA	AA	C4	00	00	00	00	00	00	00	00	00
000001F0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

In the above example, some commands are one nibble long. For purposes of writing to the EEPROM the data must be arranged in bytes. The chip automatically distinguishes between command and data. On power-up, the keys are configured as a single execution. Hence, after this routine is executed, the chip returns to sleep and wakes up on another key press. If the keys were configured as a continuous execution, at the end of the sleep command, the chip restarts at address 0180h and re-executes the routine until the key is released.

Address	Command	Data	Related Register	Remarks
180–181	8	872	Configuration Control	433MHz band, FSK dev=90kHz, Crystal CL=12pF
182–183	A	610	Frequency	fc=(43+1552/4000)*10MHz [433.92MHz]
184–185	C6	60	Data Transmit	Transmit the next 96 bytes
186–1E5		96xAAh		Data
1E6–1E7	C4	00	Sleep	Power down immediately (no clocks)

3.0 TXC101 Functional Characteristics

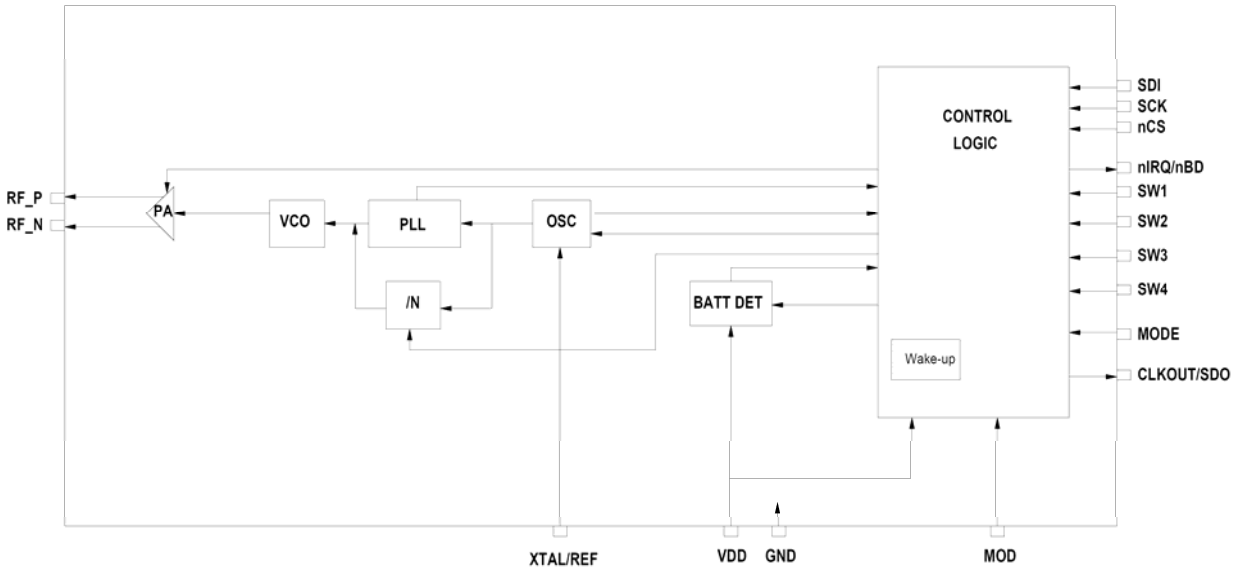

Figure 3. Functional Block Diagram

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Output Power Amplifier

The power amplifier is an open-collector, differential output with programmable output power which can directly drive a loop or dipole antenna, and with proper matching may also drive a monopole antenna. Incorporated in the power amplifier is an automatic antenna tuning circuit to avoid manual tuning during production and to offset “hand effects”. Registers common to the Power Amplifier are:

- *Power Management Register*
- *Transmit Power Configuration Register*

Phase Lock Loop (PLL)

The PLL synthesizer is the heart of the operating frequency. It is programmable and completely integrated, providing all functions required to generate the carriers and tunability for each band. The PLL requires only a single 10MHz crystal reference source. RF stability is controlled by choosing a crystal with the particular specifications to satisfy the application.

The PLL is able to perform manual and automatic calibration to compensate for changes in temperature or operating voltage. When changing band frequencies, re-calibration must be performed. This can be done by disabling the synthesizer and re-enabling again through the *Power Management Register*. Registers common to the PLL are:

- *Power Management Register*
- *Configuration Register*
- *Frequency Setting Register*
- *Transmit Configuration Register*

Transmit Register

The transmit register is configured as two 8-bit shift registers connected in series to form a single 16-bit shift register. This register is a master when in EEPROM Mode. The TXC101 generates the chip select and clock to read the EEPROM contents into the register.

For Microcontroller Mode, this register is not available. Data may be applied in two ways: directly to the FSK MOD pin (16) after enabling the oscillator, synthesizer, and power amplifier, or directly to the SDI pin following the clock timing on page 19 of the *Transmit Command Register*.

Crystal Oscillator

The TXC101 incorporates an internal crystal oscillator circuit that provides a 10MHz reference, as well as internal load capacitors. This significantly reduces the component count required. The internal load capacitance is programmable from 8.5pF to 16pF in 0.5pF steps. This has the advantage of accepting a wide range of crystals from many different manufacturers having different load capacitance requirements. Since the crystal is the PLL reference for the carrier, being able to vary the load capacitance also helps with fine tuning the final carrier frequency

An external clock signal is also provided that may be used to run an external processor. This also has the advantage of reducing component count by eliminating an additional crystal for the host processor. The clock frequency is also programmable from eight pre-defined frequencies, each a pre-scaled value of the 10MHz crystal reference. These values are programmable through the *Battery Detect Threshold and Clock Output Register.* The internal clock oscillator may be disabled, thus also disabling the output clock signal to the host processor. When the oscillator is disabled, the chip provides an additional 196 clock cycles before releasing the output, which may be used by the host processor to setup any functions before going to sleep.

Sleep Mode

The TXC101 draws very little current when in sleep mode (200nA typical). See the *Power Management Register* and *Sleep/Clock Command Register* definitions on how to program the TXC101 into full sleep mode.

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Wake-Up Mode

The TXC101 has an internal wake-up timer that has very low current consumption (1.5uA typical) and may be programmed from 1msec to several days. A calibration is performed to the crystal at startup and every 30 sec thereafter, even if in sleep mode. If the oscillator circuit is disabled the calibration circuit will turn it on briefly to perform a calibration to maintain accurate timing and return to sleep.
The TXC101 also incorporates other power saving modes aside from the wake-up timer. Return to active mode may be initiated from several external events:

- Logic '0' applied to nINT pin (16)
- Low Supply Voltage Detect
- FIFO Fill
- SPI request

If any of these wake-up events occur, including the wake-up timer, the TXC101 generates an external interrupt which may be used as a wake-up signal to a host processor. The source of the interrupt may be read out from the *Status Register* over the SPI bus. To re-enter wake-up mode the WKUPEN bit (1) of the *Power Management Register* must be cleared then set.

Low Battery Detect

The integrated low battery detector monitors the voltage supply against a preprogrammed value and generates an interrupt when the supply voltage falls below the programmed value. The detector circuit has 50mV of hysteresis built in.

Key Switch Inputs

In microcontroller mode, the TXC101 generates an interrupt on the nIRQ pin when a key is pressed. The source of the interrupt may be determined by reading the *Status Register*. In EEPROM mode, each switch has an internal address assigned to it. It uses this address as the entry point to the EEPROM and executes commands after that address until it sees a sleep command (C400h). The chip has internal weak pull-up resistors so there is no need for additional components. These weak pull-ups may be disabled through the *Button Command Register.* For each mode the chip repeats this function while the key is pressed if configured by the *Button Command Register*. In the microcontroller mode, the chip continuously generates interrupts until the key is released. In the EEPROM mode, the chip continuously enters the EEPROM at the assigned address and executes the commands following the entry point as long as the key is active, if enabled through the *Button Command Register*. There are seven defined entry points for the EEPROM mode. The chip also has an integrated, programmable de-bounce circuit for each key. See *Button Command Register* for a detailed explanation.

SPI Interface

The TXC101 is equipped with a standard SPI bus that is compatible to almost all SPI devices. All functions and status of the chip are accessible through the SPI bus. Typical SPI devices are configured for byte write operations. The TXC101 uses word writes and hence the nCS (Pin 3) should be pulled low for 16 bits. All SPI data is written to the TXC101 MSB first. The maximum SCK for the SPI bus is 20 MHz.

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TABLE 4.

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10
t_{BL}	Push-button input low time	25

Timing Diagram

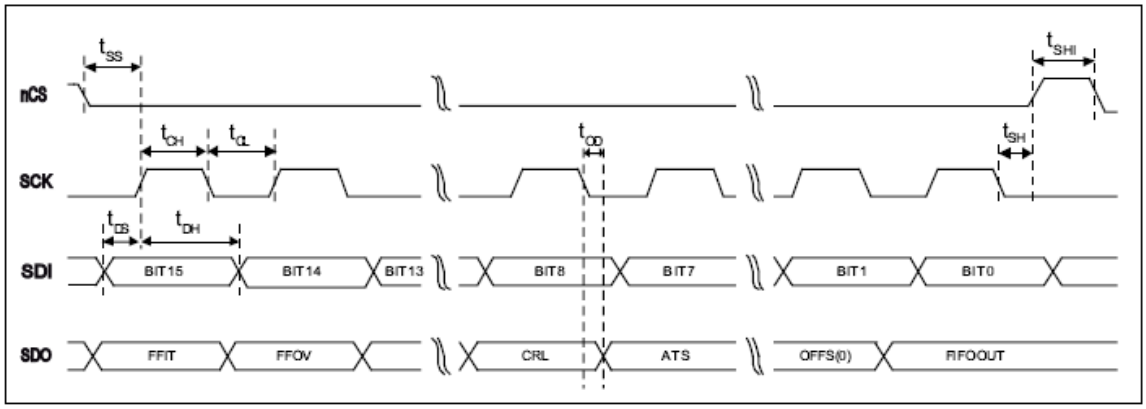

Figure 4. Timing Diagram

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4.0 Control and Configuration Registers

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
STATUS	X	X	X	X	X	X	X	X	1	1	0	0	1	1	0	0	- -
CONFIG	1	0	0	BAND1	BAND0	CLK2	CLK1	CLK0	CAP3	CAP2	CAP1	CAP0	MODP	DEV2	DEV1	DEV0	8080h
TX POWER CONFIG	X	X	X	X	X	X	X	X	1	0	1	1	OOKEN	PWR2	PWR1	PWR0	XXB0h
TX COMMAND REG	1	1	0	0	0	1	1	0	B7	B6	B5	B4	B3	B2	B1	B0	- -
FREQ SET	1	0	1	0	Freq11	Freq10	Freq9	Freq8	Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0	A7DOh
DATA RATE SET	1	1	0	0	1	0	0	0	BITR7	BITR6	BITR5	BITR4	BITR3	BITR2	BITR1	BITR0	C800h
BUTTON CMD	1	1	0	0	1	0	1	0	2KPEN	DB1	DB0	SW4	SW3	SW2	SW1	PUPDIS	CA00h
SLEEP/CLK CMD	1	1	0	0	0	1	0	0	SLP7	SLP6	SLP5	SLP4	SLP3	SLP2	SLP1	SLP0	C400h
WAKE-UP PERIOD	1	1	1	R4	R3	R2	R1	R0	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0	E000h
BATT DETECT	1	1	0	0	0	0	1	0	0	0	0	LBD4	LBD3	LBD2	LBD1	LBD0	C200h
POWER MANAGEMENT	1	1	0	0	0	0	0	0	TX1	TX0	OSCEN	SYNEN	PAEN	LBDEN	WKUPEN	CLKEN	C000h

x-Not Used

Table 5. Control and Configuration Registers Table

Status Register (**Read Only**)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	1	1	0	0

The Status Register provides feedback for:

- POR
- Interrupt Request state
- Low Battery
- Push Button event

The Status Register requires only the Command Code to be sent. Status bits can be read through the nIRQ pin (14). Clock pulses are continually sent and data is read out. When this command is issued it clears the last interrupt and starts processing the next pending interrupt. See Figure 5 for read sequence.

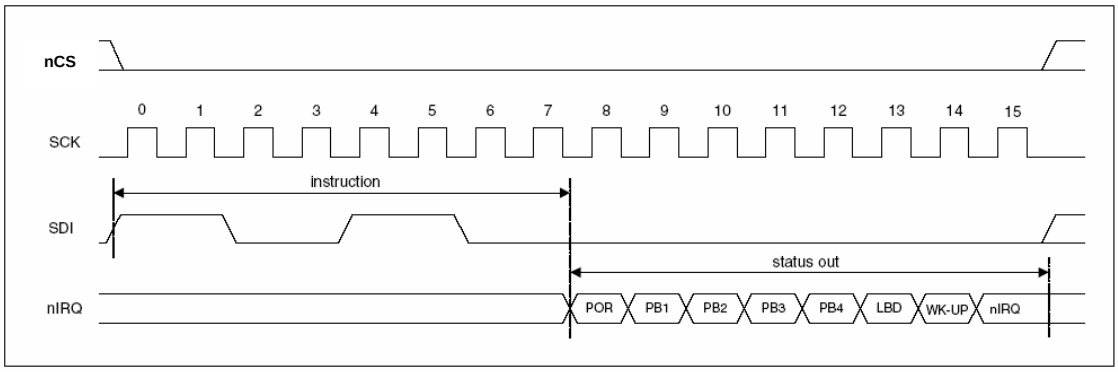

Figure 5. Status Register Read Through nIRQ (pin 14 Processor Mode)

Bit [7..0]: **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Status Register.

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Configuration Register [POR=8080h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	BAND1	BAND0	CLK2	CLK1	CLK0	CAP3	CAP2	CAP1	CAP0	MODP	DEV2	DEV1	DEV0

The configuration register sets up the following:

- Frequency Band in use
- Crystal Load capacitance
- TX Modulation Polarity
- TX Modulation Bandwidth

Bit [15..13] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the configuration register.

Bit [12..11] – **Band Select:** These bits set the frequency band to be used. There are four (4) bands that are supported. See Table 6 for Band configuration.

TABLE 6.

Frequency Band	BAND1	BAND0
315	0	0
433	0	1
868	1	0
916	1	1

Bit [10..8] – **Clock Output Frequency:** These bits set the output frequency of the on-board clock that may be used to run an external host processor. See Table 7.

TABLE 7.

Output Clock Frequency (MHz)	CLK2	CLK1	CLK0
1	0	0	0
1.25	0	0	1
1.66	0	1	0
2	0	1	1
2.5	1	0	0
3.33	1	0	1
5	1	1	0
10	1	1	1

Bit [7..4] – **Load Capacitance Select:** These bits set the load capacitance for the crystal reference. The internal load capacitance can be varied from 8.5pF to 16pF in 0.5pF steps to accommodate a wide range of crystal vendors and also to adjust the reference frequency and compensate for stray capacitance that may be introduced due to PCB layout. See Table 8 for load capacitance configuration.

TABLE 8.

CAP3	CAP2	CAP1	CAP0	Crystal Load Capacitance
0	0	0	0	8.5
0	0	0	1	9
0	0	1	0	9.5
0	0	1	1	10
	……			……
1	1	1	0	15.5
1	1	1	1	16

$$C_L = 8.5pF + (CAP[3..0] * 0.5pF)$$

Bit [3] - **Modulation Polarity:** When clear, a logic ‘0’ is defined as the lower channel frequency and a logic ‘1’ as the higher channel frequency (positive deviation). When set, a logic ‘0’ is defined as the higher channel frequency and a logic ‘1’ as the lower channel frequency (negative deviation).

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Configuration Register – continued

Bit [2..0] - **Modulation Bandwidth:** These bits set the FSK frequency deviation for transmitting a logic '1' and logic '0'. The deviation is programmable from 30kHz to 210kHz in 30kHz steps. See Table 9 for deviation settings.

TABLE 9.

Modulation Bandwidth	HEX	DEV2	DEV1	DEV0
30 kHz	00	0	0	0
60 kHz	01	0	0	1
90 kHz	02	0	1	0
120 kHz	03	0	1	1
150 kHz	04	1	0	0
180 kHz	05	1	0	1
210 kHz	06	1	1	0
Not used	07	1	1	1

Transmit Power Configuration Register [POR=B0h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
7	6	5	4	3	2	1	0
1	0	1	1	OOKEN	PWR2	PWR1	PWR0

The Power Configuration Register configures the output transmit power desired.

Bit [7..4] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Transmit Power Configuration Register.

Bit [3] – **OOKEN:** This bit enables OOK mode for the power amplifier. In this mode, data is applied to the MOD pin (16). When a logic '1' is applied, the power amplifier is On. When a logic '0' is applied, the power amplifier is Off.

Bit [2..0] – **Output Transmit Power:** These bits set the transmit output power. The output power is programmable from Max to -21dB in -3dB steps. See Table 10 for Output Power settings.

TABLE 10.

Output Power (Relative)	PWR2	PWR1	PWR0
Max	0	0	0
-3dB	0	0	1
-6dB	0	1	0
-9dB	0	1	1
-12dB	1	0	0
-15dB	1	0	1
-18dB	1	1	0
-21dB	1	1	1

Transmit Command Register [POR=C600h]

(EEPROM Mode)

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	1	0	B7	B6	B5	B4	B3	B2	B1	B0

(Processor Mode)

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
7	6	5	4	3	2	1	0
1	1	0	0	0	1	1	0

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The Transmit Command Register in EEPROM mode holds the count of the number of data bytes to follow. In processor mode, only the command code is sent and the data is applied to the SDI pin **WITHOUT** a clock. If clock pulses are sent, the data will be interpreted as commands. In this mode the SDI pin acts like the MOD input pin (16). See Figure 6.

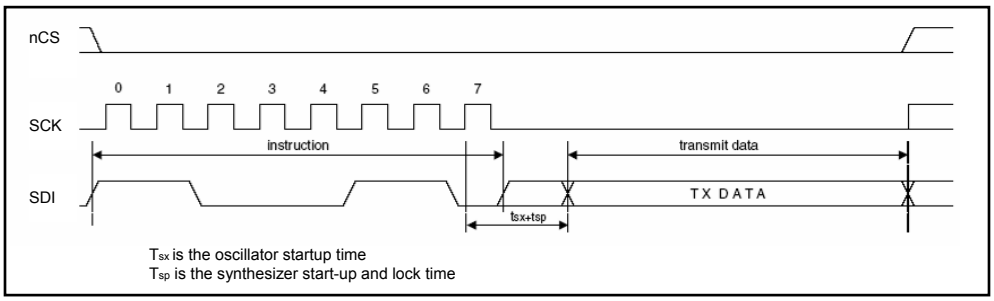

Figure 6. Data Transmit through SDI pin

The MOD pin(16) may also be used to manually send modulated data. The Oscillator and Synthesizer must manually be enabled through the *Power Management Register.* Startup and settle time must be allowed before applying a modulating signal to the MOD pin(16).

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Transmit Command Register.

Bit [7..0] – **Byte Count** (EEPROM Mode Only)**:** These bits are the 8-bit value of the number of data bytes to be transmitted. Before issuing this command the power amplifier must be enabled either by setting the respective *Power Management Register* bits PAEN bit (3) or TX0 bit (6).

Bit [7..0] - **Command Code** (Processor Mode Only)**:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Transmit Command Register.

Note: When manually controlling the oscillator and synthesizer turn-on, valid data can only be transmitted when the oscillator has had time to start-up and the synthesizer has had time to lock.

Data may also be sent through the FSK pin (16). When the Transmit Command is issued the Osc and Synthesizer are automatically enabled. If the Osc and Synthesizer are not running, there must be a delay before sending out the first bit in order to allow the Osc to stabilize and the Synthesizer to lock. See Figure 7 timing below.

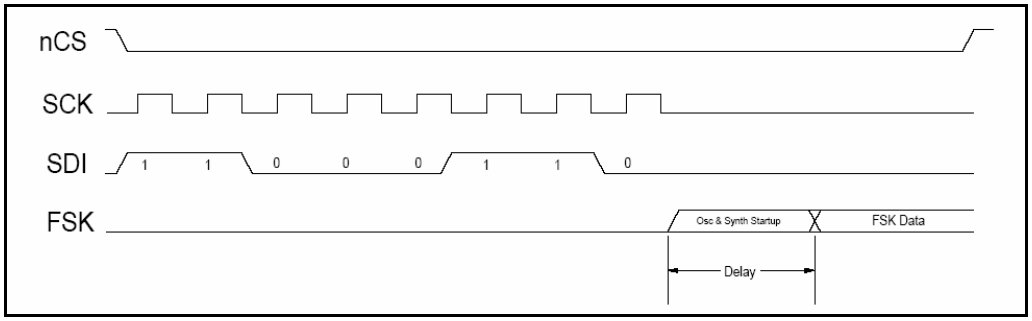

Figure 7. Data Transmit through FSK pin

Frequency Setting Register [POR=A7D0h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	Freq11	Freq10	Freq9	Freq8	Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0

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The Frequency Setting Register sets the exact frequency within the selected band for transmit or receive. Each band has a range of frequencies available for channelization or frequency hopping. The selectable frequencies for each band are:

Frequency Band	Min (MHz)	Max (MHz)	Tuning Resolution
300 MHz	310.24	319.75	2.5 kHz
400 MHz	430.24	439.75	2.5 kHz
800 MHz	860.48	879.51	5.0 kHz
900 MHz	900.72	929.27	7.5 kHz

Bit descriptions are as follows:

Bit [15..12] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the *Frequency Setting Register*.

Bit [11..0] – **Frequency Setting:** These bits set the center frequency to be used during transmit or receive. The value of bits[11..0] must be in the decimal range of 96 to 3903. Any value outside of this range will cause the previous value to be kept and no frequency change will occur. To calculate the center frequency f_c, use Table 11 and the following equation:

$$f_c = 10 * B1 * (B0 + f_{VAL}/4000) \text{ MHz}$$

where f_{VAL} = decimal value of Freq[11..0] = $96<f_{VAL}<3903$.

Use Table 11 to select the frequency band and substitute into the above equation to calculate the center frequency of the desired band.

TABLE 11.

Range	B1	B0
315 MHz	1	31
433 MHz	1	43
868 MHz	2	43
916 MHz	3	30

Data Rate Setup Register [POR=C800h] [**EEPROM Mode ONLY**]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	BITR7	BITR6	BITR5	BITR4	BITR3	BITR2	BITR1	BITR0

The *Data Rate Setup Register* configures the effective transmit data rate for the transmitter.

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Data Rate Setup Register.

Bit [7..0] – **Data Rate Parameter Value:** These bits represent the decimal value of the 8-bit parameter used to calculate the expected data rate. The definable data rates range from 1.346kpbs to 344.828kbps. To calculate the expected data rate, use the following formula:

$$DRexp(kbps) = 10000 / [29 * (BITR[7..0]+1)]$$

where BITR[7..0] is the decimal value 0 to 255.

To calculate the BITR[7..0] decimal value for a given bit rate, use the following formula:

$$BITR[7..0] = (10000 / [29 * DR_{exp}]) - 1$$

where DR_{exp} is the expected data rate.

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TABLE 12. Conversion for Common Data Rates

Hex Value	Common Data Rate (bps)
0x8E	2400
0x47	4800
0x23	9600
0x19	13200
0x17	14400
0x11	19200
0x0B	28800
0x02	115200

Button Command Register [POR=CA00h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	1	0	2KPEN	DB1	DB0	SW4	SW3	SW2	SW1	PUPDIS

The Button Command Register configures:

- Key press de-bounce time
- Key press events
- Weak Pull-ups

Bit [15..8] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Button Command Register.

Bit [7] – **2-Key Press Enable:** This bit enables simultaneous key press of SW1 and SW2 to execute the same address entry point as SW4. Enabling this bit does **NOT** disable SW4 function.

Bit [6..5] – **De-Bounce Time Set:** These bits set the key press de-bounce time. See Table 13 for settings.

TABLE 13.

DB1	DB0	De-Bounce Time
0	0	160msec
0	1	40msec
1	0	10msec
1	1	NONE

Bit [4] – **SW4 Continuous Execute Enable:** This bit, when set, enables the chip to continuously execute the routine as long as the key is pressed.

Bit [3] – **SW3 Continuous Execute Enable:** This bit, when set, enables the chip to continuously execute the routine as long as the key is pressed.

Bit [2] – **SW2 Continuous Execute Enable:** This bit, when set, enables the chip to continuously execute the routine as long as the key is pressed.

Bit [1] – **SW1 Continuous Execute Enable:** This bit, when set, enables the chip to continuously execute the routine as long as the key is pressed.

Bit [0] – **Weak Internal Pull-ups:** This bit DISABLES the internal weak pull-up resistors for all keys when set. This bit defaults to clear so that the weak pull-ups are enabled.

Sleep/Clock Command Register [POR=C400h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	0	0	SLP7	SLP6	SLP5	SLP4	SLP3	SLP2	SLP1	SLP0

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The Sleep Command Register defines the byte command and the number of clock cycles to generate after a sleep instruction to put the chip into sleep mode. When the chip sees this command issued, it immediately disables the power amplifier, turns off the synthesizer, and turns off the oscillator after SLP[7..0] (0-256) clock cycles.

Bit [15..8] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Sleep Command Register.

Bit [7..0] – **Sleep Command Value:** These bits define the number of clock cycles to generate before disabling the oscillator and before the chip goes into sleep mode. This allows time for an external processor to perform any memory or pre-sleep functions before the clock is stopped and the device enters sleep mode.

Wake-up Timer Period Register [POR=E000h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	R4	R3	R2	R1	R0	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0

The Wake-up Timer Period register sets the wake-up interval for the TXC101. After setting the wake-up interval, the WKUPEN (bit 1 of Power Management Register) should be cleared and set at the end of every wake-up cycle. To calculate the wake-up interval desired, use the following:

$$T_{WAKE} = MUL[7..0] * 2^{R[4..0]}$$

where MUL[7..0] = decimal value 0 to 255 and R[4..0] = decimal value 0 to 31.

Bit [15..13] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Wake-up Timer Period register.

Bit [12..8] – **Exponential:** These bits define the exponential value as used in the above equation. The value used must be the decimal equivalent between 0 and 31.

Bit [7..0] – **Multiplier:** These bits define the multiplier value as used in the above equation. The value used must be the decimal equivalent between 0 and 255.

Battery Detect Threshold Register [POR=C200h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	1	0	0	0	0	LBD4	LBD3	LBD2	LBD1	LBD0

The Battery Detect Threshold and Clock Output Register configures the following:

- Low Battery Detect Threshold

The Low Battery Threshold is programmable from 2.2V to 5.3V using the following equation:

$$VT = (LBD[4..0] / 10) + 2.2 \text{ (V)}$$

where LBD[4..0] is the decimal value 0 to 31.

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Battery Detect Threshold Register.

Bit [7..5] – Not Used. Write a logic '0'.

Bit [4..0] – **Low Battery Detect Value:** These bits set the decimal value as used in the equation above to calculate the battery detect threshold voltage value. When the battery level falls 50mV below this value, the LBD bit (5) in the status register is set indicating that the battery level is below the programmed threshold. This is useful in monitoring discharge sensitive batteries such as Lithium cells.

The Low Battery Detect can be enabled by setting the LBDEN bit (2) of the *Power Management Register* and disabled by clearing the bit.

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Power Management Register [POR=C000h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	TX1	TX0	OSCEN	SYNEN	PAEN	LBDEN	WKUPEN	CLKEN

The Power Management Register enables/disables the following:

- Transmit Chain
- PLL
- Power Amplifier
- Synthesizer
- Crystal Oscillator
- Low battery Detect Circuit
- Wake-up Timer
- Clock Output

Bit [15..8] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Power Management register.

Bit [7..6] – **Transmit Chain Automatic Enable [EEPROM Mode]:** These bits enable the entire transmit chain when set. When TX1 is set, the oscillator and synthesizer turn-on are controlled by the chip. When the *Data Transmit Command* is issued, the oscillator is enabled. As soon as a stable frequency is reached the synthesizer is enabled. When TX0 is set, this turns on the power amplifier after the PLL has successfully achieved lock.

Function	TX1	TX0
Manual	0	0
PA on after synth locked	0	1
Osc and Synth on when Transmit Cmd issued	1	0
Osc and Synth on after Transmit Cmd, then PA on after synth locked	1	1

Bit [5] – **Crystal Oscillator Enable:** This bit enables the oscillator circuit when set. The oscillator provides the reference signal for the synthesizer when setting the transmit frequency of use.

Bit [4] – **Synthesizer Enable:** This bit enables the synthesizer when set. The synthesizer contains the PLL, oscillator, and VCO for controlling the channel frequency. This must be enabled when the transmitter is enabled. The oscillator also must be enabled to provide the reference frequency for the PLL. On power-up the synthesizer performs a calibration automatically. If there are significant changes in voltage or temperature, recalibration can be performed by simply disabling the synthesizer and re-enabling it.

NOTE: For correct operation of the frequency synthesizer, the frequency and band of operation need to be programmed before the synthesizer is started. Directly after activation of the synthesizer, the RF VCO is calibrated to ensure proper operation in the programmed frequency band. It is suggested that recalibration routines be added to compensate for significant changes in temperature and supply voltages.

Bit [3] –**Power Amplifier Enable:** This bit enables the power amplifier when set. The power amplifier may be manually enabled from other functions.

Bit [2] – **Low Battery Detector:** This bit enables the battery voltage detect circuit when set. The battery detector can be programmed to 32 different threshold levels. See *Battery Detect Threshold and Clock Output Register* section for programming.

Bit [1] – **Wake-up Timer Enable:** This bit enables the wake-up timer when set. See *Wake-up Timer Period Register* section for programming the wake-up timer interval value.

Bit [0] – **Clock Output Disable:** This bit disables the oscillator clock output when set. On chip reset or power up, clock output is on so that a processor may begin execution of any special setup sequences as required by the designer. See *Battery Detect Threshold and Clock Output Register* section for programming details.

Sleep Mode

The device enters sleep mode by writing a 0xC001 which disables all functions and turns off the clock output. If the clock output is not disabled by writing a '1' to bit 0, the oscillator circuit will continue to run and draw additional current.

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5.0 Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	Notes	Min	Max	Units
VDD	Positive supply voltage		-0.5	6	V
V_{in}	Voltage on any pin (except RF_P and RF_N)		-0.5	Vdd+0.5	V
Voc	Voltage on open collector outputs (RF1, RF2)	1	-0.5	6	V
I_{in}	Input current into any pin except VDD and VSS		-25	25	mA
ESD	Electrostatic discharge with human body model			1000	V
T_{stg}	Storage temperature		-55	125	°C
T_{lead}	Lead temperature (soldering, max 10 s)			260	°C

Note 1: At maximum, VDD+1.5 V cannot be higher than 7 V.

Recommended Operation Ratings

Symbol	Parameter	Notes	Min	Max	Units
VDD	Positive supply voltage		2.2	5.4	V
VDC_{RF}	DC voltage on open collector outputs (RF1, RF2)	1,2	Vdd-1	Vdd+1	V
T_{op}	Ambient operating temperature		-40	85	°C

Note 1: At minimum, VDD - 1.5 V cannot be lower than 1.2 V.
Note 2: At maximum, VDD+1.5 V cannot be higher than 5.5 V.

6.0 DC Electrical Characteristics

(Min/max values are valid over the whole recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Digital I/O	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			Min	typ	max		
Supply current (TX mode, Pout = Pmax, into 50 Ohm Load)	Idd_{TX}			10	12	mA	315MHz Band
				10	12		433MHz Band
				12	14		868MHz Band
				13	15		916MHz Band
Sleep current	I_S			0.2		µA	All blocks disabled
Idle current	I_{IDLE}			1.5		mA	Oscillator and baseband enabled
Low battery voltage detector current consumption	I_{VD}			0.5		µA	
Wake-up timer current consumption	I_{WUT}			1.5		µA	
Low battery detect threshold	Vlb		2.2		5.3	V	Programmable in 0.1 V steps
Low battery detection accuracy				±75		mV	
Digital input low level	Vil				0.3*Vdd	V	
Digital input high level	Vih		0.7*Vdd			V	
Digital input current low	Iil		-1		1	µA	Vil = 0 V
Digital input current high	Iih		-1		1	µA	Vih = Vdd, Vdd = 5.4 V
Digital output low level	Vol				0.4	V	Iol = 2 mA
Digital output high level	Voh		Vdd-0.4			V	Ioh = -2 mA
Digital input capacitance					2	pF	
Digital output rise/fall time					10	ns	Load = 15 pF

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7.0 AC Electrical Characteristics

(Min/max values are valid over the whole recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Transmitter	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			**min**	**typ**	**max**		
Open collector output DC current			0.1		2.5	mA	Programmable
Output power (Differential Load)	P_{DL}			+3		dBm	315MHz Band
				+3			433 MHz Band
				+1			868 MHz Band
				+1			916 MHz Band
Output power (into 50 Ohms)	P_O			0		dBm	315MHz Band
				-1			433 MHz Band
				-4			868 MHz Band
				-4			916 MHz Band
Reference Spur				-60		dBm	315MHz Band
				-65			433MHz Band
				-65			868MHz Band
				-65			916MHz Band
2nd Harmonics				-35		dBm	315MHz Band
				-35			433MHz Band
				-40			868MHz Band
				-45			916MHz Band
3rd Harmonics				-35		dBm	315MHz Band
				-35			433MHz Band
				-50			868MHz Band
				-55			916MHz Band
Antenna tuning capacitance			1.5	2.3	3.1	pF	315MHz Band
							433MHz Band
			1.6	2.2	2.8		868MHz Band
							916MHz Band
Output capacitance Quality factor			16	18	22		315MHz Band
							433MHz Band
							868MHz Band
							916MHz Band
Phase noise				-75		dBc/Hz	100 kHz from carrier
				-85			1 MHz from carrier
FSK bit rate					256	kbps	ΔFSK = 210kHz
OOK bit rate					512	kbps	
FSK frequency deviation			30		210	kHz	Programmable in 30 kHz steps

Timing	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			**min**	**Typ**	**max**		
Internal POR timeout					100	ms	Vdd at 90% of final value
Wake-up timer period				1		ms	Calibrated every 30 seconds
Wake-up Time			1		2e+9	ms	

PLL Characteristics	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			**min**	**typ**	**max**		

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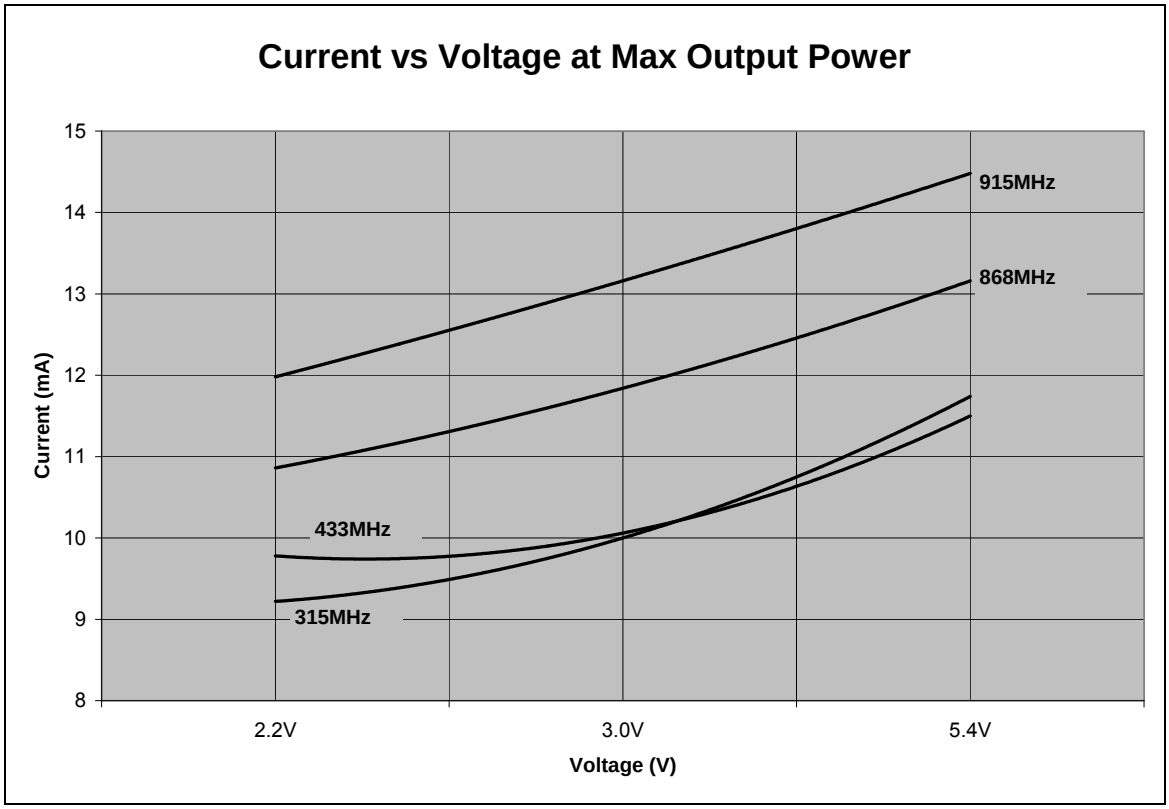
PLL reference freq			8	10	12	MHz	
PLL lock time				10		us	within 1kHz settle, 10MHz step
PLL startup time					250	us	Crystal running
Crystal load capacitance	CL		8.5		16	pF	Programmable in 0.5 pF steps, tolerance +/- 10%
Xtal oscillator startup time				1.25	5	ms	Crystal ESR < 100
Tuning Range (w/ 10MHz ref xtal)			310.24		319.75	MHz	315MHz Band (2.5kHz steps)
			430.24		439.75		433MHz Band (2.5kHz steps)
			860.48		879.51		868MHz Band (5.0kHz steps)
			900.72		929.27		916MHz Band (7.5kHz steps)

8.0 Transmitter Measurement Results



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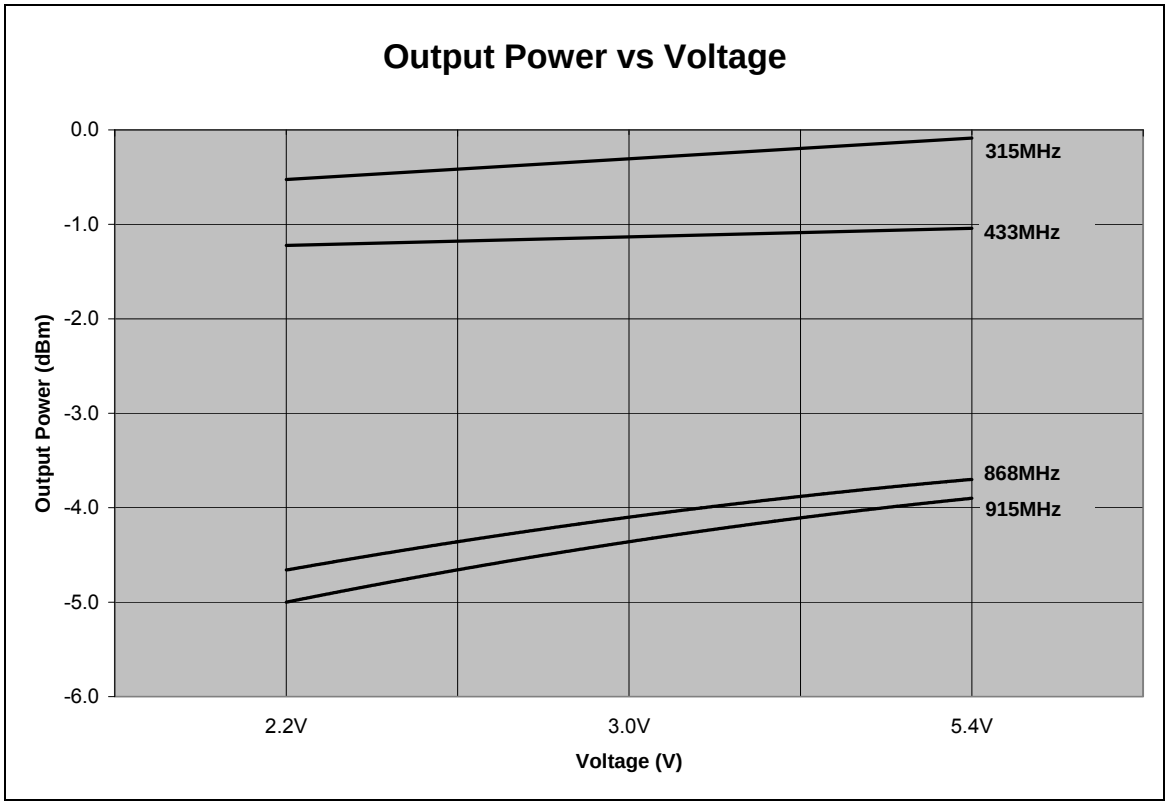

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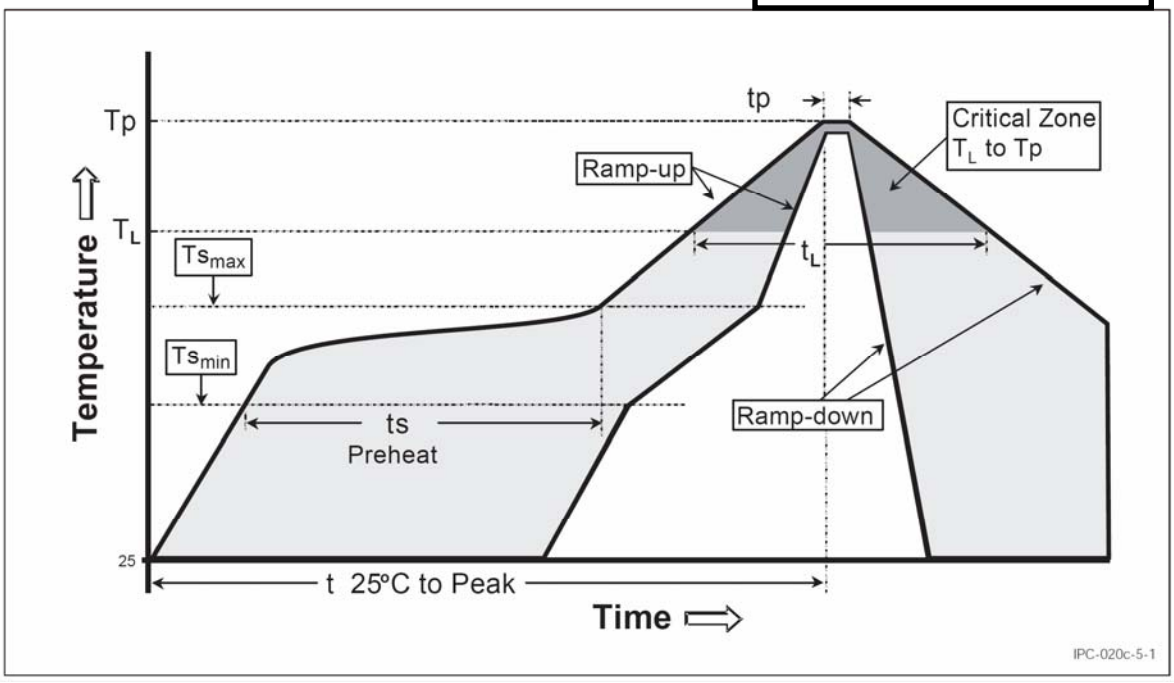
IPC/JEDEC J-STD-020C REFLOW PROFILE

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



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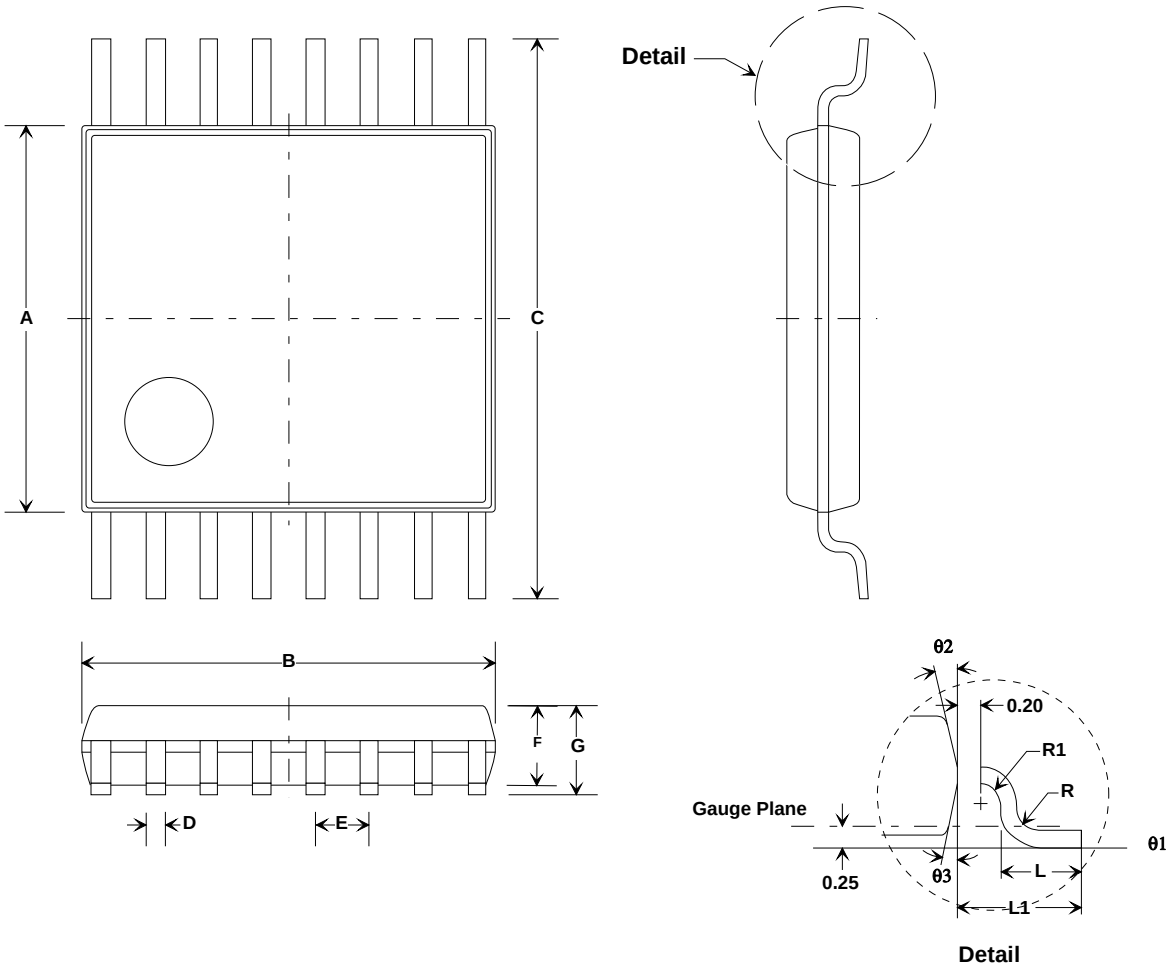
9.0 Package Dimensions – 6.4x5mm 16-pin TSSOP Package

(all values in mm)



Symbol	Dimensions in mm			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.30	4.40	4.50	0.169	0.173	0.177
B	4.90	5.00	5.10	0.193	0.197	0.201
C		6.40 BSC.			0.252 BSC.	
D	0.19		0.30	0.007		0.012
E		0.65 BSC.			0.026 BSC.	
F	0.80	0.90	1.05	0.031	0.035	0.041
G			1.20			0.47
L	0.50	0.60	0.75	0.020	0.024	0.030
L1		1.00 REF.			0.39 REF	
R	0.09			0.004		
R1	0.09			0.004		
θ1	0		8	0		8
θ2		12 REF.			12 REF.	
θ3		12 REF.			12 REF.	

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单击下面可查看定价，库存，交付和生命周期等信息

>>Murata(村田)

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