RXC101

300-1000 MHz Receiver

Complies with Directive 2002/95/EC (RoHS)

16-TSSOP package

Product Overview

RXC101 is a highly integrated single chip, zero-IF, multi-channel, low power, high data rate RF receiver designed to operate in the unlicensed 315/433/868/915 MHz frequency bands. All critical RF and baseband functions are completely integrated in the chip, thus minimizing external component count and simplifying design-ins. Its small size with low power consumption makes it ideal for various short range radio applications.

The RXC101 supports two modes – Microcontroller mode and Standalone mode. In the Micro controller mode, the use of a generic 10MHz crystal and a low-cost microcontroller is all that is needed to create a complete Receiver link. Simple short range radio applications can be supported by using the RXC101 in the Standalone mode, which allows complete receiver operation without the use of a microcontroller.

Key Features

- Modulation: FSK (Frequency Hopping Spread Spectrum capability)
- Limited OOK capability
- Operating frequency: 315/433/868/915 MHz
- High Sensitivity: (-112dBm)
- Low current consumption (RX current ~ 8mA)
- Wide Operating supply voltage: 2.2 to 5.4V
- Low standby current (0.1uA)
- FSK Data rate up to 256kbps
- Support for Multiple Channels
  - [315/433 Bands]: 95 Channels (100kHz)
  - [868 Band]: 190 Channels (100kHz)
  - [915 Band]: 285 Channels (100kHz)
- Generic 10MHz Xtal reference
- Processor or Standalone Operation Mode
- Automatic Frequency Alignment
- Programmable Analog/Digital Baseband Filter
- Programmable Data Rate
- Programmable Input LNA Gain
- Programmable Clock Output Frequency
- Programmable Wake-up Timer with programmable Duty Cycle
- Programmable Crystal Load Capacitance
- Programmable, Positive/Negative FSK Deviation
- Programmable Push Button Control
- Internal Valid Data Recognition
- Integrated PLL, IF & Baseband Circuitry
- Integrated Selectable Analog/Digital RSSI
- Integrated, Programmable Low Battery Voltage Detector
- Integrated Crystal Oscillator
- Integrated Clock Recovery
- Standard SPI interface
- External Wake-up Events
- External Processor Interrupt pin
- Receive FIFO or External Pin
- TTL/CMOS Compatible I/O pins
- No Manual Adjustment Needed for Production
- Very few external components requirement
- Small size plastic package: 16-pin TSSOP
- Standard 13 inch reel, 2000 pieces.

Popular applications

- Remote control applications
- Active RFID tags
- Wireless PC Peripherals
- Automated Meter reading
- Home & Industrial Automation
- Security systems
- Remote keyless entry
- Automobile Immobilizers
- Sports & Performance monitoring
- Wireless Toys
- Medical equipment
- Low power two way telemetry systems
- Wireless mesh sensors
- Wireless modules

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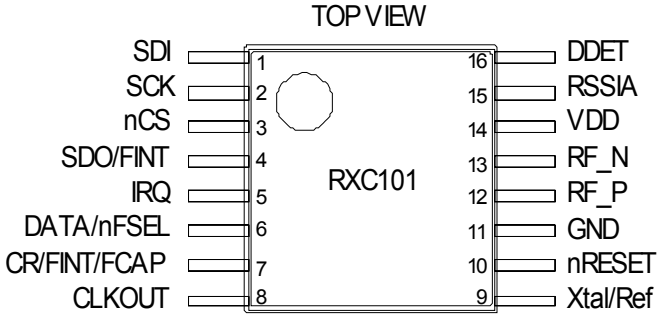
1. Pin Description

Processor Mode

Pin	Name	Description
1	SDI	**SPI Data In**
2	SCK	**SPI Data Clock**
3	nCS	**Chip Select Input**– Selects the chip for an SPI data transaction. The pin must be pulled 'low' for a 16-bit read or write function. See Figure 6 for timing specifications.
4	nFINT/SDO	**FIFO Interrupt Output (active low)** – When the internal FIFO is enabled (*Configuration Register,* Bit [6]), this pin acts as a FIFO Fill interrupt indicating that the FIFO has filled to its pre-programmed limit (*FIFO Configuration Register*, Bit [7..4]). **SPI Serial Data Out** – May be used to read out the *Status Register* contents.
5	nIRQ	**Interrupt Request Output** – Any of the following events will generate an external interrupt: -Wake-up timer timeout -Low Battery Detect -FIFO fill -FIFO overflow To determine the source of the interrupt, the processor may read the first four bits of the *Status Register*.
6	DATA/nFSEL	**Data Output** – Received data can be taken from this pin when the FIFO is not used. **FIFO Select Input** – When the FIFO is used this pin selects the FIFO when data is to be read out over the SDO pin.
7	DCLK/FCAP/ FINT	**Data Recovery Clock Output** – Recovered Data clock Output (FIFO not used). **Filter Capacitor** – When the analog filter is used this pin is the connection for the RC lowpass filter. The corner frequency should be set as close to the data rate as possible to retain good sensitivity. **FIFO Interrupt Output (active high)** – Indicates when there are remaining bits in the FIFO to be read. Set the FIFO Fill level to 1 in the *FIFO Configuration Register*.
8	ClkOut	Optional host processor Clock Output. Frequency programmable through the *Battery Detect Threshold and Clock Output Register.*
9	Xtal/Ref	**Xtal** - Connects to a 10MHz series crystal or an external oscillator reference. The circuit contains an integrated load capacitor (See *Configuration Register*) in order to minimize the external component count. The crystal is used as the reference for the PLL, which generates the local oscillator frequency. The accuracy requirements for production tolerance, temperature drift and aging can be determined from the maximum allowable local oscillator frequency error. Whenever a low frequency error is essential for the application, it is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. **Ext Ref** – An external reference, such as an oscillator, may be connected as a reference source. Connect through a .01uF capacitor.
10	nRST	**Reset Output** (active Low)
11	GND	System Ground
12	RF_P	**RF Diff I/O**
13	RF_N	**RF Diff I/O**
14	VDD	Supply Voltage
15	RSSIA	**Analog RSSI Output** – This pin may be used as an input to an A/D for signal strength or may be used as a baseband data output for OOK signaling. See *Baseband Filter Register* to calculate the appropriate filter capacitor value.
16	DDET	**Valid Data Detector Output** - (See *Receiver Control Register* for output definition)

1.1 Processor Mode Pin Configuration



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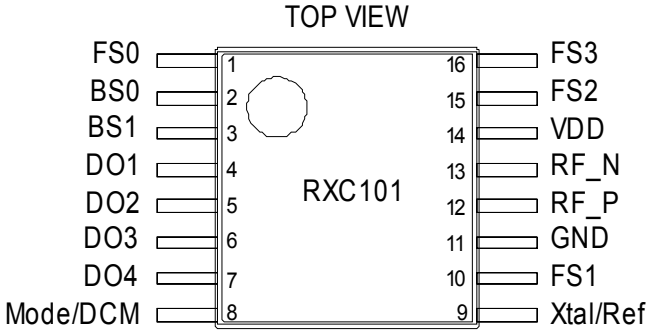
Simple Mode

Pin	Name	Description
1	FS0	**Frequency Select Bit 0**
2	BS0	**Band Select Bit 0**
3	BS1	**Band Select Bit 1**
4	DO1	**Digital Output 1** – May be connected to an LED or other device.
5	DO2	**Digital Output 2** – May be connected to an LED or other device.
6	DO3	**Digital Output 3** – May be connected to an LED or other device.
7	DO4	**Digital Output 4** – May be connected to an LED or other device.
8	Mode/DCM	**Mode Select** – Sets the device in Processor or Simple Mode. When the chip powers on it checks the state of this pin and determines what mode to select. When this pin is connected to VDD or GND, the chip enters Simple Mode. Leaving this pin unconnected powers up the chip in Microprocessor Mode. **(Low Power) Duty Cycle Mode** – After power-up pulling this pin high puts the chip into the predefined duty cycle mode (see page 10 for description).
9	Xtal/Ref	**Xtal** – Connects to a 10MHz series crystal or an external oscillator reference. **Ext Ref** – An external reference, such as an oscillator, may be connected as a reference source. Connect through a .01uF capacitor.
10	FS1	**Frequency Select Bit 1**
11	GND	System Ground
12	RF_P	**RF Signal Input**
13	RF_N	**RF Signal Input**
14	VDD	Supply Voltage
15	FS2	**Frequency Select Bit 2**
16	FS3	**Frequency Select Bit 3**

1.2 Simple Mode Pin Configuration



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2. Functional Description

The RXC101 is a low power, frequency agile, zero-IF, multi-channel FSK receiver for use in the 315, 433, 868, and 916 MHz bands. All RF and baseband functions are completely integrated requiring only a single 10MHz crystal as a reference source and an external low-cost processor. Functions include:

- PLL synthesizer
- LNA, programmable gain
- I/Q Mixers
- I/Q Demodulators
- Baseband Filters
- Baseband Amplifiers
- RSSI
- Low Battery Detector
- Wake-up Timer/Duty Cycle Mode
- Valid Data Detection/Data Quality

The RXC101 is ideal for Frequency Hopping Spread Spectrum (FHSS) applications requiring frequency agility to meet FCC requirements. The RXC101 supports use of a low-cost microcontroller, or may operate as a single chip solution for simple applications. The RXC101 also incorporates different sleep modes to reduce overall current consumption and extend battery life. It is ideal for applications operating from typical lithium coin cells.

2.1 RXC101 Typical Application Circuit

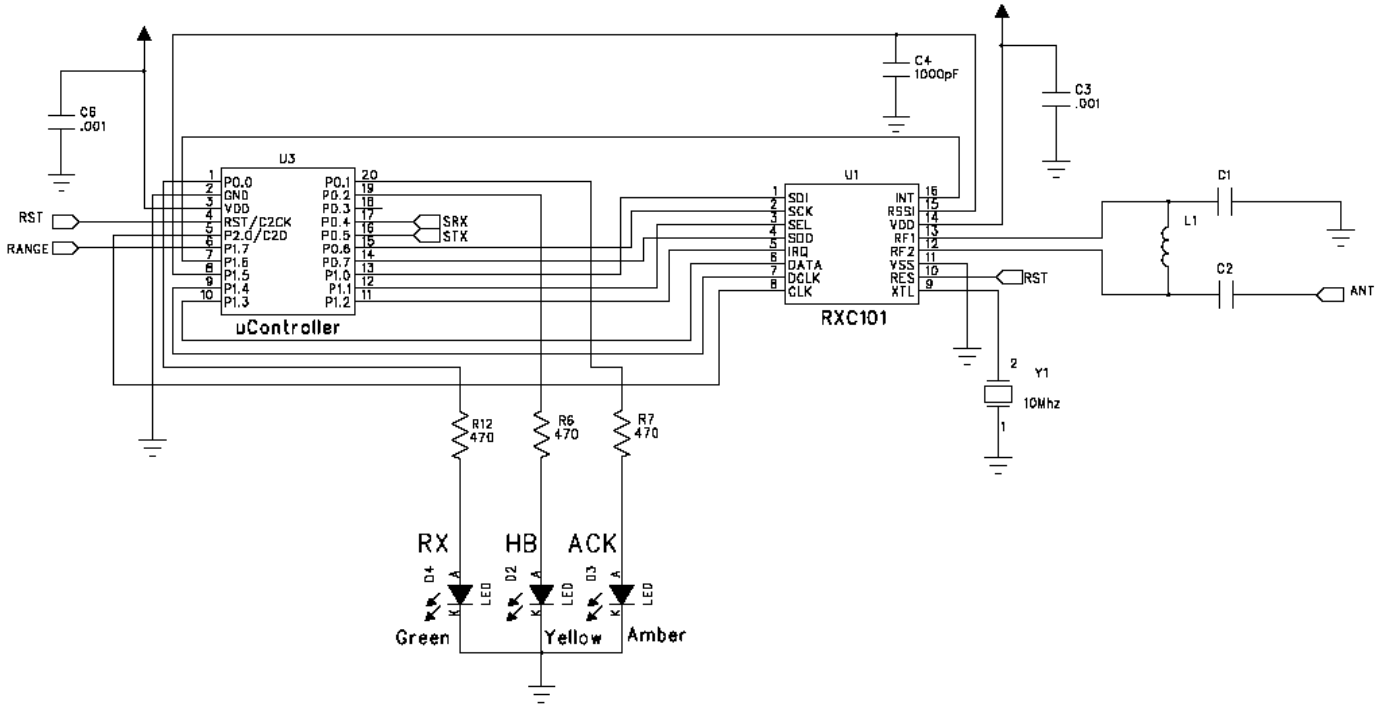

Figure 1. Typical Processor Mode Application Circuit

Processor Mode (Application Circuit)

The RF pins are high impedance and differential. The optimum differential load for the RF port is 250 Ohms. Antennas ideally suited for this would be a Dipole, Folded Dipole, and Loop. A single ended 50 Ohm connection may also be used with the matching circuit given in Figure 1. Matching component values for each band are given in Table 16.

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The matching component values for each band are given in Table 1.

Table 1.

Band	L1	C1=C2
315	56 nH	9 pF
433	36 nH	7 pF
868	15 nH	3 pF
916	15 nH	3 pF

Antenna Design Considerations

The RXC101 was designed to drive a differential output such as a Dipole antenna or a Loop. Most compact applications use the loop since it can be made small. The dipole is typically not an attractive option for compact designs based on the fact of its inherent size at resonance and distance needed away from a ground plane to be an efficient antenna. A monopole is possible with addition of a balun or using the matching circuit in Figure 1.

PCB Layout Considerations

PCB layout is the most critical. For optimal receive performance, the trace lengths at the RF pins must be kept as short as possible. Using small, surface mount components, like 0402, will yield the best performance as well as keep the RF port compact. Make all RF connections short and direct. A good rule of thumb to adhere to is for every 0.1" of trace length add 1nH of series inductance to the path.

The crystal oscillator is also affected by additional trace length in that it adds parasitic capacitance to the overall load of the crystal. To minimize this effect place the crystal as close as possible to the chip and make all connections short and direct. This will minimize the effects of "frequency pulling" that stray capacitance may introduce and allow the internal load capacitance of the chip to be more effective in properly loading the crystal oscillator circuit.

If using an external processor, the RXC101 provides an on-chip clock for that purpose. Even though this is an integrated function, long runs of the clock signal may radiate and cause interference, especially if there is no ground plane run directly under the trace. This can degrade receiver performance. Keep clock connections as short as possible and surround the clock trace with an adjacent ground plane pour where needed. This will help in reducing any radiation or crosstalk due to long runs of the clock signal.

Good power supply bypassing is also essential. Large decoupling capacitors should be placed at the point where power is applied to the PCB. Smaller value decoupling capacitors should then be placed at each power point of the chip as well as bias nodes for the RF port. Poor bypassing lends itself to conducted interference which can cause noise and spurious signals to couple into the RF sections, significantly reducing performance.

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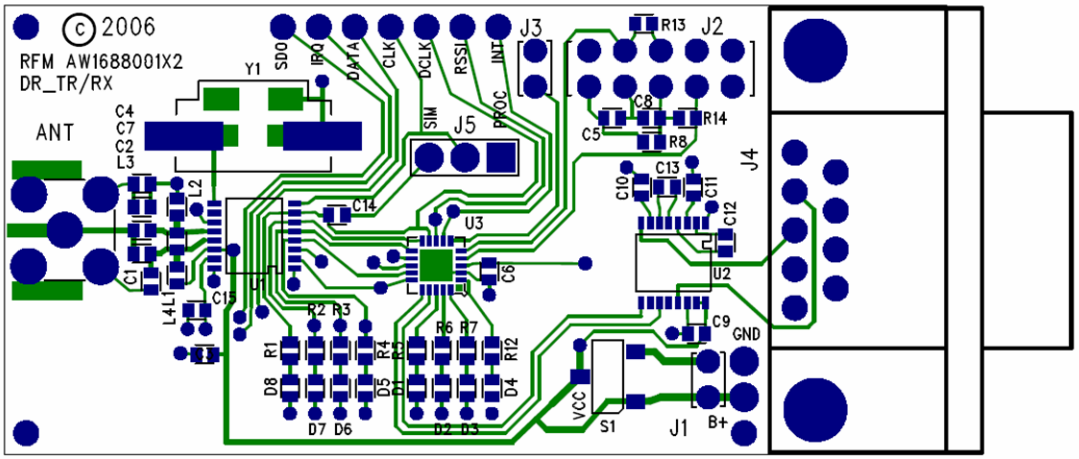
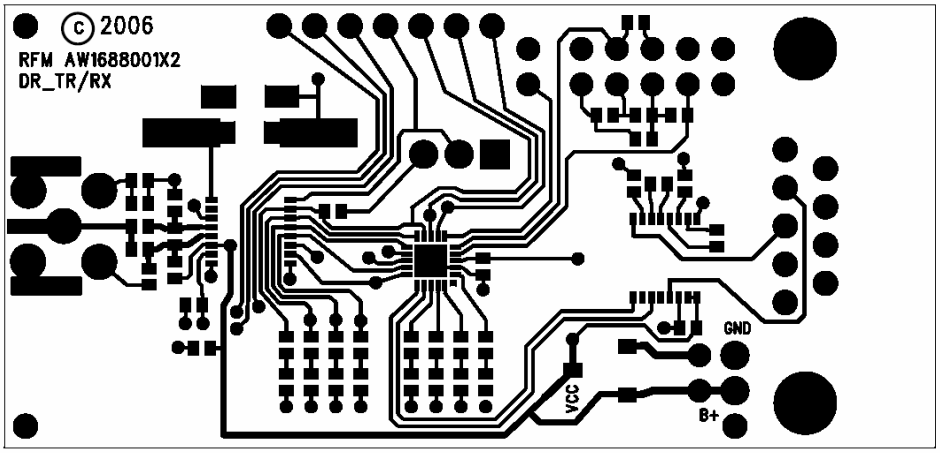
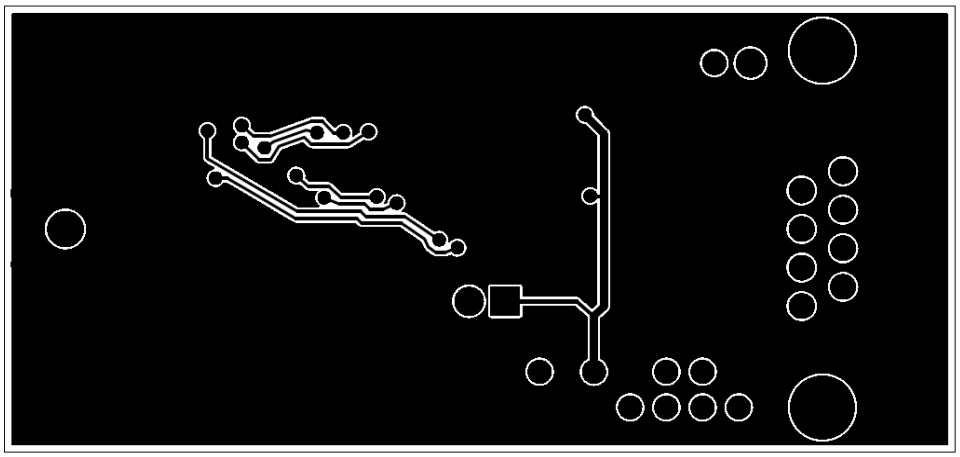


Assembly View



Top Side



Bottom Side

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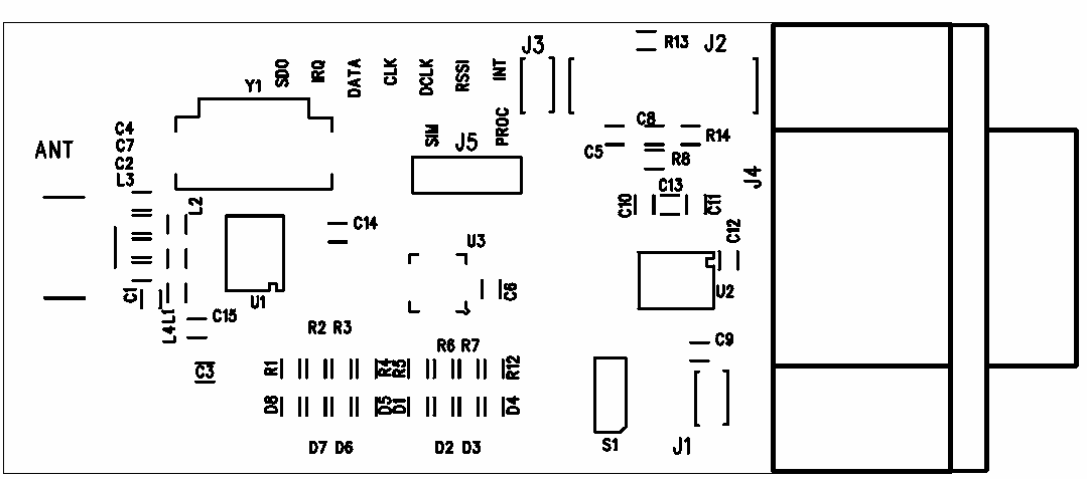

Silkscreen

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2.2 Simple Mode

The RXC101 can be configured for Simple Mode which does not require the use of a processor. All values on for internal registers are the default values assumed during POR. Even though the device is in this mode, the SPI bus, pins 1, 2 and 3, are still available to change internal configurations yet remain in simple mode operation.

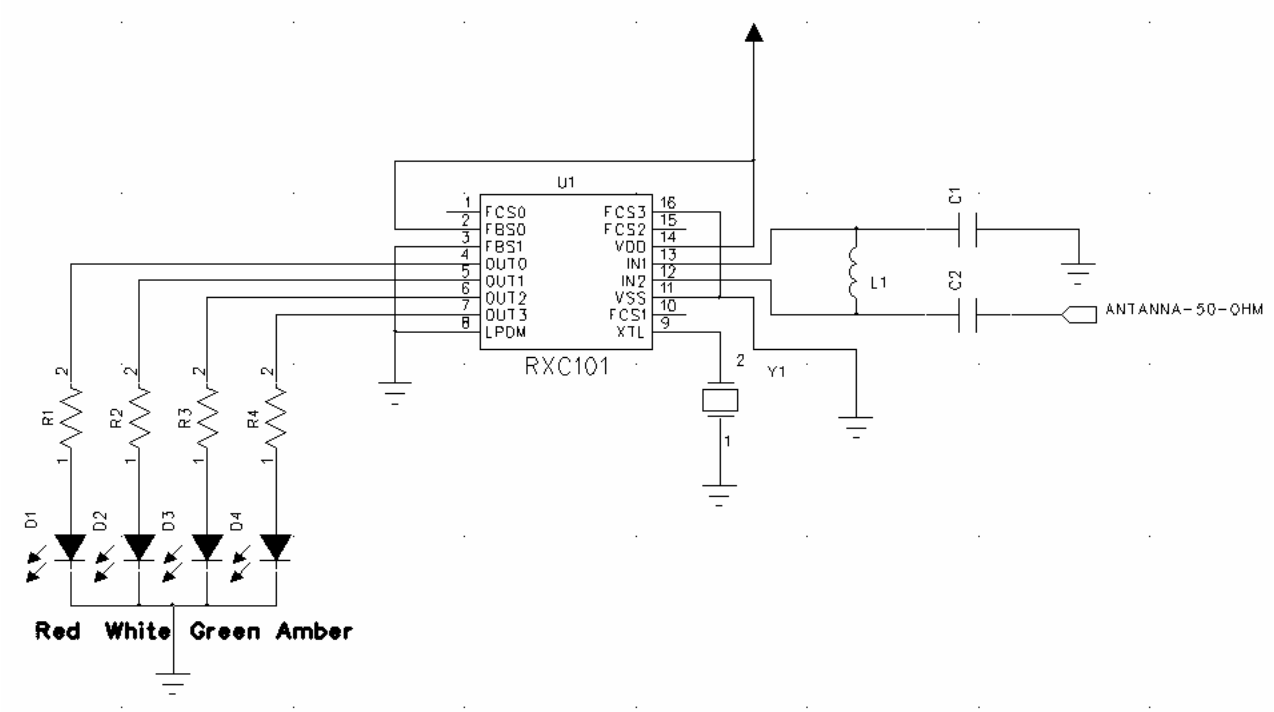

Figure 2. Typical Simple Mode Application Circuit

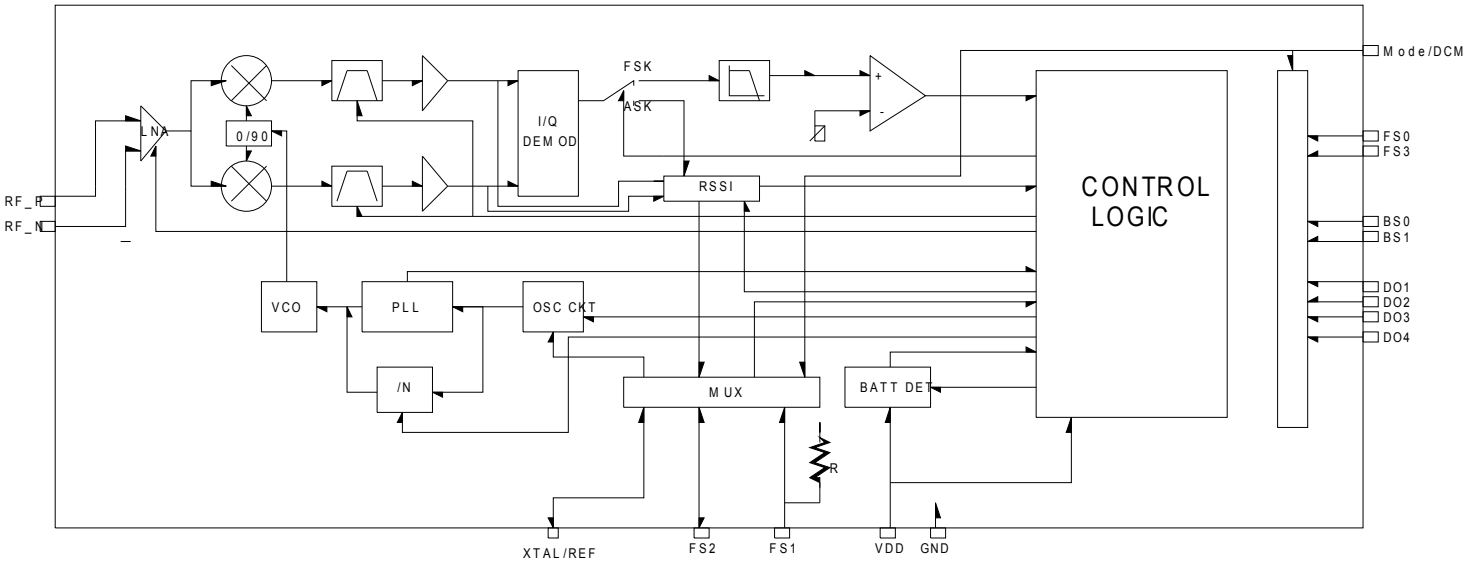

Figure 3. Simple Mode Functional Block Diagram

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At power-up the chip samples the state of pin 8. If the pin is logic '1' on power-up then it enters simple mode. If pin 8 is left unconnected it enters processor mode. In simple mode, 6 pins select the band and frequency within that band of operation. A seventh pin is available to operate the chip in duty cycle mode. Table 2 shows the 6-pin setup configuration.

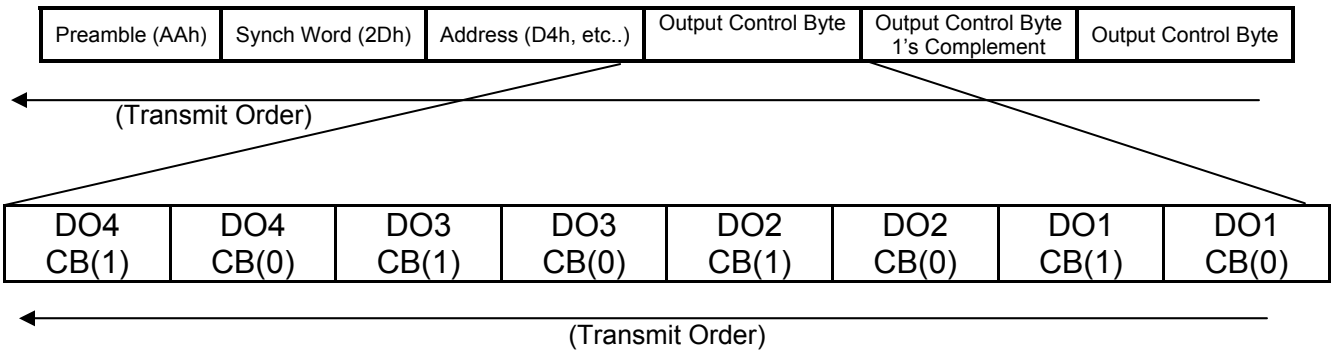
Table 2.

315MHz BS[1,0]=00	433MHz BS[1,0]=01	868MHz BS[1,0]=10	916MHz BS[1,0]=11	Address	FS3	FS2	FS1	FS0
310.320	4330360	*867.680	*900.960	D4h	0	0	0	0
310.960	433.440	*867.840	902.880	D2h	0	0	0	1
311.600	433.520	*868.000	904.800	B4h	0	0	1	0
312.240	433.600	868.160	906.720	B2h	0	0	1	1
312.880	433.680	868.320	908.640	D4h	0	1	0	0
313.520	433.760	868.480	910.560	D2h	0	1	0	1
314.160	433.840	868.640	912.480	B4h	0	1	1	0
314.800	433.920	868.800	914.400	B2h	0	1	1	1
315.440	434.000	868.960	916.320	D4h	1	0	0	0
316.080	434.080	869.120	918.240	D2h	1	0	0	1
316.720	434.160	869.280	920.160	B4h	1	0	1	0
317.360	434.240	869.440	922.080	B2h	1	0	1	1
318.000	434.320	869.600	924.000	D4h	1	1	0	0
318.640	434.400	869.760	925.920	D2h	1	1	0	1
319.280	434.480	869.920	927.840	B4h	1	1	1	0
319.920	434.560	*870.080	*929.760	B2h	1	1	1	1

*Out of Band Frequencies

NOTE: Setting FS0='1' will change the DRSSI threshold from -103dBm to -97dBm.

For simple mode a predefined data sequence is defined in order to toggle the four outputs available. The sequence includes a 16-bit preamble, synch word, address, and control bytes. The following is the sequence flow:



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The Control Byte function is defined as follows:

Table 3.

Output Function	CB(1)	CB(0)
NOP	0	0
Set to Logic '0'	0	1
Toggle	1	0
Set to logic '1' for 100ms	1	1

The data section of the packet must be sent as indicated. The 1's complement of the data is internally verified against the actual incoming data to ensure it is receiving the correct data and not spurious transmission from noise or a nearby interferer. By sending the data twice, once before and once after the 1's complement, this confirms to the receiver that it is receiving valid data.

It is possible to use the receiver in a "mixed mode". The SPI bus architecture allows access to the SPI bus in simple mode (pins 1, 2, 3) and thereby makes it possible to overwrite the simple mode default POR values of the control registers. In this way the operating parameters of the receiver can be altered retaining the functionality of the standalone mode when receiving the proper data sequence.

Duty Cycle Mode

After power-up, connecting pin 8 to VDD will enable duty cycle mode. In this mode the chip will wake up every 300ms to sample the signal strength of the incoming signal. If there is none detected then it goes back into sleep until the next 300ms window arrives. When operating in Duty Cycle Mode, the chip consumes less than 500uA of average current.

From start to finish, when the wake-up timer expires and the chip comes out of sleep, it switches on the oscillator and waits 2ms for the oscillator to stabilize then it switches on the synthesizer. The receiver then monitors the incoming signal strength for 6ms. If it detects a signal within that 6ms the synthesizer remains on for 30ms and waits for the preamble and the rest of the packet. If it does not detect a strong enough signal within the 6ms, it goes back into sleep mode until the next wake-up time. If it detects a strong signal, but incorrect data, at the end of the 30ms it will re-enter sleep mode until the next wake-up time. It should be noted that when the receiver is checking for signal strength, the state of the FS0 pin will determine the threshold limit. See NOTE after Table 2. Figure 4 shows the timing for Duty Cycle Mode.

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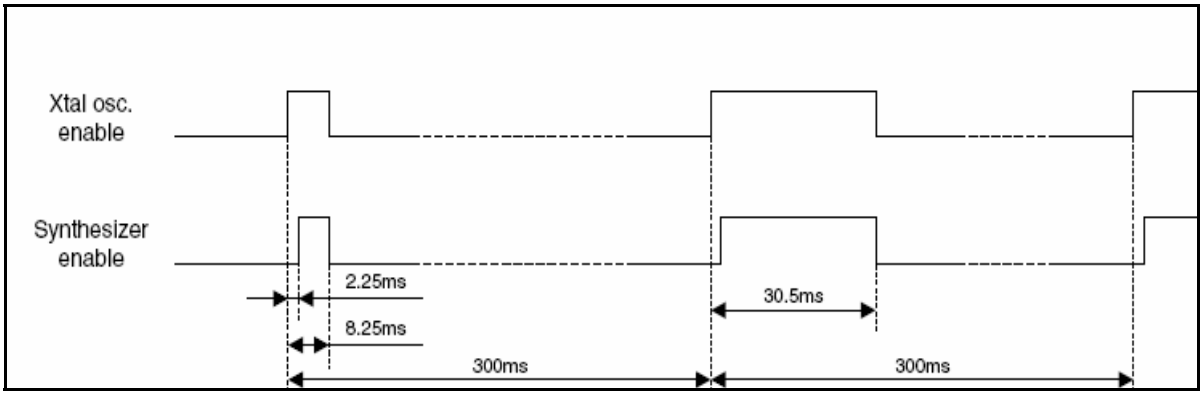

Figure 4. Duty Cycle Mode Wake-up Timing

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3. RXC101 Functional Characteristics

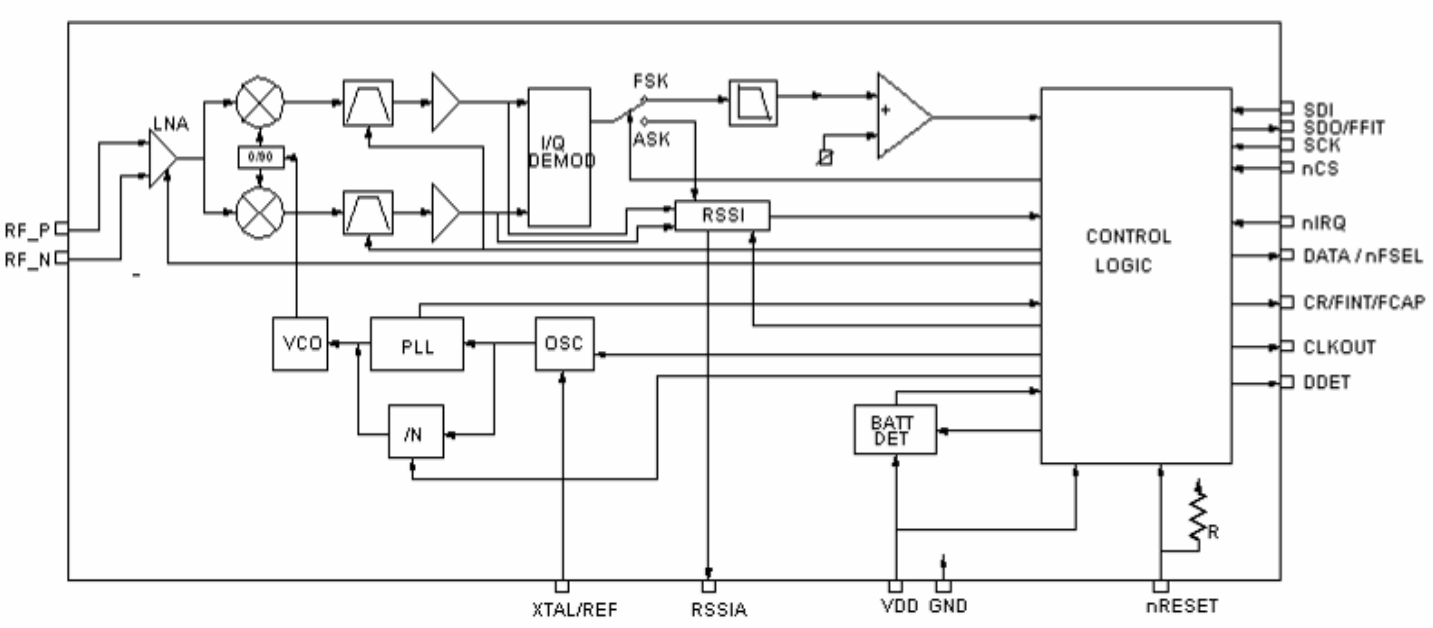

Figure 5. Functional Block Diagram

Input Amplifier (LNA)

The LNA has selectable gain (0dB, -6dB, -14dB, -20dB) which may be useful in an environment with strong interferers. The LNA has a 250ΩOhm differential input impedance (0dB, -14dB) which requires a matching circuit when connected to 50 Ohm devices. Registers common to the LNA are:

- Receiver Control Register

Baseband Data and Filtering

The baseband receiver has several programmable options that optimize the data link for a wide range of applications. The programmable functions include:

- Receive bandwidth
- Receive data rate
- Baseband Analog Filter
- Baseband Digital Filter
- Clock Recovery (CR)
- Receive FIFO
- Data Quality Detector

The receive bandwidth is programmable from 67 kHz to 400 kHz to accommodate various FSK modulation deviations as well as fast data rates. If the data rate is known for a given transmitter, the best results are obtained with a bandwidth at least twice the data rate.

The receive data rate is programmable from 337bps to 256kbps. An internal prescaler is used to give better resolution when setting up the receive data rate. The prescaler is optional and may be disabled through the *Data Rate Setup Register.*

The type of baseband filtering is selectable between an Analog filter and a Digital filter. The analog filter is a simple RC lowpass filter. An external capacitor may be chosen depending on the actual data rate. The chip

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has an integrated 10KOhm resistor in series that makes the RC lowpass network. With the analog filter selected, a maximum data rate of 256kbps can be achieved. The digital filter is used with a clock frequency of 29X data rate. In this mode a clock recovery (CR) circuit is used to provide a synchronized clock source to recover the data using an external processor. The CR has three modes of operation: fast, slow, and automatic, all configurable through the *Baseband Filter Register.* The CR circuit works by sampling the preamble on the incoming data. The preamble must contain a series of 1's and 0's in order for the CR circuit to properly extract the data timing. In slow mode the CR circuit requires more sampling (12 to 16 bits) and thus has a longer settling time before locking. In fast mode the CR circuit takes fewer samples (6 to 8 bits) before locking so settling time is not as long and timing accuracy is not critical. In automatic mode the CR circuit begins in fast mode to coarsely acquire the timing period with fewer samples then changes to slow mode after locking. Further details of the CR and data rate clock are provided in the *Baseband Filter Register.* CR is only used with the digital filter and data rate clock. These are not used when configured for the analog filter.

The Data Quality Detector looks at the unfiltered incoming data and counts the "spikes" for a given period. The higher the "spike" count, the lower the data quality. The data quality threshold may be set, restricting when the chip may report "Good Signal Quality".

Data Quality Detector (DQD)

The DQD is a unique function of the TRC101. The DQD circuit looks at the prefiltered incoming and counts the "spikes" of noise for a predetermined period of time to get an idea of the quality of the link. This parameter is programmable through the *Data Filter Command Register*. The DQD count threshold is programmable from 0 to 7 counts. The higher the count the lower the quality of the data link. This means the higher the content of noise spikes in the data stream the more difficult it will be to recover clock information as well as data.

Valid Data Detector (DDet)

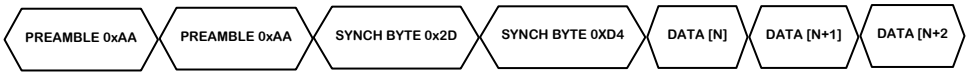
The VDI is an extension of the DQD. When incoming data is detected, it uses the DQD signal, the Clock Recovery Lock signal, and the Digital RSSI signal to determine if the incoming data is valid. The VDI signal is valid when using either the internal receive FIFO or an external pin to capture baseband data. The VDI has three modes of operation: slow, medium, fast. Each mode is dependent on what signals it uses to determine valid data as well as the number of incoming preamble bits present at the beginning of the packet.

Receiver FIFO

The receive FIFO is configured as one 16-bit register. The FIFO can be configured to generate an interrupt after a predefined number of bits have been received. This threshold is programmable from 1 to 16 bits (0..15). It is recommended to set the threshold to at least half the length of the register (8 bits) to insure the external host processor has time to set up before performing a FIFO read. The FIFO read clock (SCK) must be < $f_{XTAL}/4$ or <2.5 MHz for a 10 MHz reference xtal.

The receive FIFO may also be configured to fill only when valid data has been identified. The RXC101 has a synchronous pattern detector that watches incoming data for a particular pattern. When it sees this pattern it begins to store any data that follows. At the same time, if pin 16 is configured for Valid Data Indicator output (See *Receiver Control Register)*, this pin will go 'high' signaling valid data. This can be used to wake up or prepare a host processor for processing data. The internal synchronous pattern is set to 2DD4h and is not configurable.

The receive packet structure when using the synchronous pattern should be:



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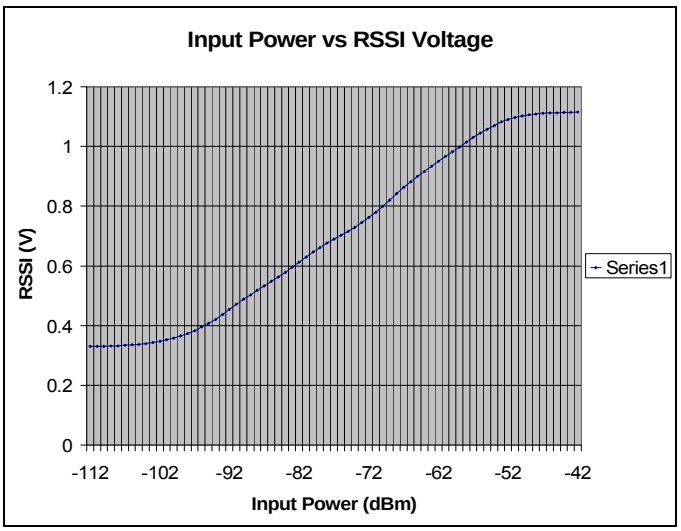
Any packet sent, whether using the synchronous pattern or not, should always start with a preamble sequence of alternating 1's and 0's, such as 1-0-1-0-1. This corresponds to sending a 0xAA or 0x55. The preamble may be one byte (Fast CR lock) or two bytes (Slow CR lock). The next two bytes should be the synchronous pattern. In this case, data storage begins immediately following the 2nd synch byte. All other following bytes are treated as data.

The FIFO can be read out through the SDO pin only by pulling the nFSEL pin (6) 'Low" which selects the FIFO for read and reading out data on the next SPI clock. The FINT pin (7) will stay active (logic '1') until the last bit has been read out, and it will then go 'low'. This pin may also be polled to watch for valid data. When the number of bits received in the FIFO match the pre-programmed limit, this pin will go active (logic '1') and stay active until the last bit is read out as above. An alternative method of reading the FIFO is through an SPI bus *Status Register* read. The drawback to this is that all interrupt and status bits must be read first before the FIFO bits appear on the bus. This could pose a problem for receiving large amounts of data. The best method is using the SDO pin and the associated FIFO function pins.

Receive Signal Strength Indicator (RSSI)

The RXC101 provides an analog RSSI and a digital RSSI. The digital RSSI threshold is programmable through the *Receiver Control Register* and is readable through the *Status Register* only. When an incoming signal is stronger than the preprogrammed threshold, the digital RSSI bit in the *Status Register* is set.



The analog RSSI is available through and external pin (15). This pin requires an external capacitor which sets the settling time. The analog RSSI may be used to recover OOK modulated data at a low rate on the order of 1-2Kbps. The external capacitor value will control the received OOK data rate allowed so choosing a lower value capacitor enables recovery of faster data at the expense of amplitude. Using pin (15) with a sensitive external comparator will yield better results.

Automatic Frequency Adjustment (AFA)

The PLL has the capability to do fine adjustment of the carrier frequency automatically. In this way, the receiver can minimize the offset between the transmit and receive frequency. This function may be enabled or disabled through the *Automatic Frequency Adjustment Register*. The range of offset can be programmed as well as the offset value calculated and added to the frequency control word within the PLL to incrementally change the carrier frequency. The chip can be programmed to automatically perform an adjustment or may be manually activated by a strobe signal. This function has the advantage of allowing:

- Low cost, lower accuracy crystals to be used
- Increased receiver sensitivity by narrowing the receive bandwidth
- Achieving higher data rates

Crystal Oscillator

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The RXC101 incorporates an internal crystal oscillator circuit that provides a 10MHz reference, as well as internal load capacitors. This significantly reduces the component count required. The internal load capacitance is programmable from 8.5pF to 16pF in 0.5pF steps. This has the advantage of accepting a wide range of crystals from many different manufacturers having different load capacitance requirements. Being able to vary the load capacitance also helps with fine tuning the final carrier frequency since the crystal is the PLL reference for the carrier. When the shunt capacitance, Co, is worst case 7pF and the ESR is 300 Ohms max, the oscillator can be expected to meet the start-up times as defined in the AC Characteristics. Crystals with less than 7pF shunt capacitance and lower ESR guarantee much faster start-up times.

An external clock signal is also provided that may be used to run an external processor. This also has the advantage of reducing component count by eliminating an additional crystal for the host processor. The clock frequency is also programmable from eight pre-defined frequencies, each a pre-scaled value of the 10MHz crystal reference. These values are programmable through the *Battery Detect Threshold and Clock Output Register.* The internal clock oscillator may be disabled which also disables the output clock signal to the host processor. When the oscillator is disabled, the chip provides an additional 196 clock cycles before releasing the output, which may be used by the host processor to setup any functions before going to sleep. When putting the device into sleep mode, the clock output must be disabled. If the clock out is not disabled then the crystal oscillator will continue to run causing excessive current consumption.

Frequency Control (PLL) and Frequency Synthesizer

The PLL synthesizer is the heart of the operating frequency. It is programmable and completely integrated, providing all functions required to generate the carriers and tunability for each band. The PLL requires only a single 10MHz crystal reference source. RF stability is controlled by choosing a crystal with the particular specifications to satisfy the application. This gives maximum flexibility in performance.

The PLL is able to perform manual and automatic calibration to compensate for changes in temperature or operating voltage. When changing band frequencies, re-calibration must be performed. This can be done by disabling the synthesizer and re-enabling again through the *Configuration Register*. Registers common to the PLL are:

- Configuration Register
- Frequency Setting Register
- Automatic Frequency Adjust Register

Wake-Up Mode

The RXC101 has an internal wake-up timer that has very low current consumption (1.5uA typical) and may be programmed from 1msec to several days. A calibration is performed to the crystal at startup and every 30 sec thereafter, even if in sleep mode. If the oscillator circuit is disabled the calibration circuit will turn it on briefly to perform a calibration to maintain accurate timing and return to sleep.
The RXC101 also incorporates other power saving modes aside from the wake-up timer. Return to active mode may be initiated from several external events:

- Logic '0' applied to nINT pin (16)
- Low Supply Voltage Detect
- FIFO Fill
- SPI request

If any of these wake-up events occur, including the wake-up timer, the RXC101 generates an external interrupt which may be used as a wake-up signal to a host processor. The source of the interrupt may be read out from the *Status Register* over the SPI bus.

Duty Cycle Mode

The duty cycle register may be used in conjunction with the wake-up timer to reduce the average current consumption of the receiver. The duty cycle register may be set up so that when the wake-up timer brings the chip out of sleep mode the receiver is turned on for a short time to sample if a signal is present and then goes back into sleep and the process starts over. See the *Duty Cycle Set Register*. The receiver must be disabled (RXEN bit 0 cleared in *Receiver Control Register*) and the wake-up timer must be enabled (WKUPEN bit 9 set in *Configuration Register*) for operation in this mode. Figure 6 shows the timing for Duty Cycle Mode.

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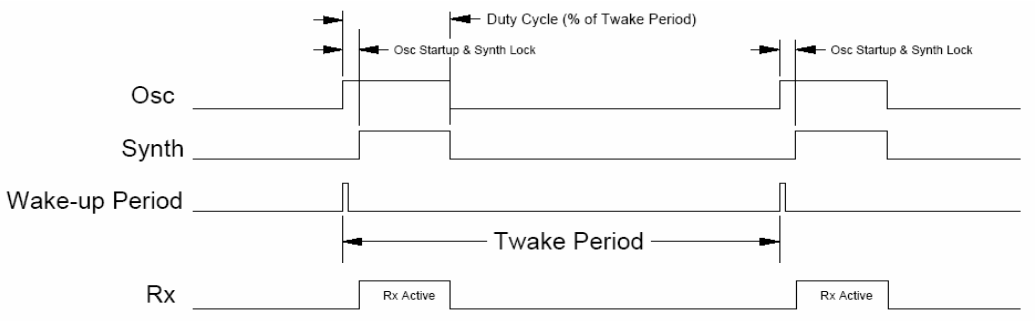

Figure 6. Duty Cycle Mode Timing

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Low Battery Detect

The integrated low battery detector monitors the voltage supply against a preprogrammed value and generates an interrupt when the supply voltage falls below the programmed value. The detector circuit has 50mV of hysteresis built in.

OOK Operation

The RXC101 may operate in a limited OOK function. The RSSI is internally connected to a comparator and the output data is then applied to pin 6. The limitations for this mode are due to the fact that the RSSI signal is not internally capacitively coupled to the comparator, which limits the dynamic range of the received signal, and the DRSSI threshold sets the reference point for the internal comparator.

The best approach for optimal received signal dynamic range would be to implement an external comparator circuit and capacitively couple the RSSI signal from pin 15 to the external comparator. This would eliminate the need to adjust the DRSSI threshold and allow for a much smaller signal amplitude to be recovered. The input LNA gain would still need to be adjusted depending on the strength of the signal in order to optimize the dynamic range. Upon power-up or signal reception, the RSSI may be sampled by an A/D for DC level to determine if the RSSI is in saturation and decide whether to increase or decrease LNA gain for best signal recovery.

SPI Interface

The RXC101 is equipped with a standard SPI bus that is compatible to most any SPI device. All functions and status of the chip are accessible through the SPI bus. Typical SPI devices are configured for byte write operations. The TRC101 uses word writes so the nCS pin should be pulled low for 16 bits. The maximum clock for the SPI bus is 20 MHz.

Symbol	Parameter	Minimum Value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

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Timing Diagram

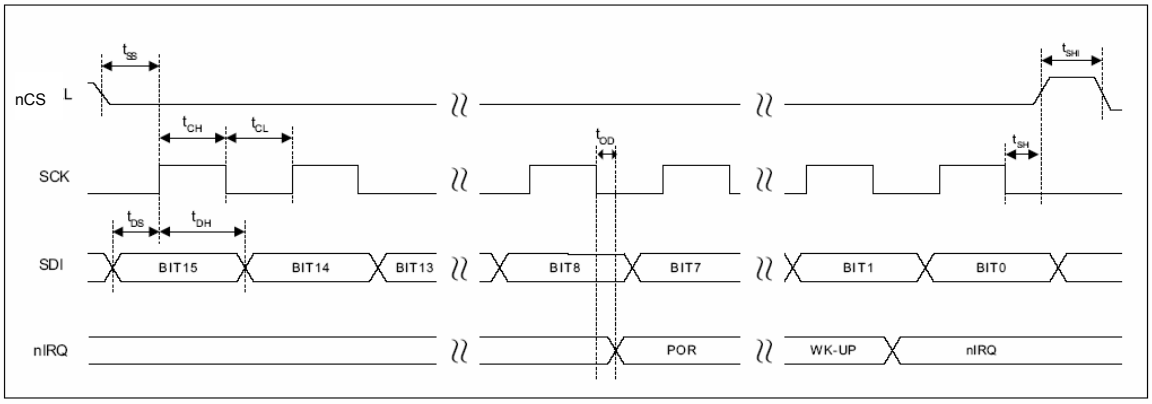

Figure 7. SPI Interface Timing

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4. Control and Configuration Registers

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
STATUS	FIFOIT	FIFOV	WKINT	LB	FIFEMP	RSSI	GDQD	CRLCK	AFATGL	AFA	OFFSGN	OFF4	OFF3	OFF2	OFF1	OFF0	- -
CONFIG	1	0	0	BAND1	BAND0	LBDEN	WKUPEN	OSCEN	CAP3	CAP2	CAP1	CAP0	BB2	BB1	BB0	CLKEN	893Ah
AFA	1	1	0	0	0	1	1	0	AUTO1	AUTO0	RNG1	RNG0	STRB	ACCF	OFFEN	AFEN	C6F7h
FREQ SET	1	0	1	0	Freq11	Freq10	Freq9	Freq8	Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0	A680h
RECV CTRL	1	1	0	0	0	0	0	0	VDI1	VDI0	GAIN1	GAIN0	RSSI2	RSSI1	RSSI0	RXEN	C0C1h
BASEBAND	1	1	0	0	0	1	0	0	CRLK	CRLC	1	FILT	1	DQLVL2	DQLVL1	DQLVL0	C42Ch
FIFO CONFIG	1	1	0	0	1	1	1	0	FINT3	FINT2	FINT1	FINT0	FIFST1	FIFST0	FILLEN	FIFEN	CE89h
DATA RATE SET	1	1	0	0	1	0	0	0	PRE	BITR6	BITR5	BITR4	BITR3	BITR2	BITR1	BITR0	C823h
WAKE-UP PERIOD	1	1	1	R4	R3	R2	R1	R0	MUL7	MUL6	MUL5	MUL4	MUL3	MUL2	MUL1	MUL0	E196h
DUTY CYCLE SET	1	1	0	0	1	1	0	0	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCEN	CC0Eh
BATT DETECT	1	1	0	0	0	0	1	0	CLK2	CLK1	CLK0	LBD4	LBD3	LBD2	LBD1	LBD0	C200h

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Status Register (**Read Only**)

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFOIT	FIFOV	WKINT	LB	FIFEMP	RSSI	GDQD	CRLCK	AFATGL	AFA	OFFSGN	OFF4	OFF3	OFF2	OFF1	OFF0

The Status Register provides feedback for:

- FIFO overwrite
- FIFO fill interrupt
- Low Battery
- Data Quality
- Digital RSSI signal level
- Clock Recovery
- Frequency Offset value and sign
- AFA

Note: The Status Register read command begins with a logic '0' where all other register commands begin with a logic '1'.

Bit [15]:**FIFOIT** – When set, indicates that the number of data bits received by the FIFO has reached it programmed limit. See *FIFO Fill Bit Count Bits[7..4]* of the *FIFO Configuration Register.*

Bit [14]:**FIFOV** – When set, indicates receive FIFO overflow. (Cleared after Status Reg read).

Bit [13]:**WKINT** – When set, indicates a Wake-up timer overflow. (Cleared after Status Reg read).

Bit [12]:**LB** – When set, indicates the supply voltage is below the preprogrammed limit. See *Battery Detect Threshold and Clock Output Register.*

Bit [11]:**FIFEMP** – When set, indicates receive FIFO is empty.

Bit [10]:**RSSI** – When set, this bit indicates that the incoming RF signal is above the preprogrammed Digital RSSI limit.

Bit [9]:**GDQD** – When set, indicates good data quality.

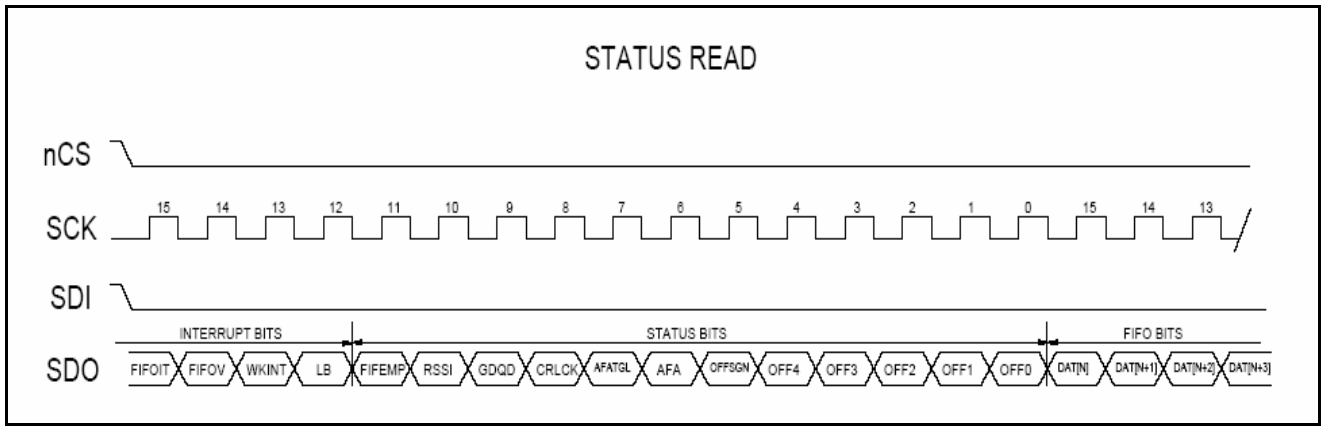
Bit [8]:**CRLCK** – When set, indicates Clock Recovery is locked.

Bit [7]:**AFATGL** – For each AFA cycle run, this bit will toggle between logic '1' and logic '0'.

Bit [6]:**AFA** – When set, indicates that the frequency adjust has detected the same offset value for two consecutive measurements and thus the frequency is stabilized.

Bit [5]:**OFFSGN** – Indicates the difference in frequency is higher (logic '1') or lower (logic '0') than the chip frequency.

Bit [4..0]:**OFF[4..0]** – The offset value to be added to the frequency control word (internal PLL). In order to get accurate values the AFA has to be disabled during the read by clearing the "AFEN" bit in the AFA Register (bit 0).



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Configuration Register [POR=893Ah]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	BAND1	BAND0	LBDEN	WKUPEN	OSCEN	CAP3	CAP2	CAP1	CAP0	BB2	BB1	BB0	CLKEN

The configuration register sets up the following:

- Internal Data Register
- Internal FIFO
- Frequency Band in use
- Crystal Load capacitance

Bit [15..13] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the *Configuration Register*.

Bit [12..11] – **Band Select:** These bits set the frequency band to be used. There are four (4) bands that are supported. See Table 4 for Band configuration.

TABLE 4.

Frequency Band	BAND1	BAND0
315	0	0
433	0	1
868	1	0
916	1	1

Bit [10] – **Low Battery Detector:** This bit enables the battery voltage detect circuit when set. The battery detector can be programmed to 32 different threshold levels. See *Battery Detect Threshold and Clock Output Register* section for programming.

Bit [9] – **Wake-up Timer Enable:** This bit enables the wake-up timer when set. See *Wake-up Timer Period Register* section for programming the wake-up timer interval value.

Bit [8] – **Crystal Oscillator:** This bit enables the oscillator circuit when set. The oscillator provides the reference signal for the synthesizer when setting the receive frequency of use.

Bit [7..4] – **Load Capacitance Select:** These bits set the load capacitance for the crystal reference. The internal load capacitance can be varied from 8.5pF to 16pF in .5pF steps to accommodate a wide range of crystal vendors as well as adjust the reference frequency and compensate for stray capacitance that may be introduced due to PCB layout. See Table 5 for load capacitance configuration.

TABLE 5.

CAP3	CAP2	CAP1	CAP0	Crystal Load Capacitance
0	0	0	0	8.5
0	0	0	1	9
0	0	1	0	9.5
0	0	1	1	10
0	1	0	0	10.5
0	1	0	1	11
0	1	1	0	11.5
0	1	1	1	12
1	0	0	0	12.5
1	0	0	1	13
1	0	1	0	13.5
1	0	1	1	14

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1	1	0	0	14.5
1	1	0	1	15
1	1	1	0	15.5
1	1	1	1	16

Configuration Register (**continued)**

Bit [3..1] – **Receiver Baseband Bandwidth:** These bits set the baseband bandwidth of the demodulated data. The bandwidth can accommodate different FSK deviations and data rates. See Table 6 for bandwidth configuration.

Table 6.

Baseband BW (kHz)	BB2	BB1	BB0
Resvd	0	0	0
400	0	0	1
340	0	1	0
270	0	1	1
200	1	0	0
134	1	0	1
67	1	1	0
Resvd	1	1	1

Bit [0] – **Clock Output Disable:** This bit disables the oscillator clock output when set. On chip reset or power up, clock output is on so that a processor may begin execution of any special setup sequences as required by the designer. See *Battery Detect Threshold and Clock Output Register* section for programming details.

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Receiver Control Register [POR=C0C1h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	VDI1	VDI0	GAIN1	GAIN0	RSSI2	RSSI1	RSSI0	RXEN

The Receiver Control Register configures the following:

- Receiver LNA gain
- Digital RSSI threshold
- Receive baseband bandwidth
- Valid Data Indicator response time
- Function of pin 16

Bit [15..8] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Receiver Control Register.

Bit [7..6] – **Pin 16 Func:** Selects the function of Pin 16. See Table 7 below.

Table 7.

Pin 16 Function	VDI1	VDI0
Digital RSSI Out	0	0
DQD Out	0	1
Clock Recovery Lock	1	0
Valid Data Output	1	1

Bit [5..4] – **Receiver LNA Gain:** These bits set the receiver LNA gain, which can be changed to accommodate environments with high interferers. The LNA gain also affects the true RSSI value. Refer to Bit [2..0] for RSSI. See Table 8 below for gain configuration.

Table 8.

LNA GAIN (dB)	GAIN1	GAIN0
0	0	0
-6	0	1
-14	1	0
-20	1	1

Bit [3..1] – **Digital RSSI Threshold:** The digital receive signal strength indicator threshold may be set to indicate that the incoming signal strength is above a preset limit. The result is stored in bit 7 of the status register. There are eight (8) predefined thresholds that can be set. See Table 9 below for settings.

Table 9.

RSSI Thresh	RSSI2	RSSI1	RSSI0
-103	0	0	0
-97	0	0	1
-91	0	1	0
-85	0	1	1
-79	1	0	0
-73	1	0	1
Resvd	1	1	0
Resvd	1	1	1

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Receiver Control Register **(continued)**

The RSSI threshold is affected by the LNA gain set value. Calculate the true RSSI set threshold when the LNA gain is set to a value other than 0 dB as:

RSSI = RSSIthres + |GainLNA|

Bit [0] – **Receiver Chain Enable:** This bit enables the entire receiver chain when set. The receiver chain comprises the baseband circuit, synthesizer, and crystal oscillator. When using this bit to control the receive chain, the clock pulses produced when the crystal oscillator is shut down is disabled. When this bit is cleared, the clock output signal stops abruptly.

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FIFO Configuration Register [POR=CE89h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	1	1	0	FINT3	FINT2	FINT1	FINT0	FIFST1	FIFST0	FILLEN	FIFEN

The Data FIFO Configuration Register configures:

- FIFO fill interrupt condition
- FIFO fill start condition
- FIFO fill on synchronous pattern
- FIFO Enable

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Data FIFO Configuration Register.

Bit [7..4] – **FIFO Fill Bit Count:** This sets the number of bits that are received before generating an external interrupt to the host processor that the receive FIFO data is ready to be read out. It is possible to set the maximum fill level to 15 (16-bits), but the designer must account for the processing time it will take to read out the data before a register overrun occurs, at which data will be lost. It is recommended to set the fill value to half of the desired number of bits to be read to ensure enough time for additional processing. See *Status Register* for description of FIFO status bits that may be read and *FIFO Read Register* for polling and interrupt-driven FIFO reads from the SPI bus.

Bit [3..2] – **FIFO Fill Start Condition:** These bits set the condition at which the FIFO begins filling with data. Table 10 describes the start conditions. See Valid Data configuration in *Receiver Control Register*.

Table 10.

Fill Start Condition	FIFST1	FIFST0
Valid Data	0	0
Synch Word	0	1
Valid Data and Sync Word	1	0
Continuous Fill	1	1

Bit [1] – **Synchronous Pattern FIFO Fill Enable:** When set, the FIFO will begin filling with data when it detects the FIFO Fill Start Condition as defined in bits[3..2] above. The FIFO fill stops and the FIFO is reset when this bit is cleared. To restart simply clear the bit and set again.

Bit [0] – **FIFO Enable:** This bit enables the internal data FIFO when set. If the data FIFO is enabled, the DATA/nFSEL pin (6) must be pulled “Low”. The FIFO is used to store data during receive. If the FIFO is enabled by setting this bit, pin 6 becomes nFSEL and pin 7 becomes FINT.

***Recommended FIFO Read Method**

The Rx FIFO is directly accessible by using the nFSEL select pin (6) and monitoring the FINT interrupt pin (7) for pending data. Each data bit may be clocked in on the rising edge of SCK. See Figure 8 for timing reference.

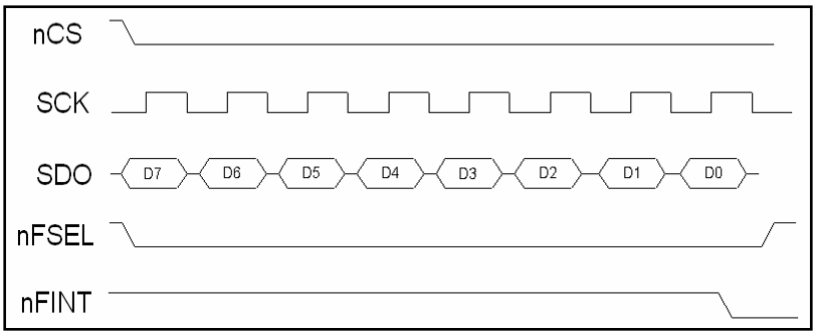

Figure 8. Recommended FIFO Read Method Timing

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***NOTE: The internal FIFO cannot be accessed faster than $f_{XTAL}/4$ when reading the FIFO or data errors will occur. For a 10MHz ref xtal the max SCK <2.5MHz.**

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Automatic Frequency Adjust Register [POR=C6F7h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	1	0	AUTO1	AUTO0	RNG1	RNG0	STRB	ACCF	OFFEN	AFEN

The AFA (Automatic Frequency Adjust) Register configures:

- Manual or Automatic frequency offset adjustment
- Calculation of the offset value and write to the Status Register
- Fine offset adjustment control

The AFA (Automatic Frequency Adjust) Register controls and configures the frequency adjustment range and mode for keeping the receiver frequency locked, providing for an optimal link. The AFA may be manually controlled by an external processor by asserting a strobe signal to initiate a sample, or may be setup for automatic operation. The AFA also calculates the offset of the transmit and receive frequency. This offset value is included in the status register read and the AFA must be disabled during the status read to ensure reporting good offset accuracy.

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Automatic Frequency Adjust Register.

Bit [7..6] – **Mode Selection:** These bits select Automatic or manual operation. When set to Manual operation, the RXC101 will take a sample when a strobe signal (See Bit [3]) is written to the register. There are four modes of operation. See Table 11 below for configuration.

TABLE 11.

Automatic f_{OFFSET} Mode	AUTO1	AUTO0
Mode Off	0	0
Run Once after Pwr-up	0	1
Keep offset during Rcv ONLY	1	0
Keep offset indep of VDI state	1	1

Mode Operation

Mode(0,1) – The circuit takes a measurement only once after power-up. This maximizes the distance that can be achieved for a single link.

Mode(1,0) – When the Valid Data Indicator (VDI) pin is low, indicating poor receiving conditions, the offset register is automatically cleared. Use this setting when receiving from several different transmitters that are operating very close to the same frequencies.

Mode(1,1) – This setting is best used when receiving from a single transmitter. The measured offset value is kept independent of the state of the VDI signal.

Bit [5..4] – **Allowable Frequency Offset:** These bits select the amount of offset allowable between Transmitter and Receiver frequencies. The allowable range can be specified as in Table 12 below.

TABLE 12.

Freq Offset Range	RNG1	RNG0
No Limit	0	0
+15*fres/-16*fres	0	1
+7*fres /-8*fres	1	0
+3*fres /-4*fres	1	1

where fres is the tuning resolution for each band as follows:

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fres: 315 MHz Band = 2.5kHz
433 MHz Band = 2.5kHz
868 MHz Band = 5kHz
916 MHz Band = 7.5kHz

Automatic Frequency Adjust Register **(continued)**

Bit [3] – **Manual Frequency Adjustment Strobe:** This bit is the strobe signal that initiates a manual frequency adjustment sample. When set, a sample of the received signal is compared to the Receiver LO signal and an offset is calculated. If enabled, this value is written to the Offset Register (See Bit [1]) and added to the frequency control word of the PLL. This bit **MUST** be reset before initiating another sample.

Bit [2] – **High Accuracy (Fine) Mode:** This bit, when set, switches the frequency adjustment mode to high accuracy. In this mode the processing time is twice the regular mode, but the uncertainty of the measurement is significantly reduced.

Bit [1] – **Frequency Offset Register Enable:** This bit, when set, enables the offset value calculated by the offset sample to be added to the frequency control word of the PLL that tunes the desired carrier frequency.

Bit [0] – **Offset Frequency Enable:** This bit, when set, enables the RXC101 to calculate the offset frequency by the sample taken from the Automatic Frequency Adjustment circuit.

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Baseband Filter Register [POR=C42Ch]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	1	0	0	CRLK	CRLC	1	FILT1	FILT0	DQLVL2	DQLVL1	DQLVL0

The Baseband Filter Register configures:

- Clock Recovery lock control
- Baseband Filter type, Digital or Analog RC
- Data Quality Detect Threshold parameter

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Baseband Filter Register.

Bit [7] – **Automatic Clock Recovery Lock:** When set, this bit configures the CR (clock recovery) lock control to automatic. In this setting the clock recovery will startup in "Fast" mode and automatically switch to "Slow" mode after locking. See Bit [6] description for details of "Fast" and "Slow" modes.

Bit [6] – **Manual Clock Recovery Lock Control:** When set, this bit configures the CR lock to "Fast" mode. "Fast" mode requires a preamble of at least 6 to 8 bits to determine the clock rate, then locks. When cleared, this bit configures the CR lock to "Slow" mode. "Slow" mode takes a little longer in that it requires a preamble of at least 12 to 16 bits to determine the clock rate, then locks. Use of the "Slow" mode requires more accurate bit timing. See *Data Rate Setup Register* for the relationship of data rate and CR.

Bit [5] – Not Used. Write a "1".

Bit [4..3] – **Filter Type:**

Table 13.

Filter	FILT1	FILT0
RSSI for OOK	0	0
Digital	0	1
Not Used	1	0
Analog RC	1	1

RSSI for OOK: The Analog RSSI Output signal is used to receive the incoming data. The Digital RSSI is used for data slicing. Set DRSSI parameter in the *Receiver Control Register.*

Digital Filter: The Digital filter is a digital version of a simple RC lowpass filter followed by a comparator with hysteresis. The time constant for the Digital filter is automatically calculated internally based on the bit rate as set in the *Data Rate Setup Register.*

Analog RC lowpass filter: The baseband signal is fed to pin 7 thru an internal 10K Ohm resistor. The lowpass cutoff frequency is set by the external capacitor connected from pin 7 to GND. To calculate the baseband capacitor value for a given data rate, use:

$$C_{FILT} = 1 / (30{,}000 * \text{Data Rate})$$

Bit [2..0] – **Data Quality Detect Threshold:** The threshold parameter should be set less than four (<4) in order for the Data Quality Detector to report good signal quality in the case that the bit rate is close to the deviation. As the data rate << deviation, a higher threshold parameter is permitted and may report good signal quality.

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Frequency Setting Register [POR=A680h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	0	Freq11	Freq10	Freq9	Freq8	Freq7	Freq6	Freq5	Freq4	Freq3	Freq2	Freq1	Freq0

The Frequency Setting Register sets the exact frequency within the selected band for receive. Each band has a range of frequencies available for channelization or frequency hopping. The selectable frequencies for each band are:

Frequency Band	Min (MHz)	Max (MHz)	Tuning Resolution
300 MHz	310.24	319.75	2.5 kHz
400 MHz	430.24	439.75	2.5 kHz
800 MHz	860.48	879.51	5.0 kHz
900 MHz	900.72	929.27	7.5 kHz

Bit descriptions are as follows:

Bit [15..12] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Frequency Setting register.

Bit [11..0] – **Frequency Setting:** These bits set the center frequency to be used during receive. The value of bits[11..0] must be in the decimal range of 96 to 3903. Any value outside of this range will cause the previous value to be kept and no frequency change will occur. To calculate the center frequency fc, use Table 3 below and the following equation:

$$\mathbf{f_c = 10 * B1 * (B0 + f_{VAL}/4000)\ MHz}$$

where f_{VAL} = decimal value of Freq[11..0] = $96<f_{VAL}<3903$.

Use Table 14 to select the frequency band and substitute into the above equation to calculate the center frequency of the desired band.

TABLE 14.

Range	B1	B0
315 MHz	1	31
433 MHz	1	43
868 MHz	2	43
916 MHz	3	30

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Data Rate Setup Register [POR=C823h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	0	0	0	PRE	BITR6	BITR5	BITR4	BITR3	BITR2	BITR1	BITR0

The Data Rate Setup Register configures:

- the expected data rate for the receiver
- the prescaler
- the effects of the data rate on clock recovery

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Data Rate Setup Register.

Bit [7] – **Prescaler Enable:** When set this bit enables the prescaler to obtain smaller values of expected data rates. The prescaler value is approximately 1/8.

Bit [6..0] – **Data Rate Parameter Value:** These bits represent the decimal value of the 7-bit parameter used to calculate the expected data rate. To calculate the expected data rate, use the following formula:

$$DR_{exp}(kbps) = 10000 / [29 * (BITR[6..0]+1) * (1+PRE*7)]$$

where BITR[6..0] is the decimal value 0 to 127 and the prescaler (PRE) is '1' (on) or '0' (off).

To calculate the BITR[6..0] decimal value for a given bit rate, use the following formula:

$$BITR[6..0] = 10000 / [29 * (1+PRE*7) * DR_{exp}] -1$$

where DRexp is the expected data rate and PRE is defined above.

Without the prescaler, the definable data rates range from 2.694kpbs to 344.828kbps. With the prescaler enabled, the definable data rates range from 337 bps to 43.103kpbs.

The Slow clock recovery mode requires more accurate bit timing when setting the data rate. To calculate the accuracy of the data rate for both Fast and Slow mode, use the following:

$$\text{Slow mode Accuracy} = \Delta BR/BR < 1/(29 * N) \qquad \text{Fast mode Accuracy} = \Delta BR/BR < 3/(29 * N)$$

where N is the longest number of expected ones or zeros in the data stream, ΔBR is the difference in the actual data rate vs. the set data rate, and BR is the expected data rate as set above using BITR[6..0].

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Wake-up Timer Period Register [POR=E196h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	R4	R3	R2	R1	R0	M7	M6	M5	M4	M3	M2	M1	M0

The Wake-up Timer Period register sets the wake-up interval for the RXC101. After setting the wake-up interval, the WKUPEN (bit 9 of *Configuration Register*) should be cleared and set at the end of every wake-up cycle. To calculate the wake-up interval desired, use the following:

$$T_{WAKE} = M[7..0] * 2^{R[4..0]}$$

where M[7..0] = decimal value 0 to 255 and R[4..0] = decimal value 0 to 31.

Bit [15..13] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Wake-up Timer Period register.

Bit [12..8] – **Exponential:** These bits define the exponential value as used in the above equation. The value used must be the decimal equivalent between 0 and 31.

Bit [7..0] – **Multiplier:** These bits define the multiplier value as used in the above equation. The value used must be the decimal equivalent between 0 and 255.

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Duty Cycle Set Register [POR=CC0Eh]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	1	1	0	0	DC6	DC5	DC4	DC3	DC2	DC1	DC0	DCEN

The duty cycle register may be used in conjunction with the wake-up timer to reduce the average current consumption of the receiver. The duty cycle register may be set up so that when the wake-up timer brings the chip out of sleep mode the receiver is turned on for a short time to sample if a signal is present and then goes back into sleep and the process starts over.

The duty cycle uses the Multiplier value of the wake-up timer in part for its calculation. To calculate the duty cycle use:

$$\text{Duty Cycle} = ((D[6..0] * 2)+ 1)/M * 100$$

where M is M[7..0] of the Wake-up Timer Period register.

Bit [15..8] – **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Wake-up Timer Period register.

Bit [7..1] – **Duty Cycle Multiplier:** These bits are the decimal value used to calculate the Duty Cycle or “On time” of the Receiver after the wake-up timer has brought the RXC101 out of sleep mode.

Bit [0] – **Duty Cycle Mode Enable:** This bit enables the duty cycle mode when set.

NOTE: The receiver must be disabled (RXEN bit 0 cleared in *Receiver Control Register*) and the wake-up timer must be enabled (WKUPEN bit 9 set in *Configuration Register*) for operation in this mode.

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Battery Detect Threshold and Clock Output Register [POR=C200h]

Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	1	0	CLK2	CLK1	CLK0	LBD4	LBD3	LBD2	LBD1	LBD0

The Battery Detect Threshold and Clock Output Register configures the following:

- Low Battery Detect Threshold
- Output Clock frequency

The Low Battery Threshold is programmable from 2.2V to 5.3V using the following equation:

$$V_T = (LBD[4..0] / 10) + 2.2 \ (V)$$

where LBD[4..0] is the decimal value 0 to 31.

Bit [15..8] - **Command Code:** These bits are the command code that is sent serially to the processor that identifies the bits to be written to the Battery Detect Threshold and Clock Output Register.

Bit [7..5] – **Clock Output Frequency:** These bit set the output frequency of the on-board clock that may be used to run an external host processor. See Table 15 below.

TABLE 15.

Output Clock Frequency (MHz)	CLK2	CLK1	CLK0
1	0	0	0
1.25	0	0	1
1.66	0	1	0
2	0	1	1
2.5	1	0	0
3.33	1	0	1
5	1	1	0
10	1	1	1

The Clock Output can be enabled by clearing the CLKEN bit (0) of the *Configuration Register* and disabled by setting the bit.

Bit [4..0] – **Low Battery Detect Value:** These bits set the decimal value as used in the equation above to calculate the battery detect threshold voltage value. When the battery level falls 50mV below this value, the LBD bit (5) in the status register is set indicating that the battery level is below the programmed threshold. This is useful in monitoring discharge sensitive batteries such as Lithium cells.

The Low Battery Detect can be enabled by setting the LBDEN bit (10) of the *Configuration Register* and disabled by clearing the bit.

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5. Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter	Notes	Min	Max	Units
VDD	Positive supply voltage		-0.5	6	V
V_{in}	Voltage in on any pin		-0.5	Vdd+0.5	V
I_{in}	Input current into any pin except VDD and VSS		-25	25	mA
ESD	Electrostatic discharge with human body model			1000	V
T_{stg}	Storage temperature		-55	125	°C
T_{lead}	Soldering Lead temperature (max 10 s)			260	°C

Recommended Operation Ratings

Symbol	Parameter	Notes	Min	Max	Units
VDD	Supply voltage		2.2	5.4	V
T_{op}	Operating temperature (Ambient environment)		-40	85	°C

Note 1: At minimum, VDD - 1.5 V cannot be lower than 1.2 V.
Note 2: At maximum, VDD+1.5 V cannot be higher than 5.5 V.

6. DC Electrical Characteristics

(Min/max values are valid over the whole recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Digital I/O	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			**min**	**typ**	**max**		
Supply current	Idd			8	13	mA	315MHz Band
				8	14		433MHz Band
				9	15		868MHz Band
				10	17		916MHz Band
Sleep current	I_S				0.15	µA	All blocks disabled
Idle current	I_{IDLE}			3	3.5	mA	Oscillator and baseband enabled
Low battery voltage detector current consumption	I_{VD}			0.5		µA	
Wake-up timer current	I_{WUT}			1.5		µA	
Low battery detect threshold	Vlb		2.2		5.3	V	Programmable in 0.1 V steps
Low battery detection accuracy				±75		mV	
Digital input low level	Vil				0.3*Vdd	V	
Digital input high level	Vih		0.7*Vdd			V	
Digital input current low	Iil		-1		1	µA	Vil = 0 V
Digital input current high	Iih		-1		1	µA	Vih = Vdd, Vdd = 5.4 V
Digital output low level	Vol				0.4	V	Iol = 2 mA
Digital output high level	Voh		Vdd-0.4			V	Ioh = -2 mA
Digital input capacitance					2	pF	
Digital output rise/fall time					10	ns	Load = 15 pF

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7. AC Electrical Characteristics

(Min/max values are valid over the whole recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Receiver	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			min	typ	max		
LNA input power			0			dBm	LNA Max gain
Receiver Sensitivity		2		-112		dBm	315MHz Band
				-110			433MHz Band
				-105			868MHz Band
				-104			916MHz Band
RF input impedance (real, differential)				250		Ohm	LNA gain (0 dB, -14 dB)
RF input capacitance				1		pF	
RF input bias		4	Vcc-0.6		Vcc-0.9	V	
Receiver bandwidth			67		400	kHz	Programmable
FSK bit rate			0.6		115	kbps	Digital filters
					256		Analog filter
OOK bit rate				1		kbps	RSSIcap = 1000pF, ext comparator
IIP3 In band interferers (-85dBm carrier, 1MHz offset, CW)		3		-46		dBm	315MHz Band
				-46			433MHz Band
				-51			868MHz Band
				-55			916MHz Band
IIP3 Out of band interferers (-85dBm carrier, 10 MHz offset, CW)				-15		dBm	315MHz Band
				-15			433MHz Band
				-25			868MHz Band
				-20			916MHz Band
RSSI Output			350		1000	mV	
RSSI output impedance				62K		Ohm	
RSSI accuracy				+/-5		dB	
RSSI dynamic range				46			
RSSI programmable steps				6		dB	
Digital RSSI response time				500		us	RSSI signal goes high after input signal exceeds programmed limit. RSSIcap = 5 nF
Spurious emission (@ Pmax)				<95		dBc	315 MHz Band
							433 MHz Band
							868 MHz Band
							916 MHz Band
AFA lock range				0.8*Δdev		kHz	Δdev = Signal FSK deviation

NOTES:

1- Other crystal frequencies may be used, but every function on chip, including wake-up timer, output clock, data rate, clock recovery, etc.., is dependent on this reference frequency and everything will scale accordingly.

2- BW=67 kHz, BR=1.2 kbps, digital filter, BER=10^{-3}

3- FCC Class 2 Blocking.

4- Vcc = 2.2-5.4V

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AC Electrical Characteristics - continued

(Min/max values are valid over the whole recommended operating range Vdd = 2.2-5.4V. Typical conditions: Top = 27°C; Vdd = 3.0 V)

Timing	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			min	typ	max		
Internal POR timeout					100	ms	Vdd at 90% of final value
Wake-up timer clock period				1		ms	Calibrated every 30 seconds

PLL Characteristics	Sym	Notes		Limit Values		Unit	Test Conditions
Parameter			min	typ	max		
PLL reference freq	f_{REF}	1	8	10	12	MHz	
PLL lock time				20		us	within 1kHz settle, 10MHz step
PLL startup time					250	us	From sleep with Crystal running
Crystal load capacitance	CL		8.5		16	pF	Programmable in 0.5 pF steps, tolerance +/- 10%
Xtal oscillator startup time					5	ms	Crystal ESR < 100
Frequency Range (w/ 10MHz ref xtal)			310.24		318.75	MHz	315MHz Band (2.5kHz steps)
			430.24		439.75		433MHz Band (2.5kHz steps)
			860.48		879.51		868MHz Band (5.0kHz steps)
			900.72		929.27		916MHz Band (7.5kHz steps)

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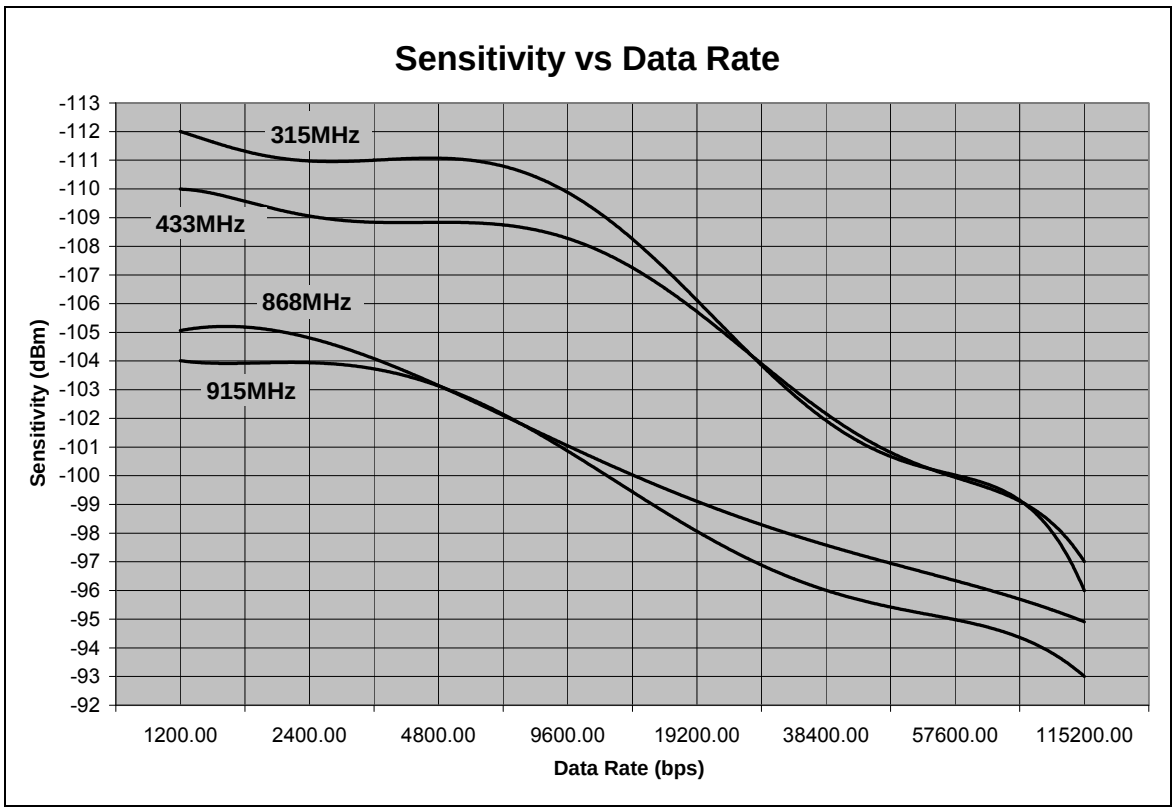
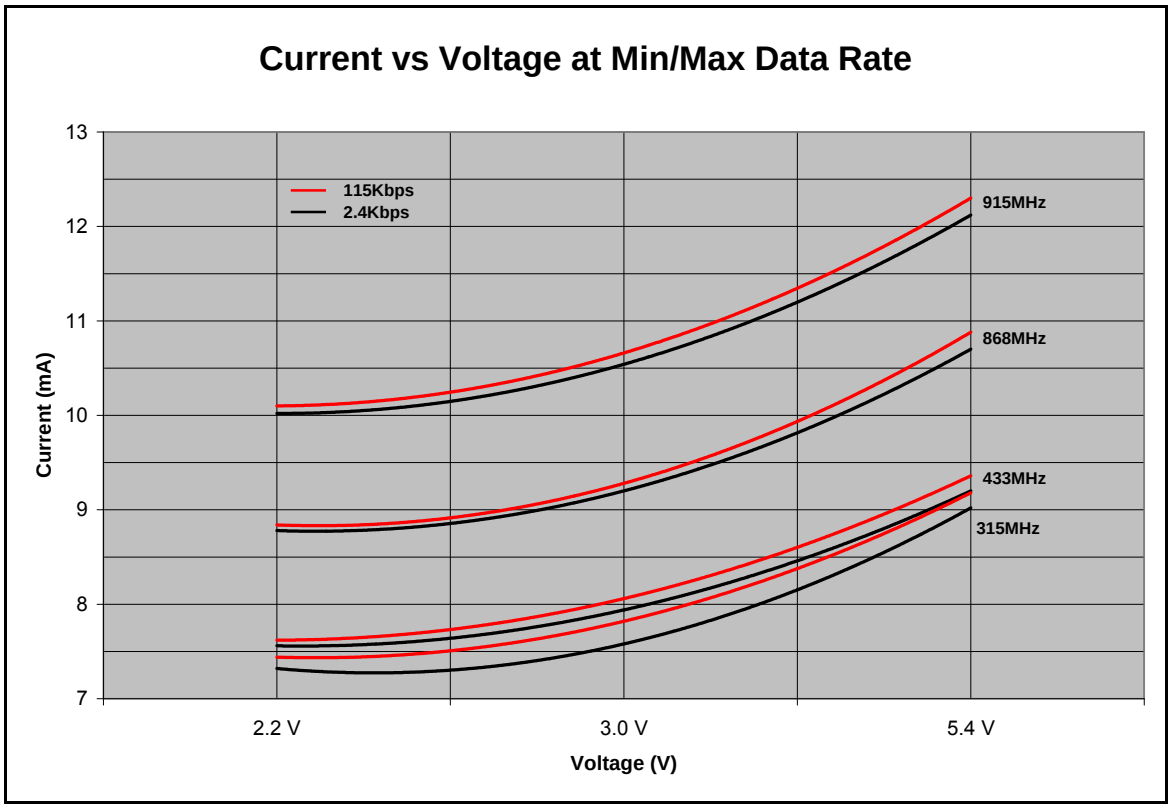
8. Receiver Measurement Results

All data rates are based on a 10^{-3} BER. The receiver measurements were derived from the *Typical Application Circuit* of Figure 1, pg 5, and the layout as suggested on pgs 7-8.





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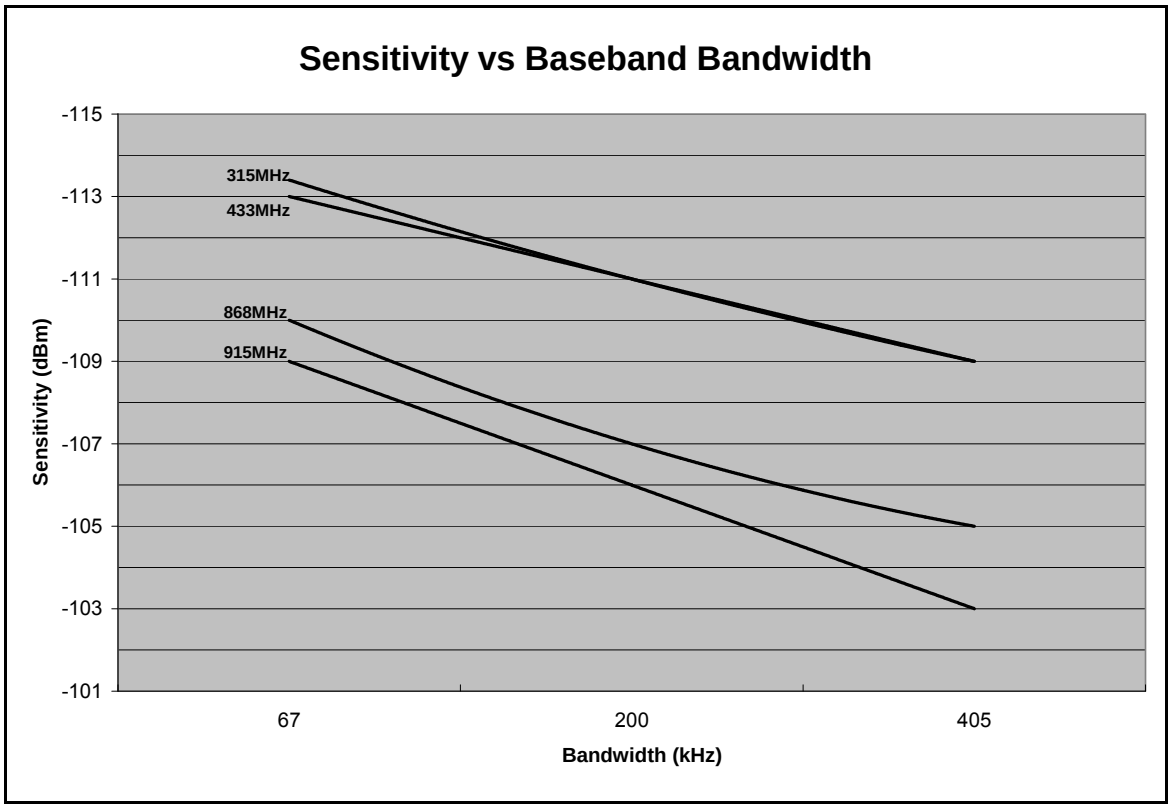

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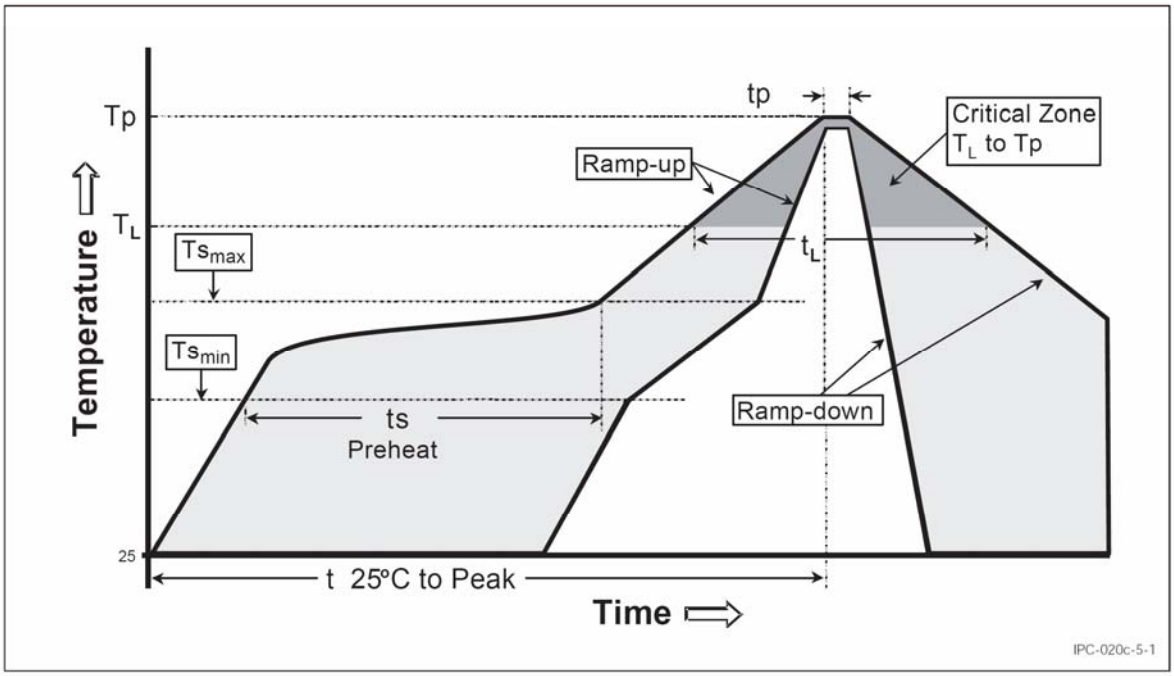
IPC/JEDEC J-STD-020C REFLOW PROFILE

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



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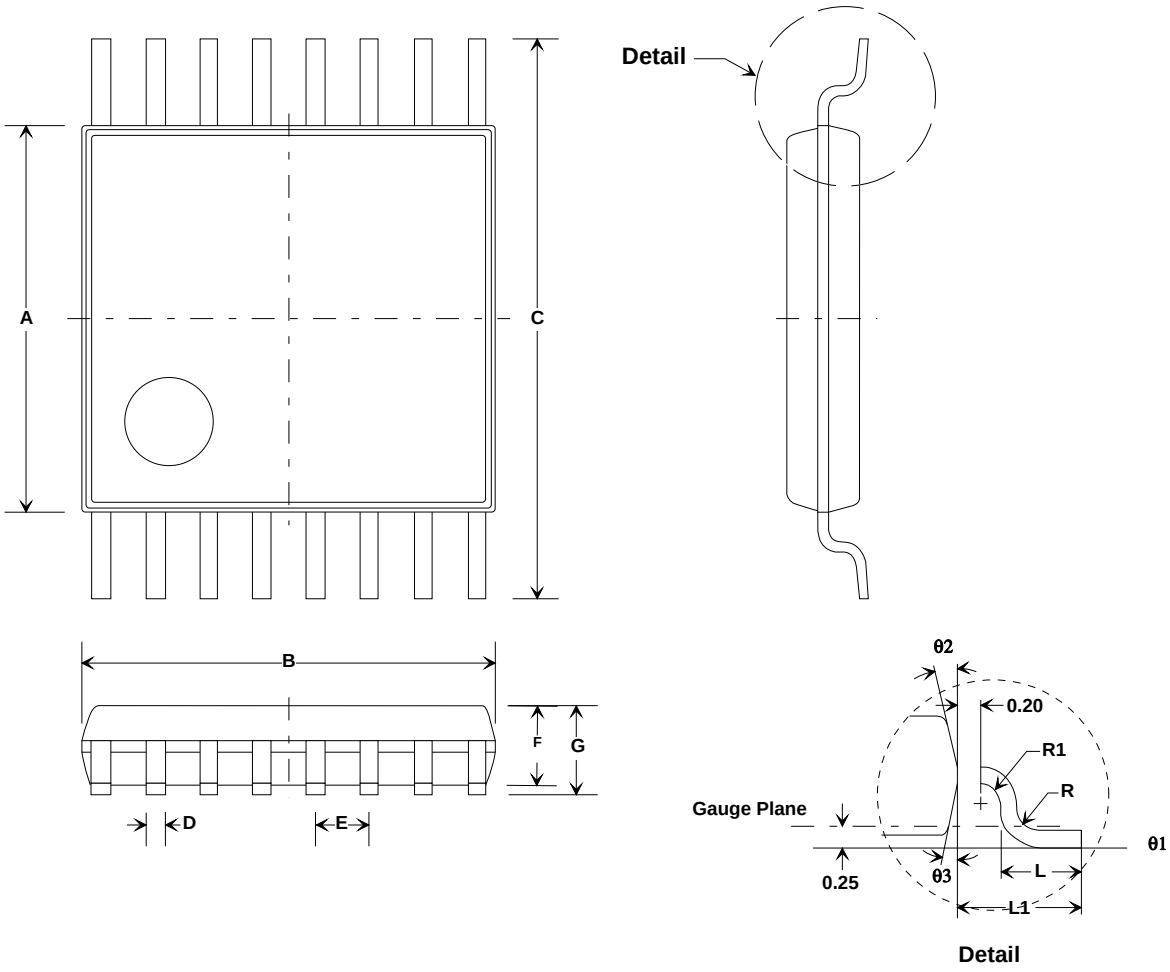
9.0 Package Dimensions – 6.4x5mm 16-pin TSSOP Package

(all values in mm)



Symbol	Dimensions in mm			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.30	4.40	4.50	0.169	0.173	0.177
B	4.90	5.00	5.10	0.193	0.197	0.201
C		6.40 BSC.			0.252 BSC.	
D	0.19		0.30	0.007		0.012
E		0.65 BSC.			0.026 BSC.	
F	0.80	0.90	1.05	0.031	0.035	0.041
G			1.20			0.47
L	0.50	0.60	0.75	0.020	0.024	0.030
L1		1.00 REF.			0.39 REF	
R	0.09			0.004		
R1	0.09			0.004		
θ1	0		8	0		8
θ2		12 REF.			12 REF.	
θ3		12 REF.			12 REF.	

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