D1U86-D-1600-12-HBxDC Series

86mm 1U Front End DC-DC Power Supply Converter

D1U86-D-1600-12-HB3DC variant shown

FEATURES

- 1600W output power
- 93% efficiency at half load
- 12V main output
- 12V standby output of 30W
- 1U height: 3.4" x 7.75" x 1.59"
- 38.6 Watts per cubic inch density
- N+1 redundancy, including hot plugging (up to 8 in parallel)
- Current sharing on 12V main output, ORing FET
- Overvoltage, overcurrent, overtemperature protection
- Internal cooling fan (variable speed)
- PMBus™ / I²C interface monitoring and control
- RoHS compliant
- Two Year Warranty

Available now at
www.murata-ps.com/en/3d/acdc.html

PRODUCT OVERVIEW

The D1U86-D-1600-12-HBxDC series are highly efficient 1600 watt, DC input front end supplies with a 12V main output and a 12V (30W) standby. They have current sharing and up to 8 supplies may be operated in parallel. The supplies may be hot plugged, they recover from overtemperature faults, and have logic and PMBus monitoring and control. Their low profile 1U package and >38.6W/cubic inch power density make them ideal for delivering reliable, efficient power to servers, workstations, storage systems and other 12V distributed power systems.

ORDERING GUIDE

Part Number	Power Output	Main Output	Standby Output[1]	Airflow	Handle Colour
D1U86-D-1600-12-HB4DC	1600W	12Vdc	12Vdc	Back to front	Red
D1U86-D-1600-12-HB3DC				Front to back	Blue

INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Nom.	Max.	Units
Input Voltage Operating Range		-40	-48	-72	Vdc
Turn-on Voltage	Ramp up	-43	-43.5	-44	Vdc
Turn-off Voltage	Ramp down	-38.5	-39	-39.5	
Maximum Current at Vin = -40Vdc	1600W			47	Adc
DC Line Inrush Peak Current	Cold start between 0 to 200msec	40		50	Apk
		72		100	
Efficiency (48V)	20% load		92		%
	50% load		93		
	100% load		89		

OUTPUT VOLTAGE CHARACTERISTICS

Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
12V	Voltage Set Point	50% load	12.17	12.20	12.23	Vdc
	Line and Load Regulation		11.4		12.6	
	Droop			3.10		mV/A
	Ripple Voltage & Noise[1]	20MHz Bandwidth			120	mV p-p
	Output Current		0		133.3	A
	Load Capacitance		0		10000	µF
12VSB	Voltage Set Point	50% load	11.97	12.0	12.03	Vdc
	Line and Load Regulation		11.4		12.6	
	Droop			120		mV/A
	Ripple Voltage & Noise[1]	20MHz Bandwidth			120	mV p-p
	Output Current		0		2.5	A
	Load Capacitance		0		350	µF

[1] Ripple and noise are measured with 0.1 µF of ceramic capacitance and 10 µF of tantalum capacitance on each of the power supply outputs. A short coaxial cable with 50Ω scope termination is used.

For full details go to
www.murata-ps.com/rohs

Test Certificate
and Test Report

OUTPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Rise Monotonicity	No voltage excursion				
Startup Time	DC ramp up		1.5	3	s
Transient Response	12V, 50% load step, 1.0A/µs di/dt		600		mV
	12VSB, 50% load step, 1.0A/µs di/dt		600		
Current sharing accuracy (up to 8 in parallel)2	At 100% load			±5	%
Hot Swap Transients	All outputs remain in regulation			5	%
Holdup Time	At full load (48V input)	1			ms

ENVIRONMENTAL CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Storage Temperature Range		-40		85	°C
Operating Temperature Range		0		55	
Operating Humidity	Noncondensing	5		90	%
Storage Humidity		5		95	
Altitude (without derating at 45°C)		3000			m
Shock	30G non-operating				
Operational Vibration	1G, 10-500Hz, 1.6G (non-operational)				
MTBF	Per Telcordia SR-322 M1C1@ 40°C	500K			hrs
Safety Approvals	CSA/UL 60950-1-07-2nd Ed. IEC 60950-1:2005 (2nd Edition) w Am. 1:2009 CE Marking per LVD DIRECTIVE 2006/95/EC				
Input Fuse	Power Supply has internal 60A/170VDC fast blow fuse on the DC line input				
Weight	1.108kg (2.44lbs)				

[2] The load current of 100% refers to each power module max load connected in an N+1 configuration; therefore the total load will be "N" x 100% load of each module. The share accuracy of ±5% is a fixed percentage irrespective of the total loading and number of units connected in parallel.

PROTECTION CHARACTERISTICS

Output Voltage	Parameter	Conditions	Min.	Typ.	Max.	Units
	Overtemperature (intake)	An OTP warning will be issued via the PMBus interface when the air inlet exceeds 70°C; however the power module shall not shut down until critical internal hotspot temperatures are exceeded.		70		°C
	Overtemperature (hotspots)	The unit will shut down when internal hot spot exceed the derating guide lines and automatically recovers when the unit is cooled down. The unit will shut down due to hot spot at ambient temperature between 55°C-60°C with main 12V at full load.		55-60		
12V	Overvoltage	Latching	13.2		14.4	V
	Overcurrent	For overloads (slow) over current events a 147A nominal constant current will be sustained until the output voltage drops below 3VDC. At this point the unit shall shut down after a 1sec period and remain in that condition for 10secs. The cycle will then repeat. For severe (short circuit) over current events the unit shall shut down within 1ms and remain in this condition for 200ms before attempting a re-start. the unit shall attempt 10 shutdown/re-start cycles before permanently latching off. It will then be necessary to either recycle the DC input or toggle the PSON# input.	137		154	
12VSB	Overvoltage	Latching	13.2		14.4	V
	Overcurrent	Auto-recovery	2.75		3.0	A

ISOLATION CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Insulation Safety Rating / Test Voltage	Input to Output - Basic	1500			Vdc
	Input to Chassis - Basic	1500			Vdc
Isolation	Output to Chassis	500			Vdc

EMISSIONS AND IMMUNITY		
Characteristic	Standard	Compliance
Conducted Emissions	FCC 47 CFR Part 15/CISPR 22/EN55022	Class A, 6dB margin
ESD Immunity	IEC/EN 61000-4-2	Level 3 criteria A
Radiated Field Immunity	IEC/EN 61000-4-3	Level 3 criteria B
Electrical Fast Transient Immunity	IEC/EN 61000-4-4	Level 3 criteria A
Surge Immunity	IEC/EN 61000-4-5	Level 2 criteria B
Radiated Field Conducted Immunity	IEC/EN 61000-4-6	Level 3 criteria A
Magnetic Field Immunity	IEC/EN 61000-4-8	3 A/m criteria B

STATUS AND CONTROL SIGNALS

Signal Name	I/O	Description	Interface Details
PSOK (Output OK)	Output	The PSOK output is a logical "OR" of three internal signals; however the output is not strictly a "digital" signal that transitions between "low" and "high" but is analogue in nature. The internal logic signals are as follows: 1. DC_OK_H 2. PWR_GOOD_H 3. PS_FAULT_L The following is a "truth table" that shows the analogue levels of operation of the signal dependent upon the three internal logic signals: PSOK TRUTH TABLE VS. ANALOG OUTPUT DC_OK_H / PWR_GOOD_H / PS_FAULT_L / PSOK / OPERATION MODE 0 / 0 / 1 / < 0.1Vdc / No DC Input 0 / 1 / 1 / (1/3) VDD / Invalid 1 / 0 / 1 / (2/3) VDD / Standby 1 / 1 / 1 / VDD / Power Good X / X / 0 / 0.2-0.4Vdc / PS Fault (VDD = 3.3Vdc) The timing relationship of this signal is shown in the Timing Specification section that follows.	Each internal signal is buffered and provided with a series or pull up resistor: 1. DC_OK_H; 1K62 series resistor 2. PWR_GOOD_H; 3K32 series resistor 3. PS_FAULT_L; a 10K pull up resistor to VDD_OR (an internally derived 3.3VDC rail) The embedded truth table shows the appropriate levels.
PS_INTERRUPT (FAULT/WARNING)	Output	The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed.	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Driven low by internal buffer (open drain output).
PRESENT#	Output	Based on the industry standard Common Slot requirement this signal is used to detect the presence of an (installed) power module within the host system. However it is also intended to "Enable" the Main 12Vdc output. The signal is also designed to control the power module during hot plug insertion/extraction in conjunction with the host system and is provided on a short "last to make; first to break" signal pin. To "enable" the Main 12Vdc output the signal requires to be pulled "high" with respect +12V_GND. The value of the pull up resistor varies with the applied voltage rail and is as follows: 1. If the signal is to be pulled up to the 12VSB output then the resistor value should be 21KΩ 2. If the signal is to be pulled up to a 3.3Vdc rail (locally derived within the host system) then the resistor value should be 5.11KΩ	The voltage level on the system side of the PSPRESENT# signal will be as follows: 1. When the power module is not installed the voltage will be as per the rail to which it is pulled up to (3.3Vdc or 12Vdc) 2. When the power module is installed the voltage will be pulled down to 0.54Vdc ±5%).
PS_ON (Power Supply Enable/Disable	Input	The PS_ON can be permanently connected to +12V_GND (via the host system mid/back plane) to "enable" the Main 12Vdc output. Alternatively the signal can be connected via the host system electronics to provide the ability to switch between "enable/disable" states. The signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12Vdc output will be enabled when this signal is pulled low to +12V_GND. In the low state the signal input shall source a nominal 1.2mAdc. The 12Vdc output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions.	Pulled up internally via 10K to 3.3Vdc. A logic high >2.0Vdc A logic low <0.8Vdc Input is via CMOS Schmitt trigger buffer.

STATUS AND CONTROL SIGNALS (CONTINUED)

Signal Name	I/O	Description	Interface Details
ADDR (Address Select)	Input	An analogue input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used during digital communications. Connection of a suitable resistor to +12V_GND, in conjunction with an internal resistor divider chain, will configure the required address.	DC voltage between the limits of 0 and +3.3Vdc.
SCL (Serial Clock)	Both	A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	V_{IL} is 0.8V maximum V_{OL} is 0.4V maximum when sinking 3mA V_{IH} is 2.1V minimum
SDA (Serial Data)	Both	A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered,	V_{IL} is 0.8V maximum V_{OL} is 0.4V maximum when sinking 3mA V_{IH} is 2.1V minimum
$I_{MONITOR}$	Analogue Voltage	The current monitor signal is an analogue DC voltage that indicates the actual current contribution provided by a single unit. If the power module is the sole contributor to the system load current then the indicated current (proportional to the DC voltage) is the total load current. If the power module is one of a number ("N") of units "sharing" the overall load current then the indicated current should be considered as a contribution where the total load will be "N" times that of the indicated current of a single module. For a single unit the voltage of the signal pin would read 8VDC at 100% module capability. For two identical units sharing the same 100% current this would read 4VDC for perfect current sharing (i.e. 50% module load capability per unit).	Analogue voltage: +8V maximum; 10K to +12V_GND

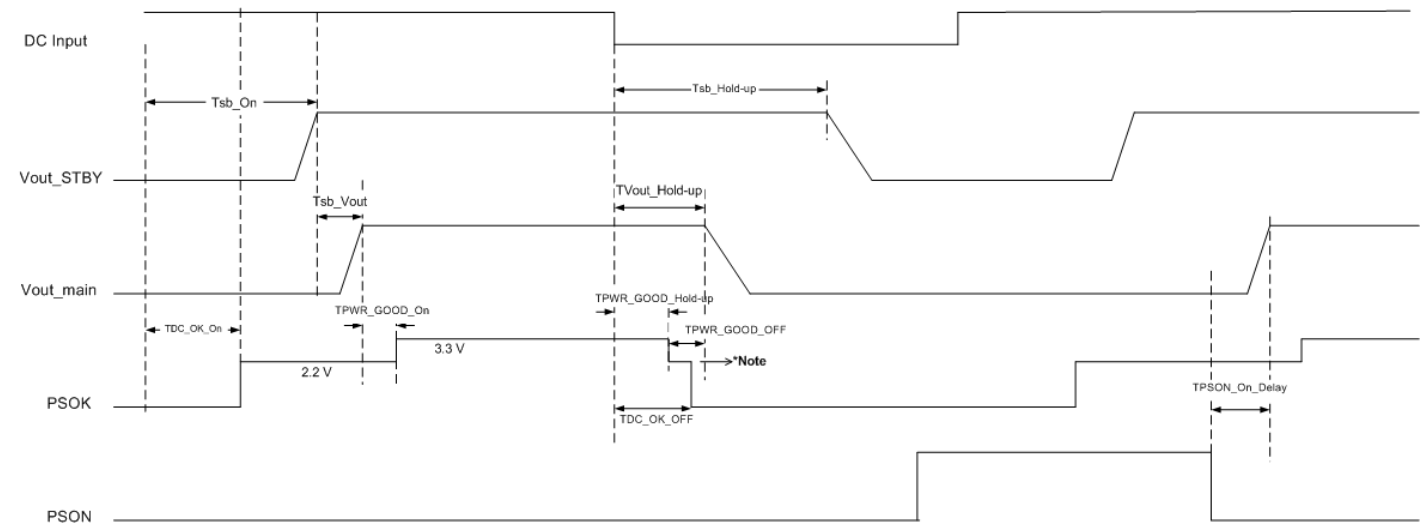
HEX Address Combinations by Analogue ADDR External Resistance Value

ADDR External Resistance to RTN/Ground (KΩ; ±5% Tolerance)	Power Module Secondary Main Controller (Serial Slave Address)	Power Module EEPROM (Serial Slave Address)
0.82	0xB0	0xA0
2.7	0xB2	0xA2
5.6	0xB4	0xA4
8.2	0xB6	0xA6
15	0xB8	0xA8
27	0xBA	0xAA
56	0xBC	0xAC
180	0xBE	0xAE

STATUS INDICATOR CONDITIONS

	LED State	Mode	Operating Condition
1.	Off	DC Turn-off	The incoming DC source is below the minimum power module turn-on specification
2.	Green – blinking 1Hz	Standby	The power module VStandby output is operating within normal parameters and main output is disabled
3.	Green – solid	Power-good	The power module VStandby & Main outputs are operating within normal parameters and delivering power
4.	Yellow – blinking 1Hz	Warning	A warning condition within the power supply has been detected
5.	Yellow – solid	Fault	A fault condition within the power supply has been detected.

TIMING DIAGRAM



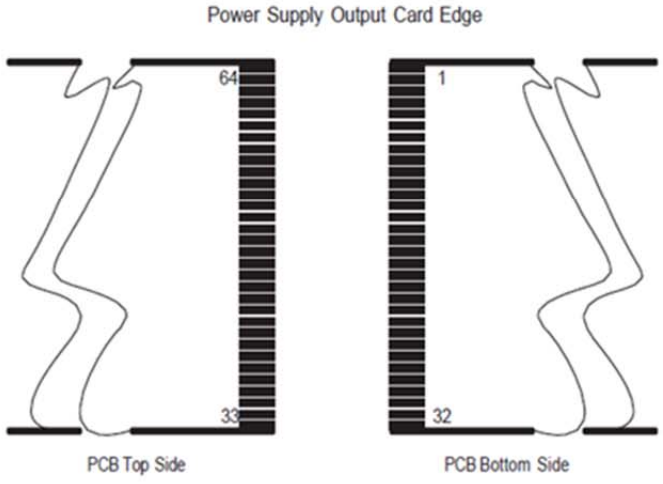
*NOTE: The PSOK levels after the loss of the incoming DC source may be either 1.1V or 2.2V depending on the relative timing of the TDCPOK_OFF and TPWRP_GOOD_HOLD-Up

TIMING SPECIFICATIONS

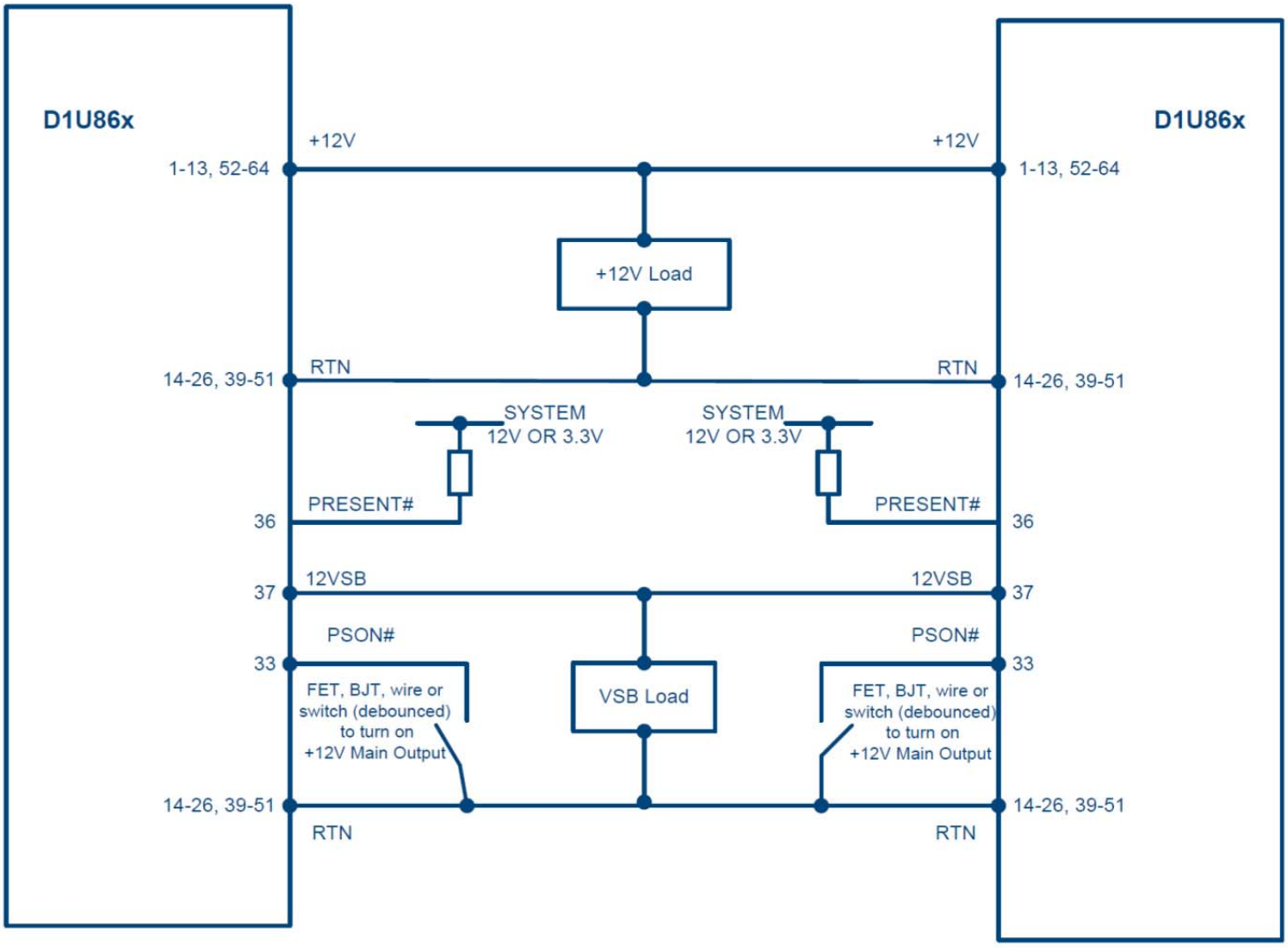
Parameter	Description	Min	Max	Unit
Tsb_On	Delay from DC being applied to standby output being within regulation	0	3000	ms
Tsb_Vout	Delay from standby output to main output voltage being within regulation	50	500	ms
TPWR_GOOD_On	Delay from output voltages within regulation limits to PWR_GOOD assertion	20	500	ms
TVout_Hold-up	Delay from loss of AC to main output being out of regulation	1		ms
Tsb_Hold-up	Delay from loss of AC to standby output being out of regulation	20	2000	ms
TPWR_GOOD_OFF	Delay from de-assertion of PWR_GOOD to output falling out of regulation	1		ms
TPSON_On_Delay	Delay from PSON assertion to output being within regulation	300	500	ms

OUTPUT AND SIGNAL SPECIFICATION

Pin#	Function	Pin Type	Description
14-26, 39-51	RTN	Power Ground	Power and Standby Return
1-13, 52-64	12V	Power	12V Output
37	12VSB	Power	12V Standby Output
38	PSINTERRUPT	Output	Active low; interrupt line for power supply fault & warning detection as per
36	PRESENT#	Input	Power Supply Present Signal (shortest
35	PSOK*	Analog output	Combination of their power supply output indicator signals: 1. DC input OK 2. Power Good 3. Power Supply Fault
34	ISHARE	Analog I/O	Analog representation of main output current. Typical analog voltage shall be 60.15mV/Amp of main output current.
33	PSON#	Input	Power Supply on/off control signal
32	SCL	Input	SMBus/PMBus Clock
31	SDA	I/O	SMBus/PMBus Data
30	GND	Analog I/O	Power Supply Signal Ground
29	N/A	N/A	Reserved; no User connection
28	N/A	N/A	Reserved; no User connection
27	ADDR	Analog input	PMBus Address



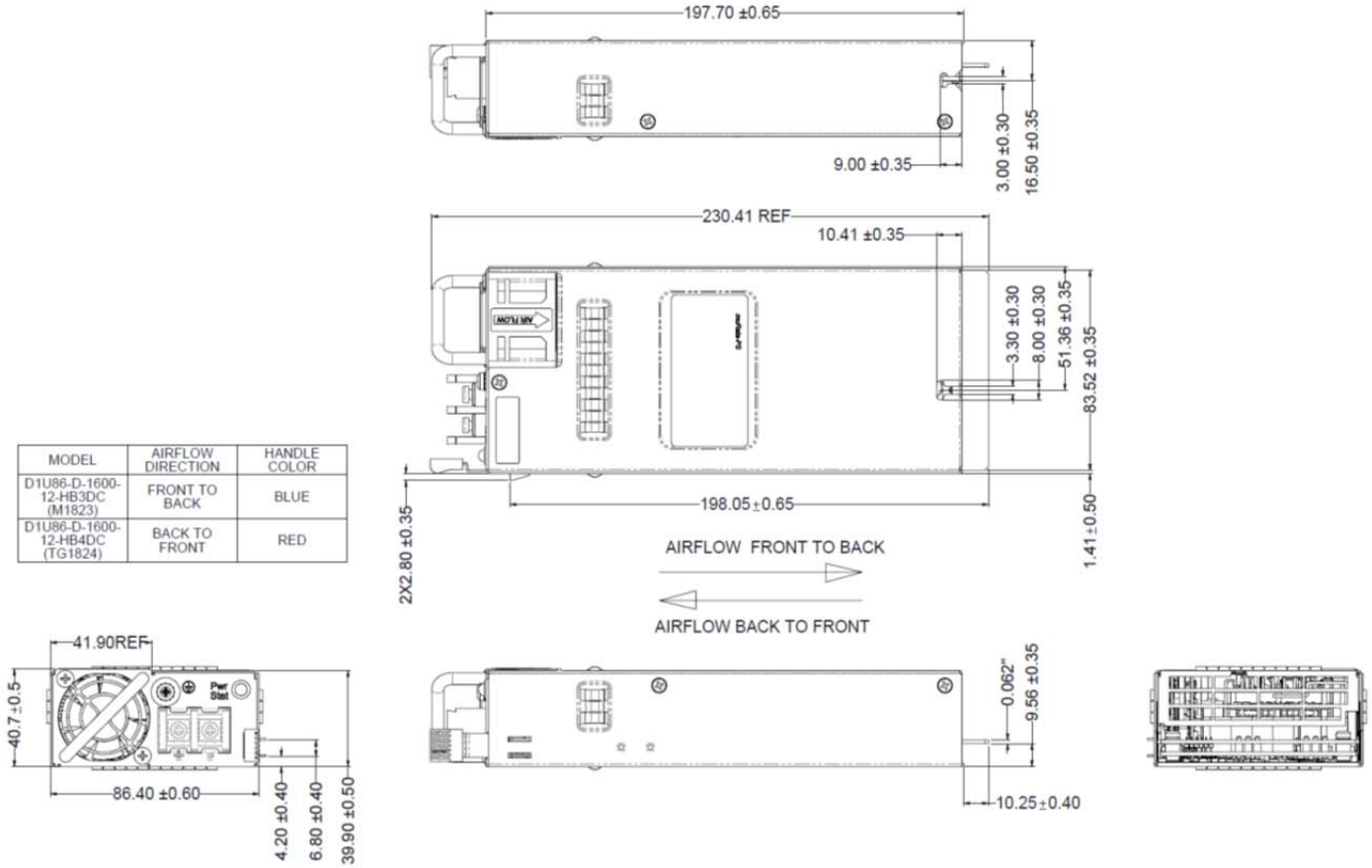
WIRING DIAGRAM FOR OUTPUT



CURRENT SHARING NOTES

Main Output: Current share is achieved using the droop method. Nominal output voltage (12.20V) is achieved at 50% load and output voltage changes at a rate of 3.10mv per amp. Startup of parallel power supplies is not internally synchronized. If more than 1600W combined power is needed, start-up synchronization must be provided by using a common PS_ON signal. To account for ±5% full load current sharing accuracy and the reduction in full load output voltage due to droop, available output power must be derated by 10% when units are operated in parallel. Internal ORing FETs are provided.
Standby output can be tied together for redundancy but total combined output power must not exceed 30W; Internal MOSFET ORing devices are used.

MECHANICAL DIMENSIONS



MODEL	AIRFLOW DIRECTION	HANDLE COLOR
D1U86-D-1600-12-HB3DC (M1823)	FRONT TO BACK	BLUE
D1U86-D-1600-12-HB4DC (TG1824)	BACK TO FRONT	RED

1. DC input connector: Terminal Block, Dinkle Enterprise: Part No. DT-7C-B14W-02
2. Dimensions: 3.4" x 7.75" x 1.59" [86mm x 196.85mm x 39.9mm]
3. This drawing is a graphical representation of the product and may not show all fine details.
4. Reference File: D1U86-D-1600-12-HBxDC (M1823-M1824)_Drawing for Product Datasheet_20160106.PDF

MATING CONNECTOR

Part Number	Description
FCI 10053363-200LF	Right Angle
FCI 10046971-008LF	Vertical

OPTIONAL ACCESSORIES

Description	Part Number
12V D1U86P Output Connector Card	D1U86P-12-CONC

APPLICATION NOTES

Document Number	Description
ACAN-50	D1U86P Output Connector Card: http://power.murata.com/datasheet?/data/apnotes/acan-50.pdf
ACAN-54	D1U86D Communication Protocol: http://power.murata.com/datasheet?/data/apnotes/acan-54.pdf

Murata Power Solutions, Inc.
11 Cabot Boulevard, Mansfield, MA 02048 -1151 U.S.A.
ISO 9001 and 14001 REGISTERED

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Refer to: http://www.murata-ps.com/requirements/

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