

PRODUCT OVERVIEW

The D1U86P-W-2200-12-HBxDC are highly efficient 2,226 watt, power factor corrected front end power supplies that provide a 12V Main and a 12V standby output. Multiple units can current share and be operated in parallel. The power supplies may be hot plugged and are protected from fault conditions such as overtemperature, overcurrent and overvoltage. Status is indicated by a front mounted multi-function LED in addition to logic signaling and may be monitored via PMBus™. The low profile 1U package and >52 W/cubic inch power density make them ideal for delivering reliable, efficient power to servers, workstations, storage systems and other 12V distributed power systems, whilst minimizing the number of required power modules.



ORDERING GUIDE

| Part Number | Main Power Output vs. AC Line | | | Output | Standby Output | Airflow |
|-------------------------------------|-------------------------------|--------------------|------------------------|--------|----------------|---------------|
| | 100-110V _{AC} | 120V _{AC} | 200-240V _{AC} | | | |
| D1U86P-W-2200-12-HB3DC | 1000W | 1150W | 2200W | 12V | 12V | Front to Back |
| D1U86P-W-2200-12-HB4DC ¹ | | | | | | Back to Front |

¹ Please contact Murata for availability

FEATURES

- 2226W total output power
- >94% minimum efficiency at 50% load
- 12V main output
- 12V 30W standby output
- 1U height: 3.4" x 7.78" x 1.59" (86.4mm x 197.7mm x 40.5mm)
- >52 Watts per cubic inch density
- N+1 redundancy, including hot plugging
- Droop current sharing with internal ORing /isolation circuit, both outputs
- Overvoltage, overcurrent, overtemperature protection
- Internal cooling fan (variable speed)
- PMBus™/I2C interfaces monitoring and control
- RoHS compliant
- Two Year Warranty

INPUT CHARACTERISTICS

| Parameter | Conditions | Min. | Nom. | Max. | Units |
|---|--|------|---------|------|-----------------|
| Input Voltage Operating Range | | 90 | 115/230 | 264 | V _{AC} |
| Frequency | | 47 | 50/60 | 63 | Hz |
| Turn-on Voltage | Ramp up | 81 | | 89 | V _{AC} |
| Turn-off Voltage | Ramp down | 70.5 | 73 | 78 | V _{AC} |
| Maximum Input Current | 100-110V, 120V, 200-240V | | | 12.0 | Arms |
| Inrush Current | At 264V _{AC} at 25°C cold start | | | 50 | Apk |
| Power Factor | At 230V _{AC} , half load | | 0.98 | | |
| Efficiency (230V _{AC}) excluding fan load | 20% load | 90 | | | % |
| | 50% load | 94 | | | % |
| | 100% load | 91 | | | % |

Note: Front-Back variant 80+ certified

OUTPUT VOLTAGE CHARACTERISTICS

| Output Voltage | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|---------------------------------------|------------------------|-------|-------|--------|-----------------|
| 12V | Voltage Set Point | 50% load | 12.17 | 12.20 | 12.23 | V _{DC} |
| | Line and Load Regulation | | 11.60 | | 12.80 | |
| | Ripple Voltage & Noise ¹ | 20MHz Bandwidth | | | 120 | mV p-p |
| | Output Current (230 V _{AC}) | | 0 | | 183 | A |
| | Output Current (120 V _{AC}) | | 0 | | 95 | A |
| | Output Current (100 V _{AC}) | | 0 | | 83 | A |
| | Load Capacitance | | | | 10,000 | µF |
| 12VSB | Voltage Set Point | 50% load | 11.97 | 12.0 | 12.02 | V _{DC} |
| | Ripple Voltage & Noise ¹ | 20MHz Bandwidth | | | 120 | mV p-p |
| | Output Current | 100-240V _{AC} | 0 | | 2.5 | A |

¹Ripple and noise measured with a parallel combination of a 1.0µF ceramic and 10µF tantalum capacitor on each of the power module outputs. A short coaxial cable connected directly to the input of a scope is required.



Available now at:
www.murata-ps.com/en/3d/acdc.html

For full details go to
www.murata-ps.com/rohs



Test Certificate and Test Report

www.murata-ps.com/support

OUTPUT CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|--|------|-----------|---------|-------|
| Output Rise Monotonicity | No voltage excursion; linear slope | | | | |
| Startup Time | AC ramp up | | 1.5 | 3 | s |
| Transient Response | 12V, 50% load step, 1.0A μ s di/dt, 5A min. load | | \pm 600 | | mV |
| | 12VSB, 50% load step, 1.0A μ s di/dt | | \pm 600 | | |
| Current sharing accuracy | At 100% load | | | \pm 7 | % |
| Hot Swap Transients | All outputs remain in regulation | | | 5 | % |
| Holdup Time | At full load | 12 | | | ms |

ENVIRONMENTAL CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|--|------|------|-----------|-----------|
| Storage Temperature Range | | -40 | | 70 | °C |
| Operating Temperature Range | | 0 | | 50 | |
| Operating Humidity | Noncondensing | 5 | | 90 | % |
| Storage Humidity | | 5 | | 95 | |
| Altitude (without derating at 45°C) | | 3000 | | | m |
| Shock | 30G non-operating | | | | |
| Vibration | 10-500Hz, 0.5G (non-operational) | | | | |
| MTBF (Target) | Per Telcordia SR-322 M1C1 @ 40°C | 559K | | | hrs |
| Acoustic | | | | 65 | dB(A)/@1m |
| Safety Approvals | CAN/CSA C22.2 No 60950-1-07, Am.1:2011, Am 2:2014 ANSI/UL 60950-1-2014 IEC60950-1:2005 (2nd Ed.), Am 1:2009 + Am 2:2013 EN 60950-1:2006+A11:2009 +A1:2010 +A12:2011 +A2:2013 CQC GB4943.1-2011; GB9254-1-2008; GB17625, 1-2012 | | | | |
| Input Fuse | Power Supply has internal 16A/250V fast blow fuse on the AC line input. | | | | |
| Weight | | | | 2.54/1.15 | lbs/Kg |

PROTECTION CHARACTERISTICS

| Output Voltage | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|---|---|------|------|------|-------|
| | Overtemperature (intake) – to be verified | An OTP warning shall be issued via the PMBus™ interface when the air inlet exceeds 60°C; however the power module shall not shut down until critical internal hotspot temperatures are exceeded. | | 60 | | °C |
| 12V | Overvoltage | Latching | 13.2 | | 14.4 | V |
| | Overcurrent at 230V _{AC} | Shutdown of the output followed by auto- recovery after one second. The output shall attempt three such auto-recovery attempts and then enter a permanent latched state. Recovery of the permanent latched state shall require cycling of the incoming AC source or toggling of the PSON# signal. | 192 | | 210 | A |
| | Overcurrent at 108 - 120V _{AC} | | 100 | | 115 | |
| | Overcurrent at 90 - 108V _{AC} | | 87 | | 96 | |
| 12VSB | Overvoltage | Latching | 13.2 | | 14.4 | V |
| | Overcurrent | Auto-recovery | 2.75 | | 3.3 | A |

ISOLATION CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---------------------------------------|------|------|------|-----------------|
| Insulation Safety Rating / Test Voltage | Input to Output - Reinforced | 3000 | | | Vrms |
| | Input to Chassis - Basic | 1500 | | | Vrms |
| Isolation | Output to Chassis | 500 | | | V _{DC} |
| Leakage Current | 1.5mA at 264V _{AC} , 50/60Hz | | | | |

EMISSIONS AND IMMUNITY

| Characteristic | Standard | Compliance & Conditions |
|------------------------------------|-------------------------------------|---|
| Input Current Harmonics | IEC/EN 61000-3-2 | Complies |
| Voltage Fluctuation and Flicker | IEC/EN 61000-3-3 | Complies |
| Conducted Emissions | FCC 47 CFR Part 15/CISPR 22/EN55022 | Class A, 6dB margin |
| ESD Immunity | IEC/EN 61000-4-2 | Level 3 criteria A |
| Radiated Field Immunity | IEC/EN 61000-4-3 | Level 3 criteria B |
| Electrical Fast Transient Immunity | IEC/EN 61000-4-4 | Level 3 criteria A; 2kV, 12V Main load 48A, 12V standby load 1.2A |
| Surge Immunity | IEC/EN 61000-4-5 | Level 3 criteria A: ¹ CM: 2kV, 2ohm line impedance, 50A load main output, 1.2A Standby load ¹ DM: 1kV 2 ohm line impedance, 50A load main output, 1.2A Standby load |
| Radiated Field Conducted Immunity | IEC/EN 61000-4-6 | Level 3 criteria A |
| Magnetic Field Immunity | IEC/EN 61000-4-8 | 3 A/m criteria A |
| Voltage dips, interruptions | IEC/EN 61000-4-11 | 230V _{in} , 100% load, Phase 0°, Dip 100% Duration 10ms (A) 230V _{in} , 50% load, Phase 0°, Dip 100% Duration 20ms (VSB:A, V1:A) 230V _{in} , 100% load, Phase 0°, Dip 100% Duration > 20ms (VSB, V1:B) |

¹ Impedance is 2 ohms for ±2kV common mode and ±1kV differential model to comply with Nebs GR-1089 limits, Maximum load capacitance is required for these tests.

STATUS AND CONTROL SIGNALS

| Signal Name | I/O | Description | Interface Details | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------------|------------|--|------------------------------------|---------------------------|----------------|--|--|--|------------------------|--|--|------|--|----------------|---------|------------|---------|-------|---------------------------|---|---|---|----------------------|----------|-----|---|---|---|-------|---------|-----------|---|---|---|-------|---------|---------|---|---|---|------------------|---------|------------|---|---|---|----------------------|----------|----------|---|
| PSOK (Output OK) | Output | <p>The PSOK output is a logical “OR” of three internal signals; however the output is not strictly a “digital” signal that transitions between “low” and “high” but is analogue in nature. The internal logic signals are as follows:</p> <ol style="list-style-type: none"> AC_OK_H PWR_GOOD_H FAULT_L <p>The following is a “truth table” that shows the analogue levels of operation of the signal dependent upon the three internal logic signals:</p> <table border="1"> <thead> <tr> <th colspan="6">PSOK TRUTH TABLE VS. ANALOG OUTPUT</th> </tr> <tr> <th colspan="3">INTERNAL LOGIC SIGNALS</th> <th colspan="2">PSOK</th> <th rowspan="2">OPERATION MODE</th> </tr> <tr> <th>AC_OK_H</th> <th>PWR_GOOD_H</th> <th>FAULT_L</th> <th>LEVEL</th> <th>LIMITS (V_{DC})</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> <td>≤ 0.6V_{DC}</td> <td>0 to 0.6</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>(1/3)</td> <td>1.030 -</td> <td>Power Off</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>(2/3)</td> <td>2.127 –</td> <td>Standby</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>VDD¹</td> <td>3.186 –</td> <td>Power Good</td> </tr> <tr> <td>X</td> <td>X</td> <td>0</td> <td>≤ 0.6V_{DC}</td> <td>0 to 0.6</td> <td>PS Fault</td> </tr> </tbody> </table> <p>¹ VDD = 3.3V_{DC}</p> <p>The timing relationship of this signal is shown in the Timing Specification section that follows.</p> | PSOK TRUTH TABLE VS. ANALOG OUTPUT | | | | | | INTERNAL LOGIC SIGNALS | | | PSOK | | OPERATION MODE | AC_OK_H | PWR_GOOD_H | FAULT_L | LEVEL | LIMITS (V _{DC}) | 0 | 0 | 1 | ≤ 0.6V _{DC} | 0 to 0.6 | Off | 0 | 1 | 1 | (1/3) | 1.030 - | Power Off | 1 | 0 | 1 | (2/3) | 2.127 – | Standby | 1 | 1 | 1 | VDD ¹ | 3.186 – | Power Good | X | X | 0 | ≤ 0.6V _{DC} | 0 to 0.6 | PS Fault | <p>The PSOK Signal is provided with a buffered output that is driven from a DAC within the secondary microprocessor.</p> <p>The output impedance is 1K15 ohms</p> |
| PSOK TRUTH TABLE VS. ANALOG OUTPUT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INTERNAL LOGIC SIGNALS | | | PSOK | | OPERATION MODE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AC_OK_H | PWR_GOOD_H | FAULT_L | LEVEL | LIMITS (V _{DC}) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | ≤ 0.6V _{DC} | 0 to 0.6 | Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | (1/3) | 1.030 - | Power Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | (2/3) | 2.127 – | Standby | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | VDD ¹ | 3.186 – | Power Good | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | X | 0 | ≤ 0.6V _{DC} | 0 to 0.6 | PS Fault | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

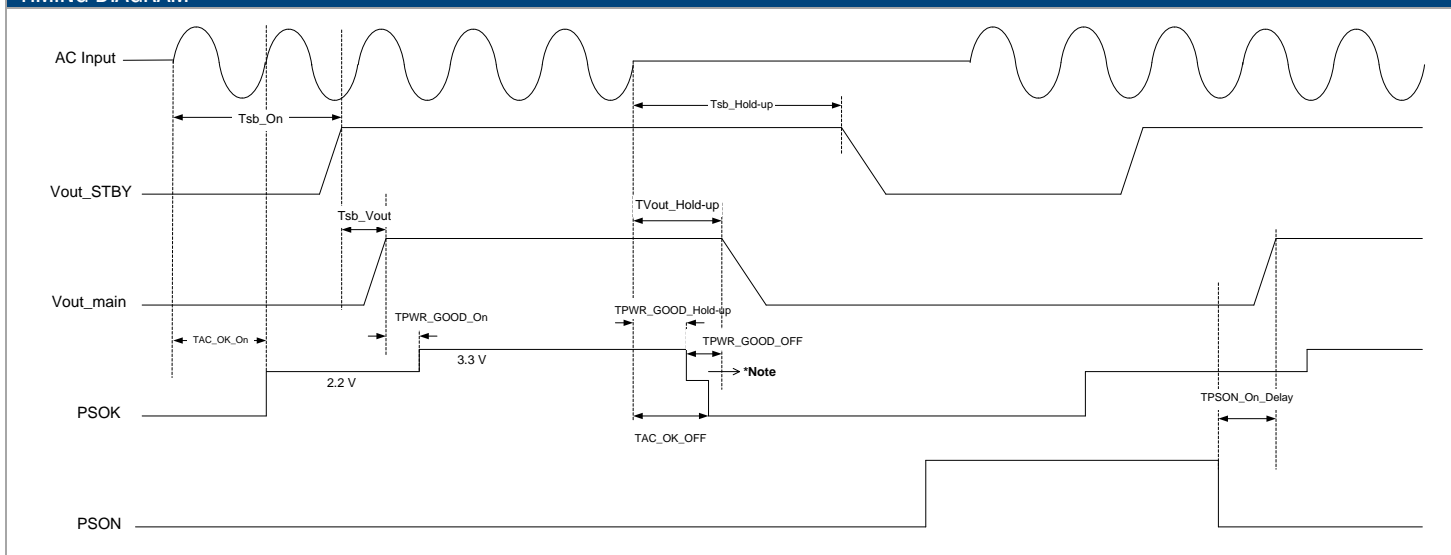
STATUS AND CONTROL SIGNALS cont'd

| Signal Name | I/O | Description | Interface Details |
|--|------------------------|--|--|
| PS_INTERRUPT (FAULT/WARNING) | Output | The signal output is driven low to indicate that the power supply has detected a warning or fault and is intended to alert the system. This output must be driven high when the power is operating correctly (within specified limits). The signal will revert to a high level when the warning/fault stimulus (that caused the alert) is removed. | Pulled up internally via 10K to 3.3V _{DC} . A logic high >2.0V _{DC} A logic low <0.8V _{DC} Driven low by internal buffer (open drain output). |
| PRESENT# | Output | Based on the industry standard Common Slot requirement this signal is used to detect the presence of an (installed) power module within the host system. However it is also intended to “Enable” the Main 12V _{DC} output. The signal is also designed to control the power module during hot plug insertion/extraction in conjunction with the host system and is provided on a short “last to make; first to break” signal pin. To “enable” the Main 12V _{DC} output the signal requires to be pulled “high” with respect +12V_GND. The value of the pull up resistor is as follows: 1. If the signal is to be pulled up to the 12VSB output then the resistor value should be 21KΩ 2. If the signal is to be pulled up to a 3.3V _{DC} rail (locally derived within the host system) then the resistor value should be 5.11KΩ | The voltage level on the system side of the PSPRESENT# signal will be follows: 1. When the power module is not installed the voltage will equal the rail to which it is pulled up to (3.3V _{DC} or 12V _{DC}) 2. When the power module is installed, the voltage will be pulled down to 0.54V _{DC} ±5%. |
| PS_ON (Power Supply Enable/Disable) | Input | The PS_ON can be permanently connected to +12V_GND (via the host system mid/back plane) to “enable” the Main 12V _{DC} output. Alternatively the signal can be connected via the host system electronics to provide the ability to switch between “enable/disable” states. The signal is pulled up internally to the internal housekeeping supply (within the power supply). The power supply main 12V _{DC} output will be enabled when this signal is pulled low to +12V_GND. In the low state the signal input shall source a nominal 1.2mA _{DC} . The 12V _{DC} output will be disabled when the input is driven higher than 2.4V, or open circuited. Cycling this signal shall clear latched fault conditions. | Pulled up internally via 10K to 3.3V _{DC} . A logic high >2.0V _{DC} A logic low <0.8V _{DC} Input is via CMOS Schmitt trigger buffer. |
| V1_SENSE V1SENSE_R | Input | Remote sense connections are intended to be connected and sense the voltage at the point of load. The voltage sense will interact with the internal module regulation loop to compensate for voltage drops due to connection resistance between the output connector and the load. If remote sense compensation is not required then the voltage can be configured for local sense by: • V1_SENSE directly connected to any of the 12V output pins 1-13, 52-64 • V1_SENSE_R directly connected to any of the RTN pins 14-26, 39-51 | Compensation for up to 0.12Vdc total connection drop (output and return connections). |
| ADDR (Address Select) | Input | An analogue input that is used to set the address of the internal slave devices (EEPROM and microprocessor) used for digital communications. Connection of a suitable resistor to +12V_GND, in conjunction with an internal resistor divider chain, will configure the required address . | DC voltage between the limits of 0 and +3.3V _{DC} . |
| SCL (Serial Clock) | Both | A serial clock line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. No additional internal capacitance is added that would affect the speed of the bus. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered. | VIL is 0.8V maximum VOL is 0.4V maximum when sinking 3mA VIH is 2.1V minimum |
| SDA (Serial Data) | Both | A serial data line compatible with PMBus™ Power Systems Management Protocol Part 1 – General Requirements Rev 1.1. The signal is provided with a series isolator device to disconnect the internal power supply bus in the event that the power module is unpowered. | VIL is 0.8V maximum VOL is 0.4V maximum when sinking 3mA VIH is 2.1V minimum |

STATUS INDICATOR CONDITIONS

| LED State | Mode | Operating Condition |
|--------------------------|-------------|---|
| 1. Off | AC Turn-off | The incoming AC source is below the minimum power module turn-on specification |
| 2. Green – blinking 1Hz | Standby | The power module VStandby output is operating within normal parameters and main |
| 3. Green – solid | Power-good | The power module VStandby & Main outputs are operating within normal parameters |
| 4. Yellow – blinking 1Hz | Warning | A warning condition within the power supply has been detected |
| 5. Yellow – solid | Fault | A fault condition within the power supply has been detected. |

TIMING DIAGRAM



*NOTE: The PSOK levels after the loss of the incoming AC source may be either 1.1V or 2.2V depending on the relative timing of the TACPOK_OFF and TPWR_GOOD_HOLD-UP

Link back to [Status and Control Signals](#)

TIMING SPECIFICATIONS

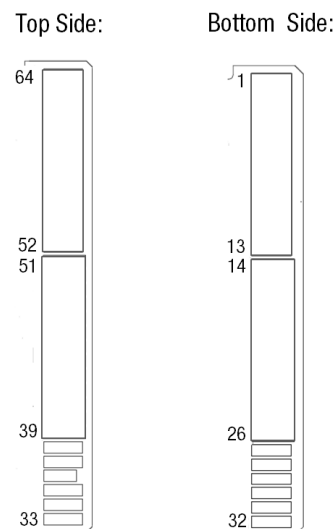
| Parameter | Description | Min | Max | Unit |
|-------------------|---|-----|------|------|
| Tsb_On | Delay from AC being applied to standby output being within regulation | 0 | 3000 | ms |
| Tsb_Vout | Delay from standby output to main output voltage being within regulation | 50 | 500 | ms |
| TPWR_GOOD_On | Delay from output voltages within regulation limits to internal PWR_GOOD_H assertion | 20 | 500 | ms |
| TAC_OK_OFF | Delay from loss of AC to de-assertion of AC_OK_H internal signal (100% load) | 2 | 10 | ms |
| TAC_OK_On | Delay from AC being applied to assertion of AC_OK_H internal signal | 1 | 3000 | ms |
| TPWR_GOOD_Hold-up | ¹ Delay from loss of AC to de-assertion of PWR_GOOD_H internal signal | 7 | 60 | ms |
| TVout_Hold-up | Delay from loss of AC to main output being out of regulation | 12 | - | ms |
| Tsb_Hold-up | Delay from loss of AC to standby output being out of regulation | 20 | 2000 | ms |
| TPWR_GOOD_OFF | Delay from de-assertion of PWR_GOOD_H internal signal to output falling out of regulation | 0 | 2 | ms |
| TPSON_On_Delay | Delay from PSON assertion to output being within regulation | 1 | 200 | ms |

¹ 100% full load

OUTPUT CONNECTOR AND SIGNAL SPECIFICATION

| Pin# | Function | Pin Type | Description |
|--------------|-----------------------------|---------------|---|
| 14-26, 39-51 | RTN | Power Ground | Power and Standby Return |
| 1-13, 52-64 | 12V | Power | 12V Output |
| 37 | 12VSB | Power | 12V Standby Output |
| 38 | PSINTERRUPT | Output | Active low; interrupt line for power supply fault & warning detection as per PMBus™ spec |
| 36 | PRESENT# | Input | Power Supply Present Signal (shortest pin) |
| 35 | PSOK | Analog output | Combination of three internal power supply indicator signals: 1. ACOK_H 2. PWOK_H 3. FAULT_L |
| 34 | N/A | N/A | Reserved; no user connection |
| 33 | PSON# | Input | Power Supply on/off control signal |
| 32 | SCL | Input | SMBus/PMBus™ Clock |
| 31 | SDA | I/O | SMBus/PMBus™ Data |
| 30 | GND | Analog I/O | Power Supply Signal Ground |
| 29 | 12V SENSE R | Input | Compensation for voltage drops due to connection resistance between the output connector and the load |
| 28 | 12V SENSE | | |
| 27 | ADDR | Analog input | PMBus™ Address see value table |

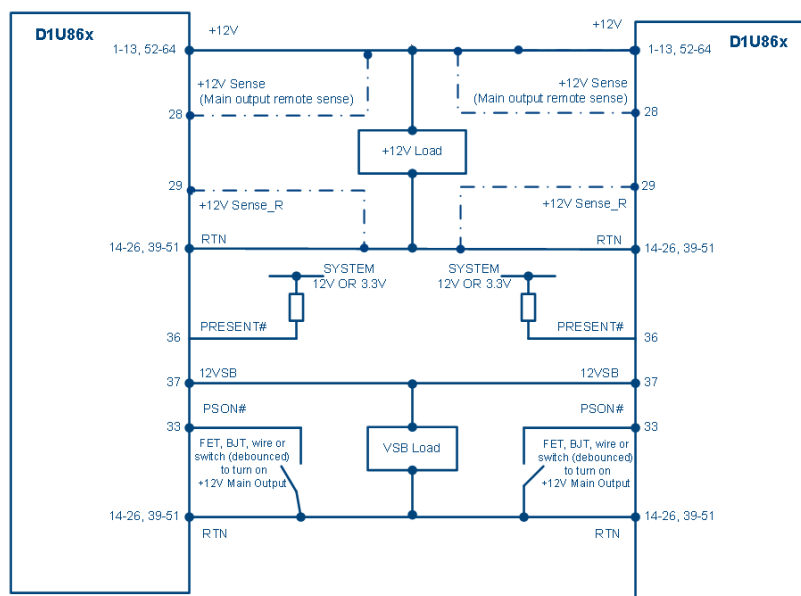
Power Supply Output Card Edge



MATING CONNECTOR

| Part Number | Description |
|--------------------|-------------|
| FCI 10053363-200LF | Right Angle |
| FCI 10046971-001LF | Vertical |


WIRING DIAGRAM FOR FOR OUTPUT




CURRENT SHARING NOTES

- 12V Output: Current sharing is achieved using droop share method.
- 12VSB Outputs can be tied together for redundancy however the combined output power must not exceed the rated standby power of a single unit.
- 12VSB Output has an internal ORing MOSFET for additional redundancy and fault tolerance.
- The load for both the main 12V and the 12VSBY outputs during startup shall not be allowed to exceed the capability of a single unit. Higher load current may be applied after a delay of 3sec (minimum) to allow all sharing units to achieve steady state regulation.

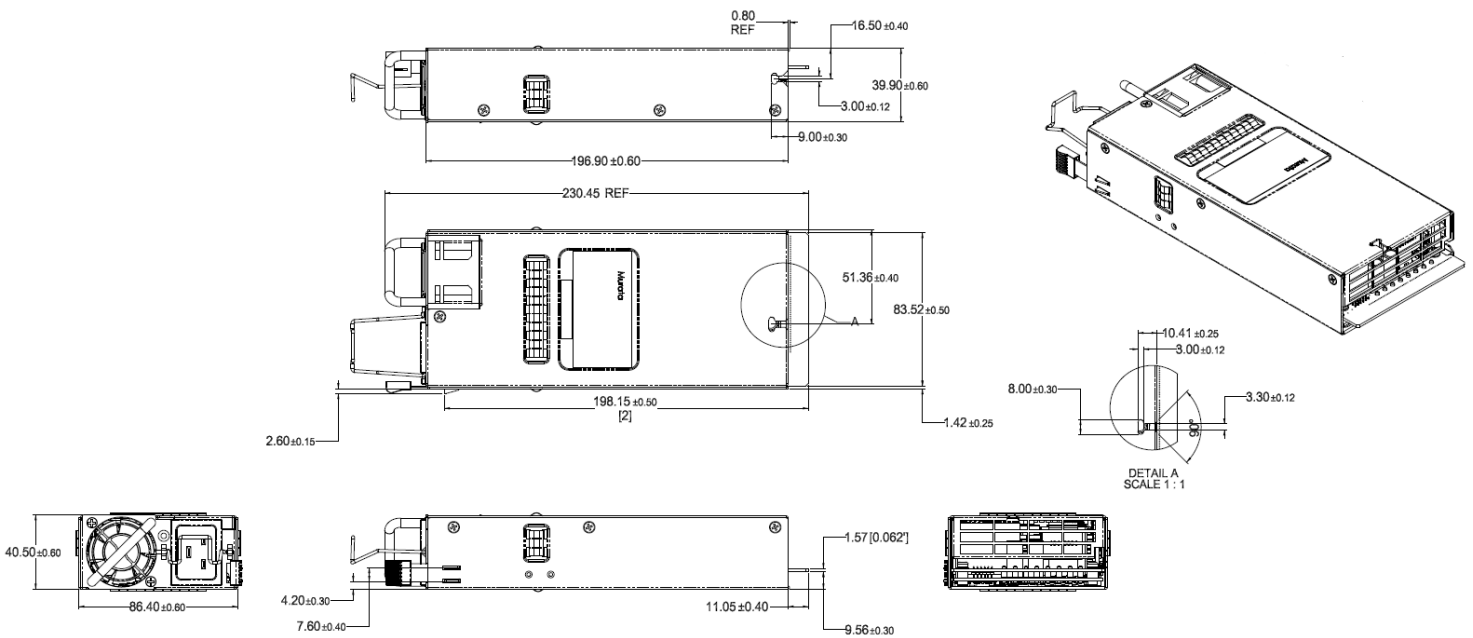
MECHANICAL DIMENSIONS



 D1U86P-W-2200-12-HB3DC – Airflow Front to Back



 D1U86P-W-2200-12-HB4DC – Airflow Back to Front



Notes

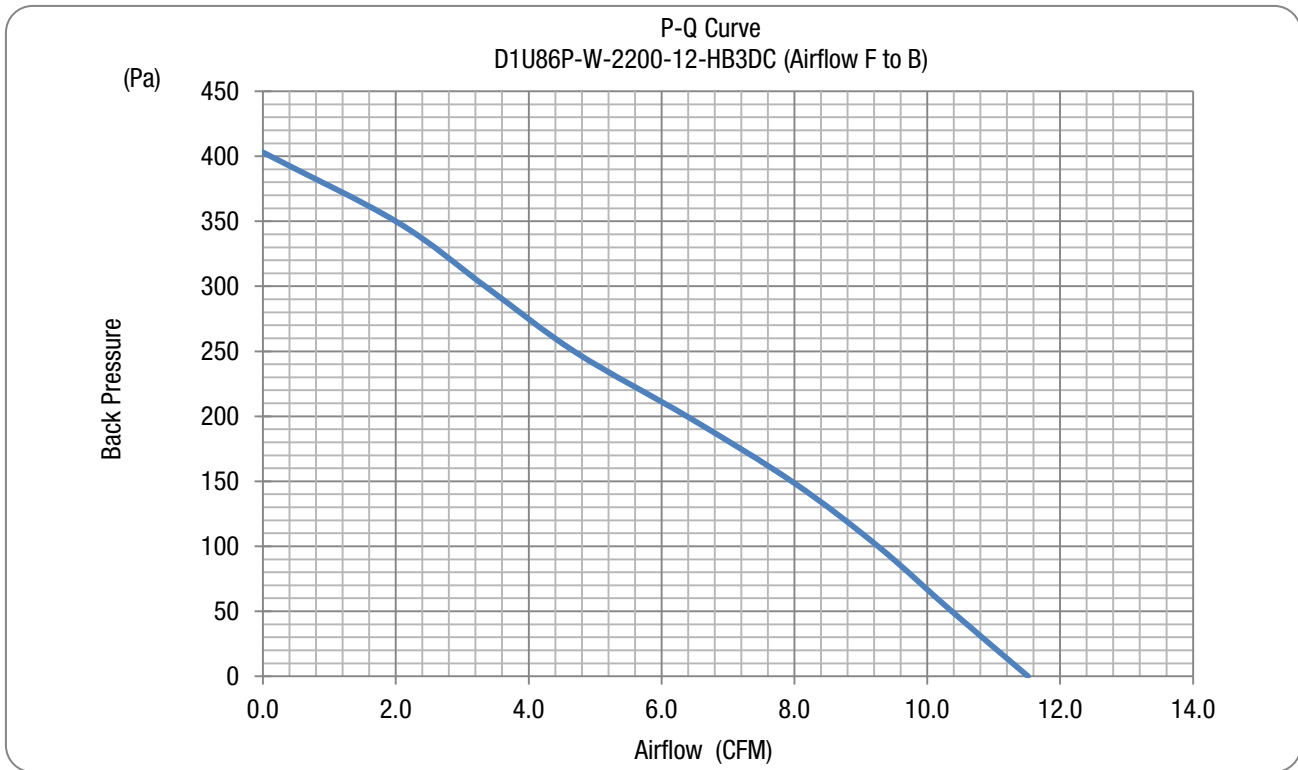
1. AC input connector: IEC 60320-C20
2. Dimensions: 86.4 mm x 197.7mm x 40.5mm [3.4" x 7.78" x 1.59"]; metric measurements take precedent
3. This drawing is a graphical representation of the product and may not show all fine details.
4. Reference File: I:\Eng_wip\UserPDDwg\1830\D1U86P-W-2200-12-HB3C_M1830-260CT17
5. Dimensions in mm unless otherwise noted
6. For illustration purposes of the envelope and main features only. Refer to 3D model should additional detail be required.

ADDR ADDRESS SELECTION

| ADDR pin resistor to GND (K-ohm, ±5%) | Power Supply Main Controller (Serial Communications Slave Address) | Power Supply External EEPROM (Serial Communications Slave Address) |
|--|---|---|
| 0.82 | 0xB0 | 0xA0 |
| 2.7 | 0xB2 | 0xA2 |
| 5.6 | 0xB4 | 0xA4 |
| 8.2 | 0xB6 | 0xA6 |
| 15 | 0xB8 | 0xA8 |
| 27 | 0xBA | 0xAA |
| 56 | 0xBC | 0xAC |
| 180 | 0xBE | 0xAE |

Link Back to [Status and Control Signals, Pinout Table](#)

Airflow Characteristics



OPTIONAL ACCESSORIES

| Description | Part Number |
|----------------------------------|-------------------|
| 12V D1U86P Output Connector Card | D1U86P-CONC-2200W |

APPLICATION NOTES

| Document Number | Description | Link to Document |
|-----------------|--------------------------------------|---|
| ACAN-75 | D1U86P Output Connector Card | http://power.murata.com/datasheet?/data/apnotes/acan-75.pdf |
| ACAN-76 | D1U86P-W-2200 Communication Protocol | http://power.murata.com/datasheet?/data/apnotes/acan-76.pdf |

[Back to introduction](#)

MPS part number Guide:

| Product | Internal MPS# |
|------------------------|---------------|
| D1U86P-W-2200-12-HB3DC | M1830 |
| D1U86P-W-2200-12-HB4DC | M2000 |
| D1U86P-CONC-2200W | M7018 |

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ISO 9001 and 14001 REGISTERED

This product is subject to the following operating requirements and the Life and Safety Critical Application Sales Policy:

Refer to: <http://www.murata-ps.com/requirements/>

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