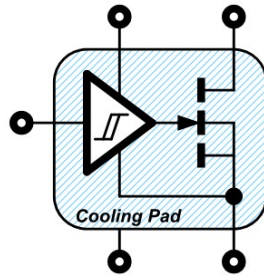


GaNFast™ Power IC



QFN 6 x 8 mm



Simplified schematic

1. Features

GaNFast™ Power IC

- Thermally enhanced version of NV6115
- Large cooling pad
- Enhanced thermals when using CS resistor
- Monolithically-integrated gate drive
- Wide V_{CC} range (10 to 30 V)
- Programmable turn-on dV/dt
- 200 V/ns dV/dt immunity
- 800 V Transient Voltage Rating
- 650 V Continuous Voltage Rating
- Low 175 m Ω resistance
- Zero reverse-recovery charge
- ESD Protection – 2,000 V (HBM), 1,000 V (CDM)
- 2 MHz operation

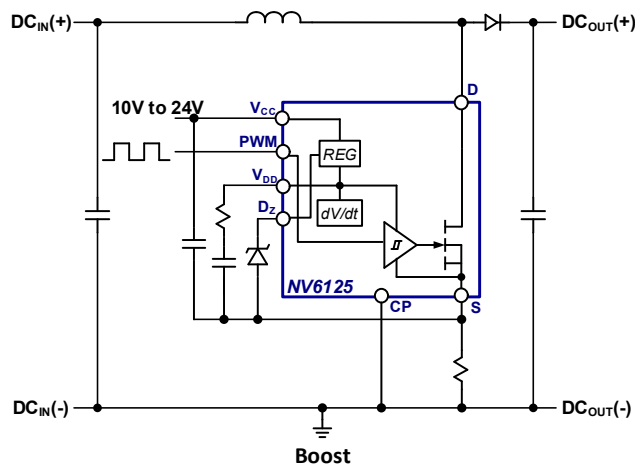
Small, low-profile SMT QFN

- 6 x 8 mm footprint, 0.85 mm profile
- Minimized package inductance

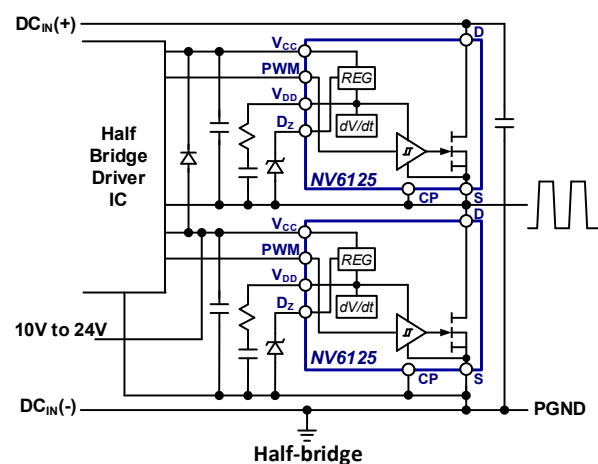
Environmental

- RoHS, Pb-free, REACH-compliant

4. Typical Application Circuits



Boost



Half-bridge

2. Description

The NV6125 is a thermally enhanced version of the popular NV6115 GaNFast™ power IC, optimized for high-frequency and soft-switching topologies.

Monolithic integration of FET, drive and logic creates an easy-to-use ‘digital-in, power-out’ high-performance powertrain building block, enabling designers to create the fastest, smallest, most efficient integrated powertrain in the world.

The highest dV/dt immunity, high-speed integrated drive and industry-standard low-profile, low-inductance, 6 x 8 mm SMT QFN package allow designers to exploit Navitas GaN technology with simple, quick, dependable solutions for breakthrough power density and efficiency.

Navitas’ GaNFast™ power ICs extend the capabilities of traditional topologies such as flyback, half-bridge, resonant, etc. to MHz+ and enable the commercial introduction of breakthrough designs.

3. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- Buck, boost, half bridge, full bridge
- Active Clamp Flyback, LLC resonant, Class D
- Quasi-Resonant Flyback
- Mobile fast-chargers, adapters
- Notebook adaptors
- LED lighting, solar micro-inverters
- TV / monitor, wireless power
- Server, telecom & networking SMPS

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6. Specifications

6.1. Absolute Maximum Ratings⁽¹⁾

(with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{DS} (TRAN)	Transient Drain-to-Source Voltage ⁽²⁾	800	V
V_{DS} (CONT)	Continuous Drain-to-Source Voltage	-7 to +650	V
V_{CC}	Supply Voltage	30	V
V_{PWM}	PWM Input Pin Voltage	-3 to +30	V
V_{DZ}	V_{DD} Setting Pin Voltage	6.6	V
V_{DD}	Drive Supply Voltage	7.2	V
V_{CP}	Cooling Pad Voltage	-10 to +10	V
I_D	Continuous Drain Current (@ $T_C = 100^\circ\text{C}$)	8	A
I_D PULSE	Pulsed Drain Current (10 μs @ $T_J = 25^\circ\text{C}$)	16	A
I_D PULSE	Pulsed Drain Current (10 μs @ $T_J = 125^\circ\text{C}$)	12	A
dV/dt	Slew Rate on Drain-to-Source	200	V/ns
T_J	Operating Junction Temperature	-55 to 150	$^\circ\text{C}$
T_{STOR}	Storage Temperature	-55 to 150	$^\circ\text{C}$

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) V_{DS} (TRAN) allows for surge ratings during non-repetitive events that are < 100 μs (for example start-up, line interruption) and repetitive events that are < 100 ns (for example repetitive leakage inductance spikes). Refer to Section 8.10 for detailed recommended design guidelines.

6.2. Recommended Operating Conditions⁽³⁾

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DZ}	Drive Supply Set Zener Voltage ⁽⁴⁾	5.8	6.2	6.6	V
V_{DD}	Drive Supply Voltage	5.5		7.0	V
I_{DD_EXT}	Regulator External Load Current			3.0	mA
R_{DD}	Gate Drive Turn-On Current Set Resistance ⁽⁵⁾	10	25		Ω
V_{PWM}	PWM Input Pin Voltage	0	5	Min. of (V_{CC} or 20)	V
V_{CC}	Supply Voltage	10		24	V
T_C	Operating Case Temperature	-40		125	$^\circ\text{C}$

(3) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

(4) Use of Zener diode other than 6.2 V is not recommended. See Table I for recommended part numbers of 6.2 V Zener diodes.

(5) R_{DD} resistor must be used. Minimum 10 Ohm to ensure application and device robustness.

6.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JS-001-2014)	2,000	V
CDM	Charged Device Model (per JS-002-2014)	1,000	V

6.4. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}^{(6)}$	Junction-to-Case	1.9	°C/W
$R_{\theta JA}^{(6)}$	Junction-to-Ambient	40	°C/W

(6) R_{θ} measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

6.5. Electrical Characteristics

Typical conditions: $V_{DS} = 400\text{ V}$, $V_{CC} = 15\text{ V}$, $V_{DZ} = 6.2\text{ V}$, $F_{SW} = 1\text{ MHz}$, $T_{AMB} = 25\text{ °C}$, $I_D = 4\text{ A}$, $R_{DD} = 10\text{ }\Omega$ (or specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} Supply Characteristics						
I_{QCC}	V_{CC} Quiescent Current		0.85	1.5	mA	$V_{PWM} = 0\text{ V}$
I_{QCC-SW}	V_{CC} Operating Current		2.3		mA	$F_{SW} = 1\text{ MHz}$, $V_{DS} = \text{Open}$
Low-Side Logic Input Characteristics						
V_{PVMH}	Input Logic High Threshold (rising edge)			4	V	
V_{PVML}	Input Logic Low Threshold (falling edge)	1			V	
V_{I-HYS}	Input Logic Hysteresis		0.5		V	
T_{ON}	Turn-on Propagation Delay		11		ns	Fig.1, Fig.2
T_{OFF}	Turn-off Propagation Delay		9		ns	Fig.1, Fig.2
T_R	Drain rise time		6		ns	Fig.1, Fig.2
T_F	Drain fall time		3		ns	Fig.1, Fig.2
Switching Characteristics						
F_{SW}	Switching Frequency			2	MHz	
t_{PW}	Pulse width	0.02		1000	μs	
GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.2	25	μA	$V_{DS} = 650\text{ V}$, $V_{PVM} = 0\text{ V}$
I_{DSS}	Drain-Source Leakage Current		7	50	μA	$V_{DS} = 650\text{ V}$, $V_{PVM} = 0\text{ V}$, $T_C = 125\text{ °C}$
$R_{DS(ON)}$	Drain-Source Resistance		175	260	m Ω	$V_{PVM} = 6\text{ V}$, $I_D = 4\text{ A}$
$R_{DS(ON)}$	Drain-Source Resistance		362		m Ω	$V_{PVM} = 6\text{ V}$, $I_D = 4\text{ A}$, $T_C = 125\text{ °C}$
V_{SD}	Source-Drain Reverse Voltage		3.2	5	V	$V_{PVM} = 0\text{ V}$, $I_{SD} = 4\text{ A}$
Q_{OSS}	Output Charge		16		nC	$V_{DS} = 400\text{ V}$, $V_{PVM} = 0\text{ V}$
Q_{RR}	Reverse Recovery Charge		0		nC	
C_{OSS}	Output Capacitance		18		pF	$V_{DS} = 400\text{ V}$, $V_{PVM} = 0\text{ V}$
$C_{O(er)}^{(8)}$	Effective Output Capacitance, Energy Related		24		pF	$V_{DS} = 400\text{ V}$, $V_{PVM} = 0\text{ V}$
$C_{O(tr)}^{(9)}$	Effective Output Capacitance, Time Related		40		pF	$V_{DS} = 400\text{ V}$, $V_{PVM} = 0\text{ V}$

(8) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(9) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

6.6. Switching Waveforms

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified)

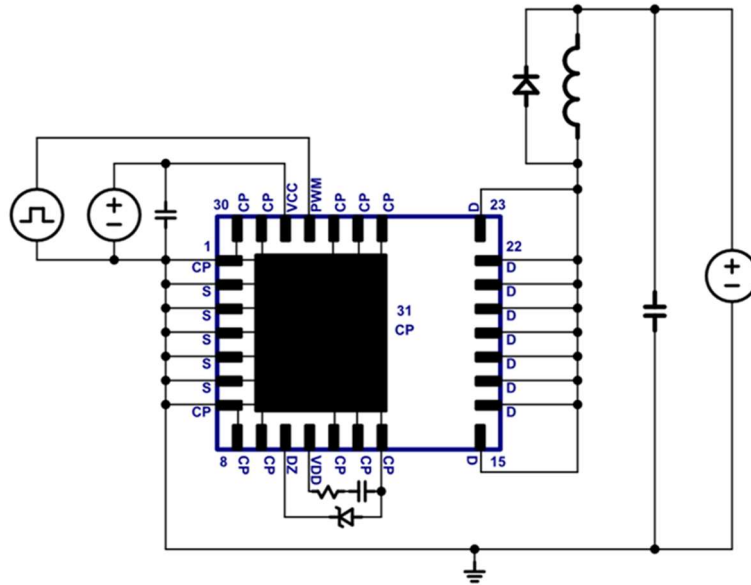


Fig. 1. Inductive switching circuit

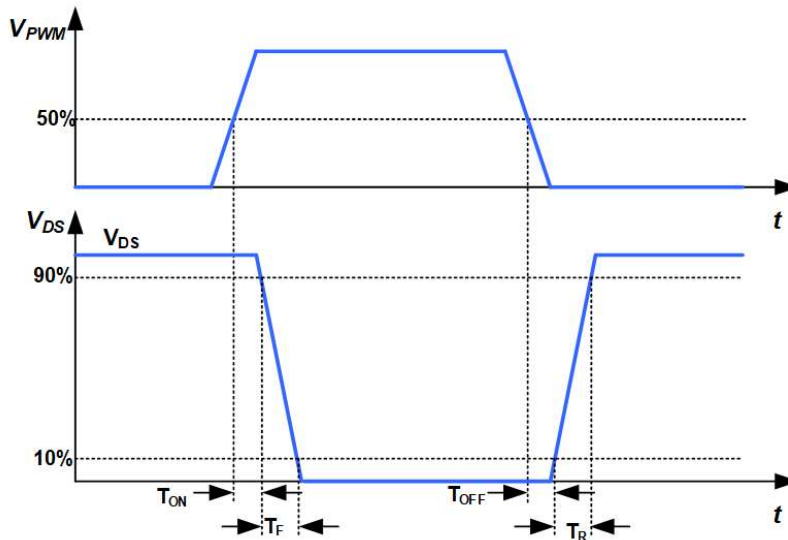


Fig. 2. Propagation delay and rise/fall time definitions

6.7. Characteristic Graphs

(GaN FET, $T_c = 25\text{ }^\circ\text{C}$ unless otherwise specified)

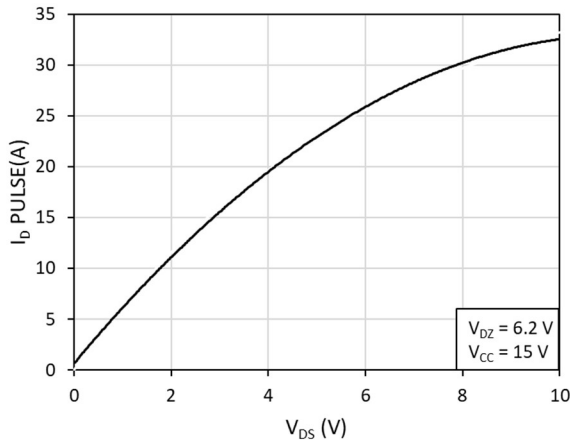


Fig. 3. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at $T = 25\text{ }^\circ\text{C}$

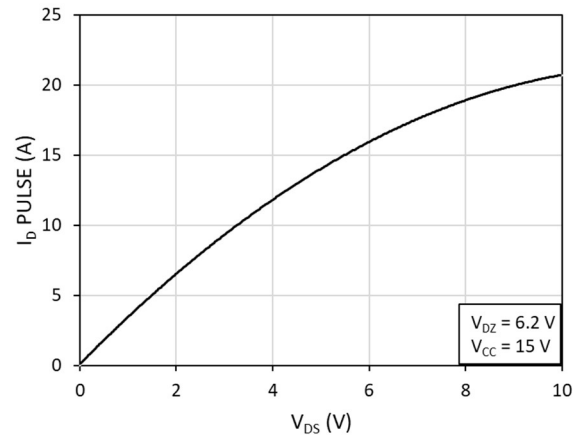


Fig. 4. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at $T = 125\text{ }^\circ\text{C}$

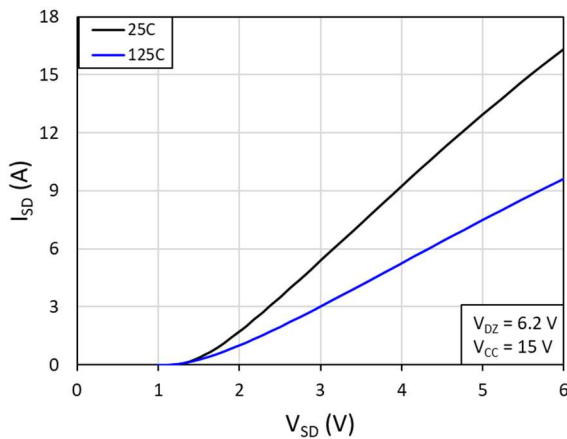


Fig. 5. Source-to-drain reverse conduction voltage

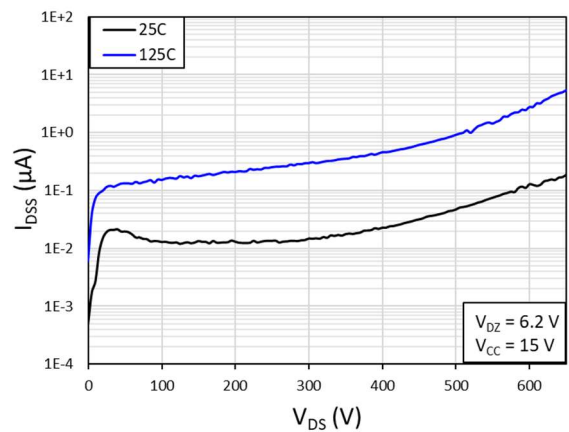


Fig. 6. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

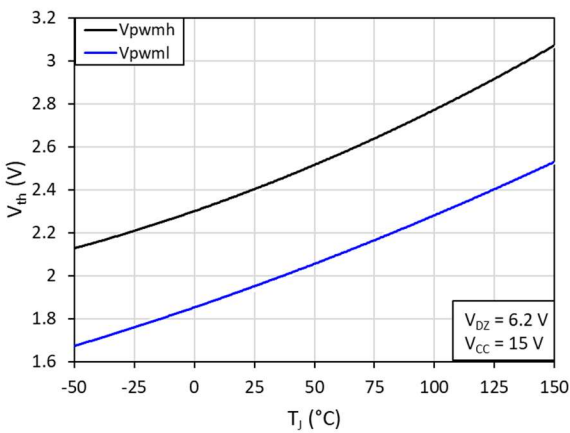


Fig. 7. V_{PWMH} and V_{PWML} vs. junction temperature (T_J)

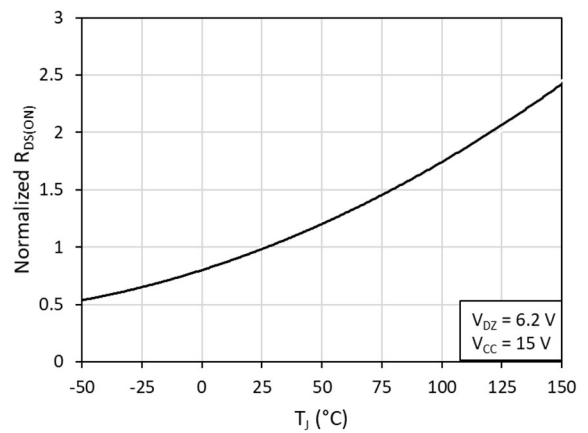


Fig. 8. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

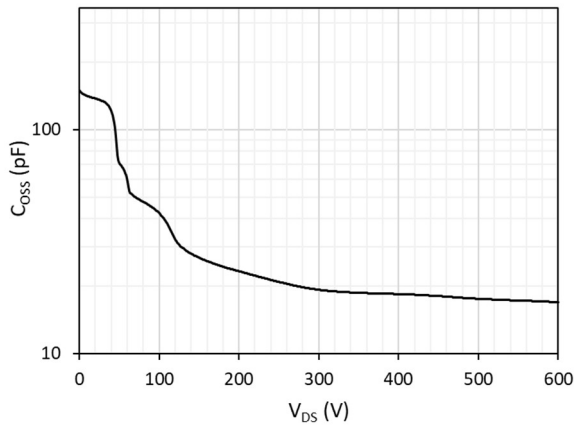


Fig. 9. Output capacitance (C_{OSS}) vs. drain-to-source voltage (V_{DS})

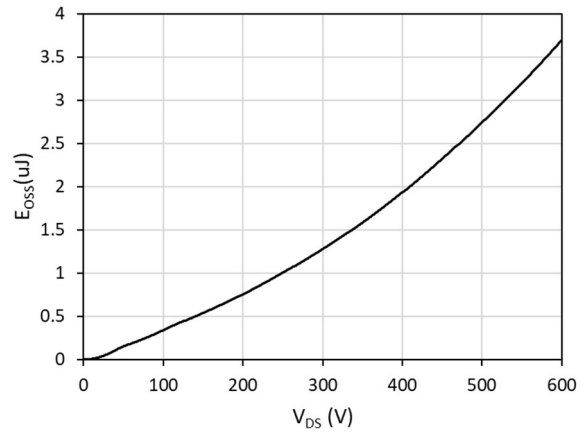


Fig. 10. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

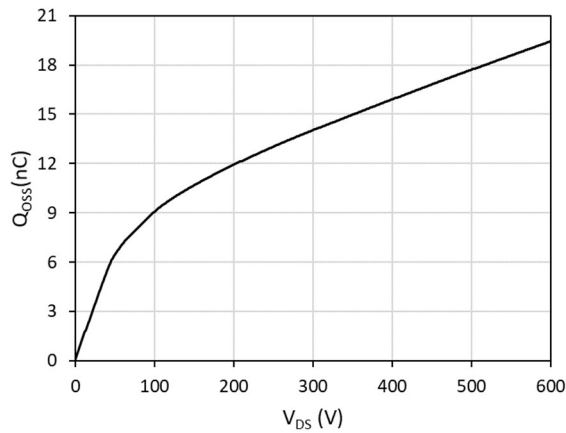


Fig. 11. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

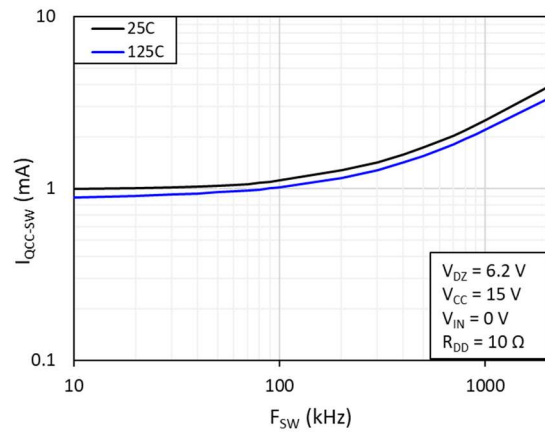


Fig. 12. V_{CC} operating current (I_{QCC-SW}) vs. operating frequency (F_{SW})

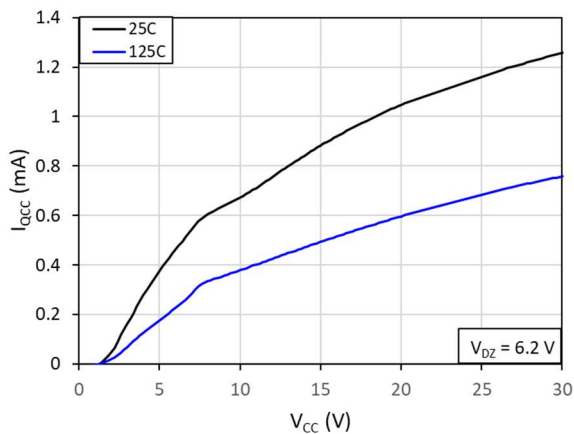


Fig. 13. V_{CC} quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

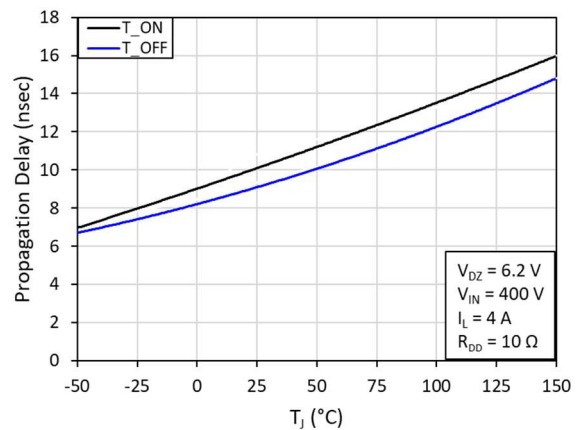


Fig. 14. Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

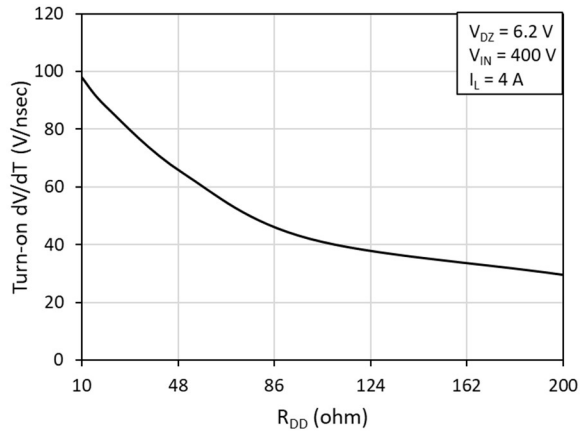


Fig. 15. Slew rate (dV/dt) vs. gate drive turn-on current set resistance (R_{DD}) at $T = 25\text{ }^{\circ}\text{C}$

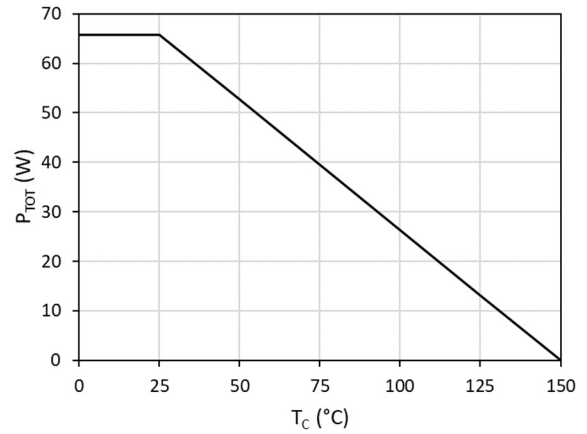


Fig. 16. Power dissipation (P_{TOT}) vs. case temperature (T_C)

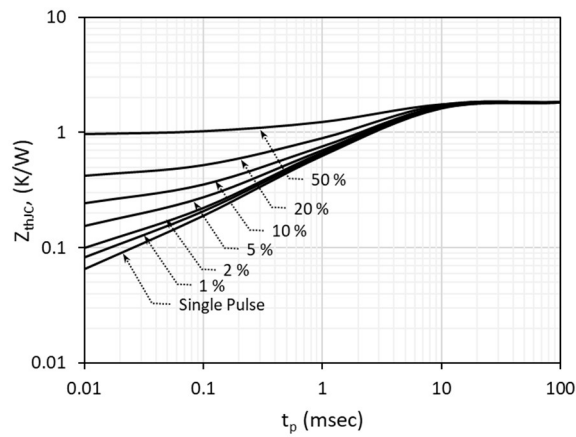
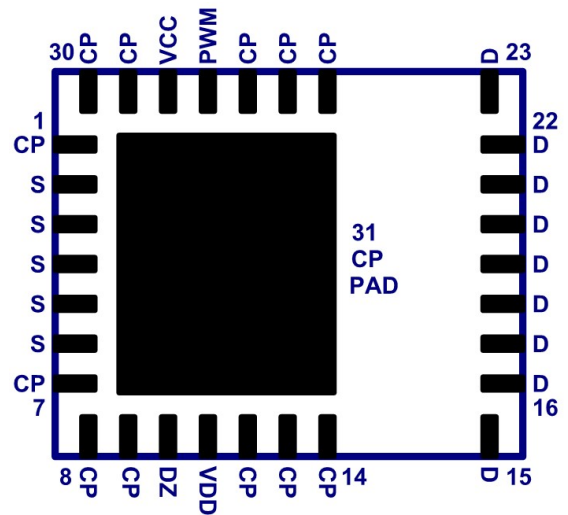
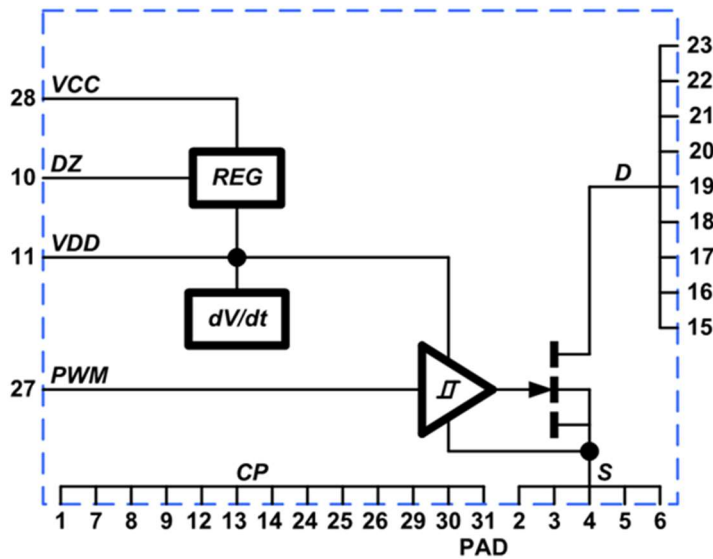


Fig. 17. Max. thermal transient impedance (Z_{thJC}) vs. pulse width (t_p)

7. Internal Schematic, Pin Configurations and Functions



Package Top View

Pin		I/O ⁽¹⁾	Description
Number	Symbol		
1,7,8,9,12,13,14,24,25,26,29,30,31	CP	T	Metal cooling pad on bottom of package for thermal management. CP must be connected to Source or circuit PGND. Do not leave CP unconnected or floating!
2,3,4,5,6	S	O, G	Source of power FET & GaN IC supply ground.
10	D _Z	I	Gate drive supply voltage set pin (connect 6.2 V Zener to GND).
11	V _{DD}	I	Gate drive supply voltage. Gate drive turn-on current set pin (using R _{DD}).
27	PWM	I	PWM input
28	V _{CC}	P	Supply voltage (10V to 24V)
15,16,17,18,19,20,21,22,23	D	P	Drain of power FET

(1) I = Input, O = Output, P = Power, G = GaN IC Ground, T = Thermal

8. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality.

8.1. Start Up

When the V_{CC} supply is first applied to the NV6125, care should be taken such that the V_{DD} and D_Z pins are up at their correct voltage levels before the PWM input signal starts. The V_{DD} pin ramp up time is determined by the internal regulator current at this pin and the external C_{VDD} capacitor. C_{VDD} time constant should be calculated such that there is sufficient time to charge up the C_{VDD} capacitor to $\sim 6V$. In some scenarios, where fast startup is required, an optional diode in parallel with the R_{DD} can be used to ensure the C_{VDD} capacitor is fully charged before the first PWM pulse is applied. Also, since the D_Z pin voltage sets the V_{DD} voltage level, the V_{DD} pin will ramp up together with the D_Z pin (Fig. 18).

For half-bridge configurations, it is important that the V_{CC} supply, the D_Z pin, and the V_{DD} supply of the high-side NV6125 are all charged up to their proper levels before the first high-side PWM pulses start. For LLC applications, a long on-time PWM pulse to the low-side ($> 10 \mu s$) is typically provided by the LLC controller to allow the supply pins of the high-side NV6125 to charge up (through the external bootstrap diode) to their correct levels before the first high-side PWM pulses start (Fig. 19).

For active clamp flyback (ACF) applications, the half-bridge must be ready very quickly due to the soft-start mode of the ACF controller. When the first few PWM pulses are generated by the ACF controller, the high-side supply pins of the NV6125 will require a few low-side pulses to charge up (through the external bootstrap diode) before the high-side starts to switch (Fig. 20).

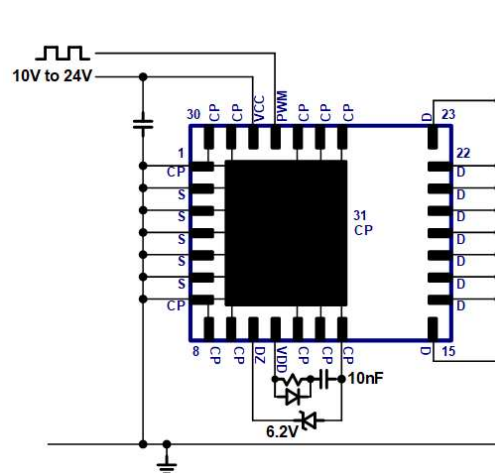


Fig. 18. Start-up circuit

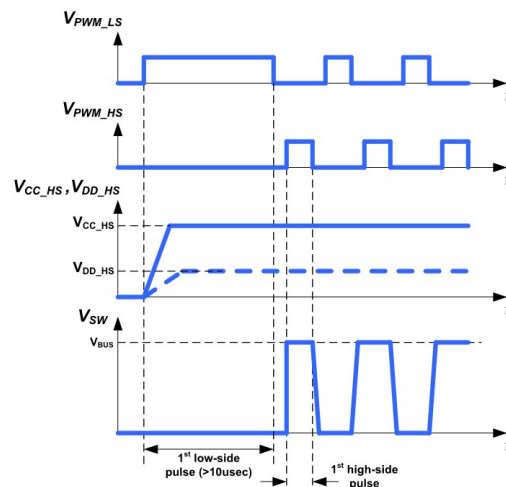


Fig. 19. LLC half-bridge start-up timing diagram

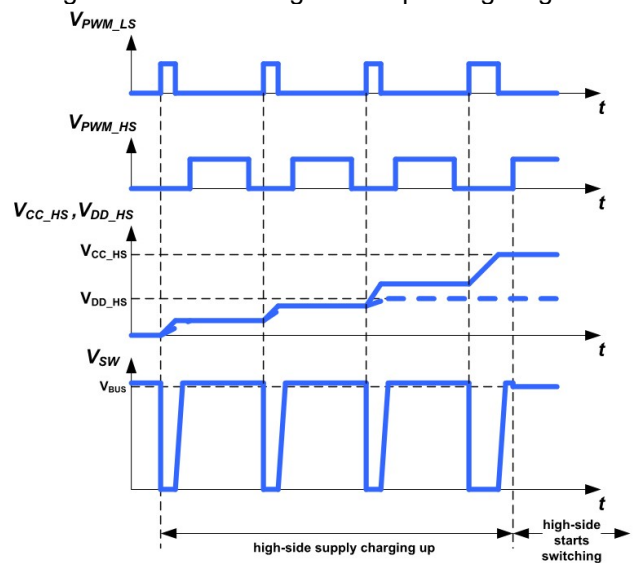


Fig. 20. ACF half-bridge start-up timing diagram

8.2. Normal Operating Mode

During Normal Operating Mode, all of the internal circuit blocks are active. V_{CC} is operating within the recommended range of 10 V to 24 V, the V_{DD} pin is at the voltage set by the Zener diode at the D_Z pin (6.2 V), and the internal gate drive and power FET are both enabled. The external PWM signal at the PWM pin determines the frequency and duty-cycle of the internal gate of the power FET. As the PWM voltage toggles above and below the rising and falling input thresholds (4 V and 1 V), the internal gate of the power FET toggles on and off between V_{DD} and 0 V (Fig. 21). The drain of the power FET then toggles between the source voltage (typically power ground) and a higher voltage level (650 V max), depending on the external power conversion circuit topology.

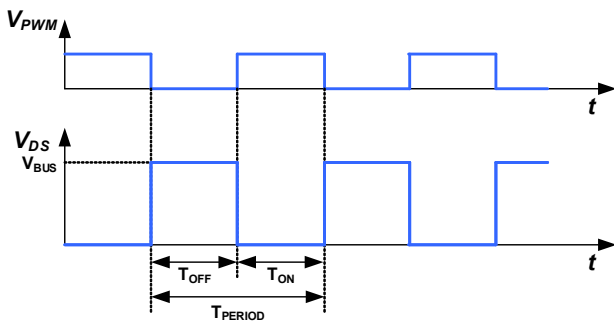


Fig. 21. Normal operating mode timing diagram

8.3. Standby Mode

For applications where a low standby power is required, an external series cut-off circuit (Fig. 22) can be used to disconnect V_{CC} of the NV6125 from the main V_{CC} supply of the power supply. This will reduce V_{CC} current consumption when the converter is in burst mode during light-load or open load conditions. The V_{CC} cut-off circuit consists of a series PMOS FET that is turned on and off with a pull-down NMOS FET. The gate of the NMOS is controlled by an external ENABLE signal that should be provided by the main controller of the power supply. The capacitor value at the V_{CC} pin should then be selected according to the desired start-up speed of the NV6125 each time the ENABLE signal toggles high. A 22 nF capacitor at V_{CC} , for example, will give a typical start-up time of approximately 2 μ s. An additional 200 k Ω resistor is placed across the PMOS cut-off FET to provide a small V_{CC} voltage level for proper start-up.

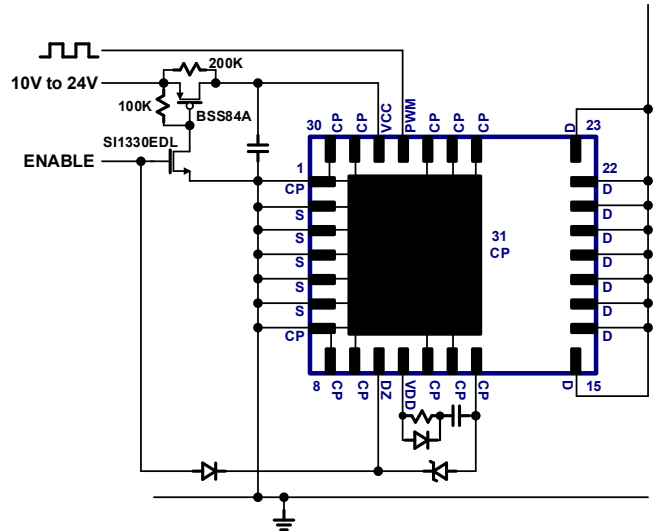


Fig. 22 Standby mode V_{CC} cut-off circuit

8.4. Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the power FET during turn-on. This is necessary to reduce EMI or reduce circuit switching noise. To program the turn-on dV/dt rate of the internal power FET, a resistor (R_{DD}) is placed in between the V_{DD} capacitor and the V_{DD} pin. This resistor (R_{DD}) sets the turn-on current of the internal gate driver and therefore sets the turn-on falling edge dV/dt rate of the drain of the power FET (Fig. 23). A typical turn-on slew-rate change with respect to R_{DD} is shown in Fig. 15.

Minimum 10 Ω R_{DD} is required.

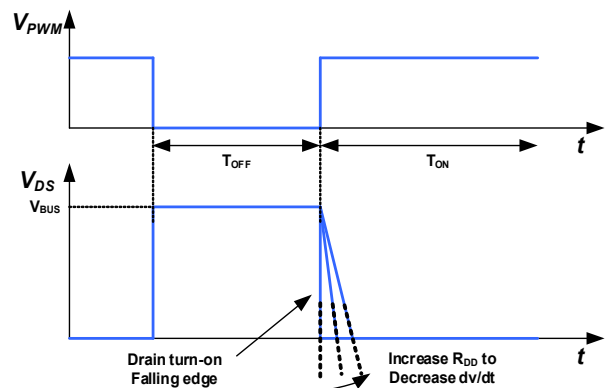


Fig. 23. Turn-on dV/dt slew rate control

8.5. Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the power FET. To sense the current flowing through the NV6125, a standard current-sensing resistor can be placed in between the source and power ground (Fig. 24). In this configuration, all of the components around the NV6125 (C_{VCC} , C_{VDD} , D_Z , etc.) should be grounded with a single connection at the source. Also, an additional RC filter can be inserted between the PWM signal and the PWM pin (100 Ω , 100 pF typical). This filter is necessary to prevent false triggering due to high-frequency voltage spikes occurring at the source node due to external parasitic inductance from the source PCB trace or the current-sensing resistor itself. For increased cooling pad PCB copper area it may be desired to connect CP to the circuit PGND. Fig. 24 shows the components around the NV6125 grounded at the source pins (S and CP connected to PGND). This allows for all CP pins and CP pad to be connected to a large and continuous thermal copper area without being obstructed by the current sensing resistor. **CP must be connected to source (S) or circuit PGND! Do not leave CP floating!**

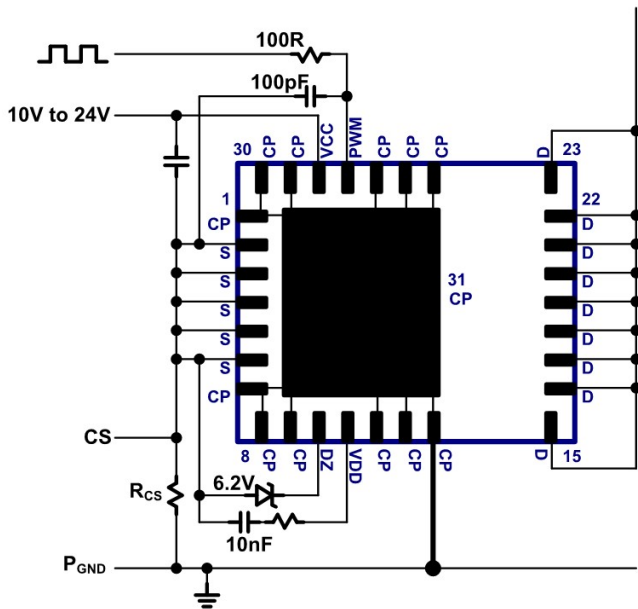


Fig. 24. Current sensing circuit

8.6. Paralleling Devices

For some applications it is desirable to parallel ICs in order to reduce conduction losses and temperatures. Two NV6125 ICs can be connected in parallel in a PFC boost application working in boundary-conduction mode (BCM) only. The parallel configuration for two NV6125 ICs is shown in Fig. 25. The paired pins that are connected together include the drain pins (D), the source pins (S), the VCC pins, the PWM pins, and the Dz. A single Dz diode can be shared by both ICs. The VDD pins are not connected together and require separate VDD supply capacitors (C_{VDD1} , C_{VDD2}) and separate turn-on current set resistors (R_{DD1} , R_{DD2}). Each IC should have its own local VCC supply filter capacitor (C_{VCC1} , C_{VCC2}). The PWM pins can have a single filter resistor (R_{PWM}) but separate filter capacitors (C_{PWM1} , C_{PWM2}) should be placed at the PWM pin of each IC. When designing the PCB layout for the two paralleled ICs, the drain and source connections should be made as symmetrical as possible two avoid any parasitic inductance or capacitance mismatch.

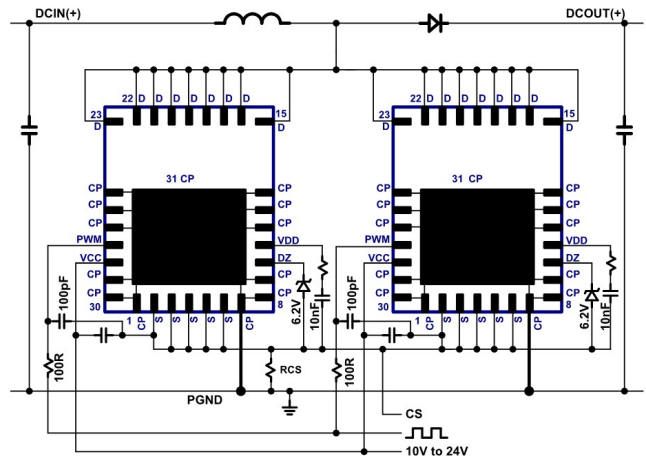


Fig. 25. Boost schematic using two parallel ICs

8.7. 3.3V PWM Input Circuit

For some applications where a 3.3 V PWM signal is required (DSP, MCU, etc.) an additional buffer can be placed before the PWM input pin (Fig. 26) with the buffer supply voltage connected to the V_{DD} capacitor.

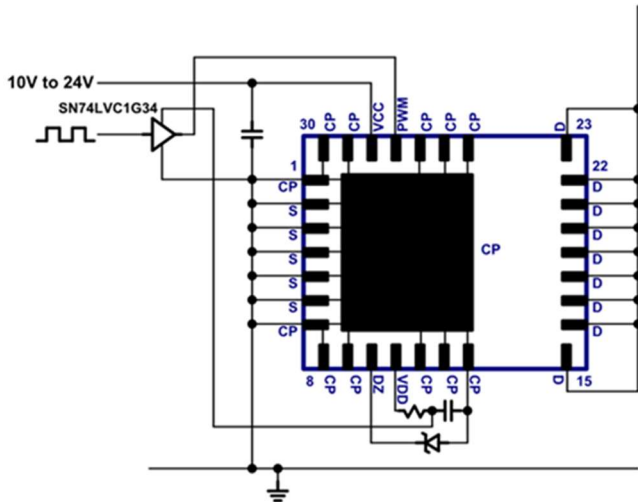


Fig. 26. 3.3 V PWM input buffer circuit

8.8. PCB Layout Guidelines

The design of the PCB layout is critical for good noise immunity, sufficient thermal management, and proper operation of the IC. Typical PCB layout examples for without current sensing resistor and with current sensing resistor are all shown in Section 10.

The following rules should be followed carefully during the design of the PCB layout:

- 1) Place all IC filter and programming components directly next to the IC. These components include (C_{VCC} , C_{VDD} , R_{PWM} , C_{PWM} , R_{DD} and D_z).
- 2) Keep ground trace of IC filter and programming components separate from power GND trace. Do not run power GND currents through ground trace of filter components!
- 3) For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers (see Section 10 for correct layout examples).
- 4) Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible (see Section 10 for correct layout examples).
- 5) For half-bridge layouts, do not extend copper planes from one IC across the components or pads of the other IC!
- 6) For high density designs, use a 4-layer PCB and 2 oz. copper to route signal connections. This allows layout to maintain large thermal copper planes and reduce power device temperature.

8.9. Recommended Component Values

The following table (Table I) shows the recommended component values for the external filter capacitors, Zener diode, and R_{DD} connected to the pins of the NV6125. These components should be placed as close as possible to the IC. Please see PCB Layout guidelines for more information. The Zener diode at the D_z pin should be a low-current type with a flat knee, and the min/max limits must be followed. R_{DD} must be a minimum of $10\ \Omega$ to ensure application and device robustness.

SYM	DESCRIPTION	PART NO.	SUPPLIER	MIN	TYP	MAX	UNITS
C_{VCC}	Maximum V_{CC} supply capacitor				0.1		μF
C_{VDD}	V_{DD} supply capacitor				0.01		μF
R_{DD}	Gate drive turn-on current set resistor			10	25		Ω
D_z	V_{DD} set Zener diode (D_z pin)	BZT52B6V2 RHG	Taiwan Semiconductor Corporation	5.8	6.2	6.6	V
		MM3Z6V2ST1G	ON-Semiconductor				
		PDZ6.2B.115	Nexperia (NXP)				
		PLVA662A.215	Nexperia (NXP)				
		LM3Z6V2T1	Leshan Radio Company				
R_{PWM}	PWM filter resistor				100		Ω
C_{PWM}	PWM filter capacitor				100		μF

Table I. Recommended component values.

8.9.1. Zener Diode Selection

The Zener voltage is a critical parameter that sets the internal reference for gate drive voltage and other circuitry. The Zener diode needs to be selected such that the voltage on the D_z pin is within recommended operating conditions (5.8 V to 6.6 V) across operating temperature (-40°C to 125°C) and bias current (10 μA to 1 mA). To ensure effective operation, the current vs. voltage characteristics of the Zener diode should be measured down to 10 μA to ensure flat characteristics across the current operating range (10 μA to 1 mA). The recommended part numbers meet these requirements. If the Zener selected by user does not ensure that the voltage on the D_z pin is always within the recommended operating range, the functionality and reliability of the NV6125 can be impacted. An external resistor ($\sim 47\ \text{k}\Omega$) between V_{CC} and D_z can improve Zener voltage stability by adding bias current to the D_z pin to ensure the voltage on the D_z pin is always within the recommended operating range (Fig. 27). This will add $\sim 200\ \mu\text{A}$ of quiescent current.

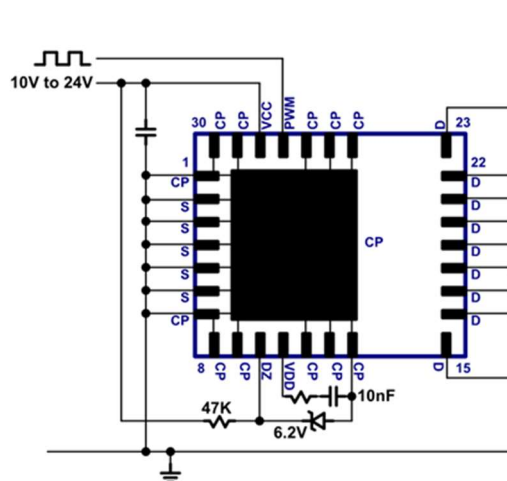


Fig. 27. Increasing Zener bias current for stable Zener voltage

8.10. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 28. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE} . The clamp circuit should be designed to control the magnitude of V_{SPIKE} . It is recommended to apply an 80% derating from $V_{DS(TRAN)}$ rating (800V) to 650 V max for repetitive V_{DS} spikes under the worst case steady-state operating conditions. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 28 as $V_{PLATEAU}$. It is recommended to design the system such that $V_{PLATEAU}$ follows a typical derating of 80% (520V) from $V_{DS(CONT)}$ (650V). Finally, $V_{DS(TRAN)}$ (800V) rating is also provided for events that occur on a non-repetitive basis, such as line surge, lightning strikes, start-up, over-current, short-circuit, load transient, and output voltage transition. 800V $V_{DS(TRAN)}$ ensures excellent device robustness and no-derating is needed for these non-repetitive events, assuming the surge duration is $< 100 \mu s$. For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{PLATEAU}$ derating guideline (520V).

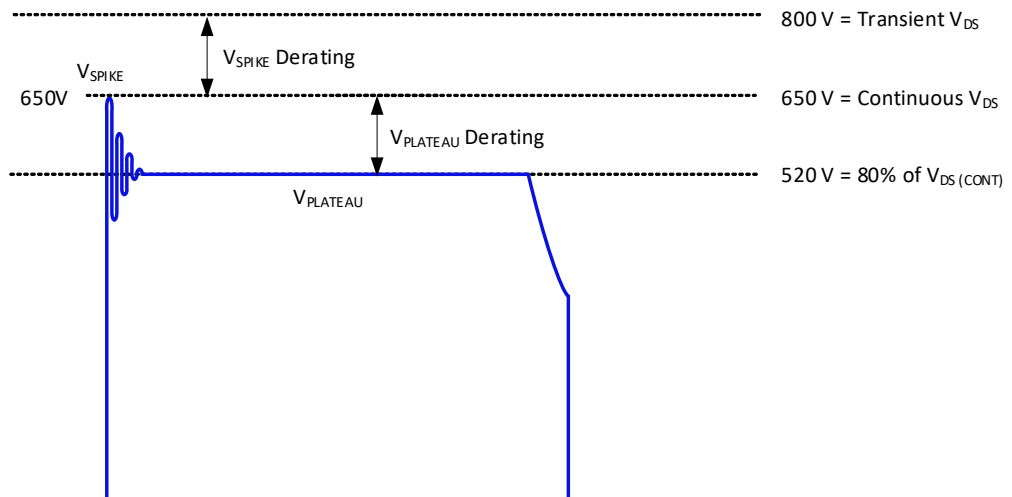
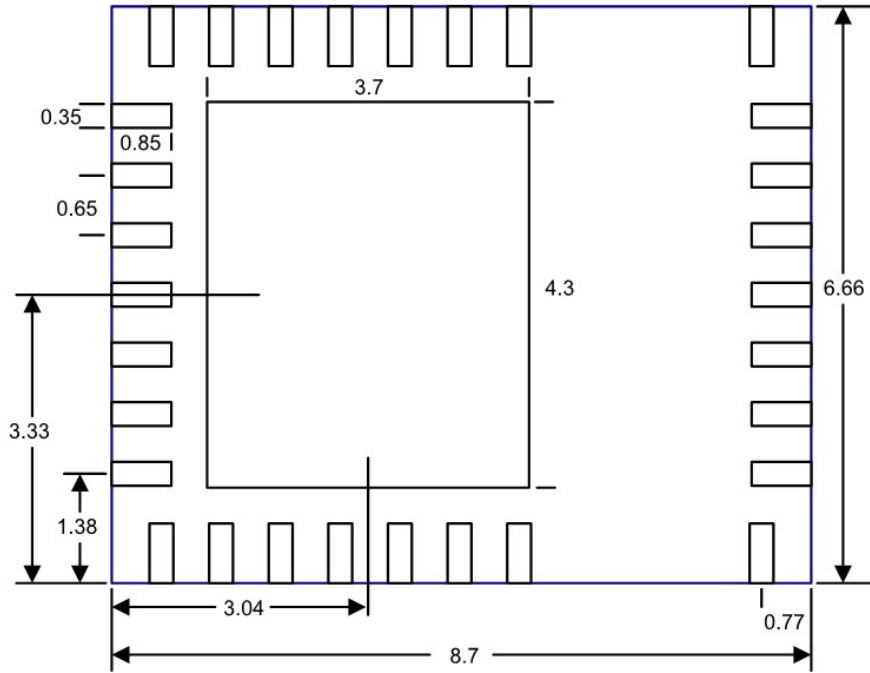


Fig. 28. QR flyback drain-to-source voltage stress diagram

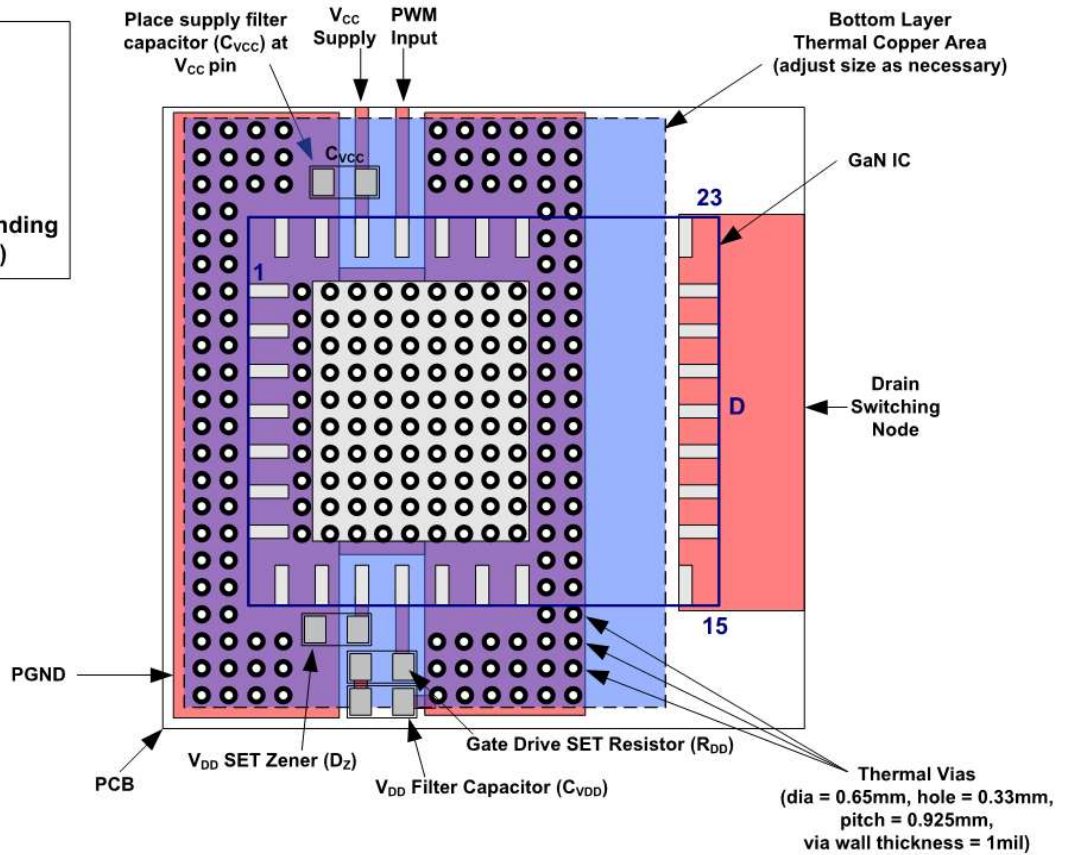
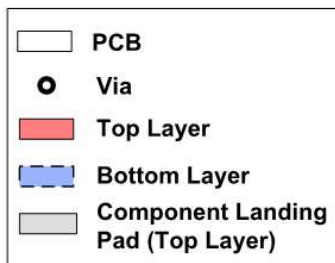
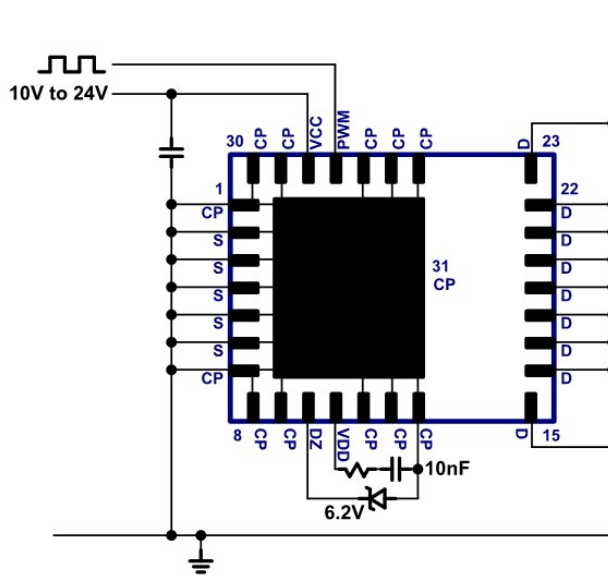
9. Recommended PCB Land Pattern



All dimensions are in mm

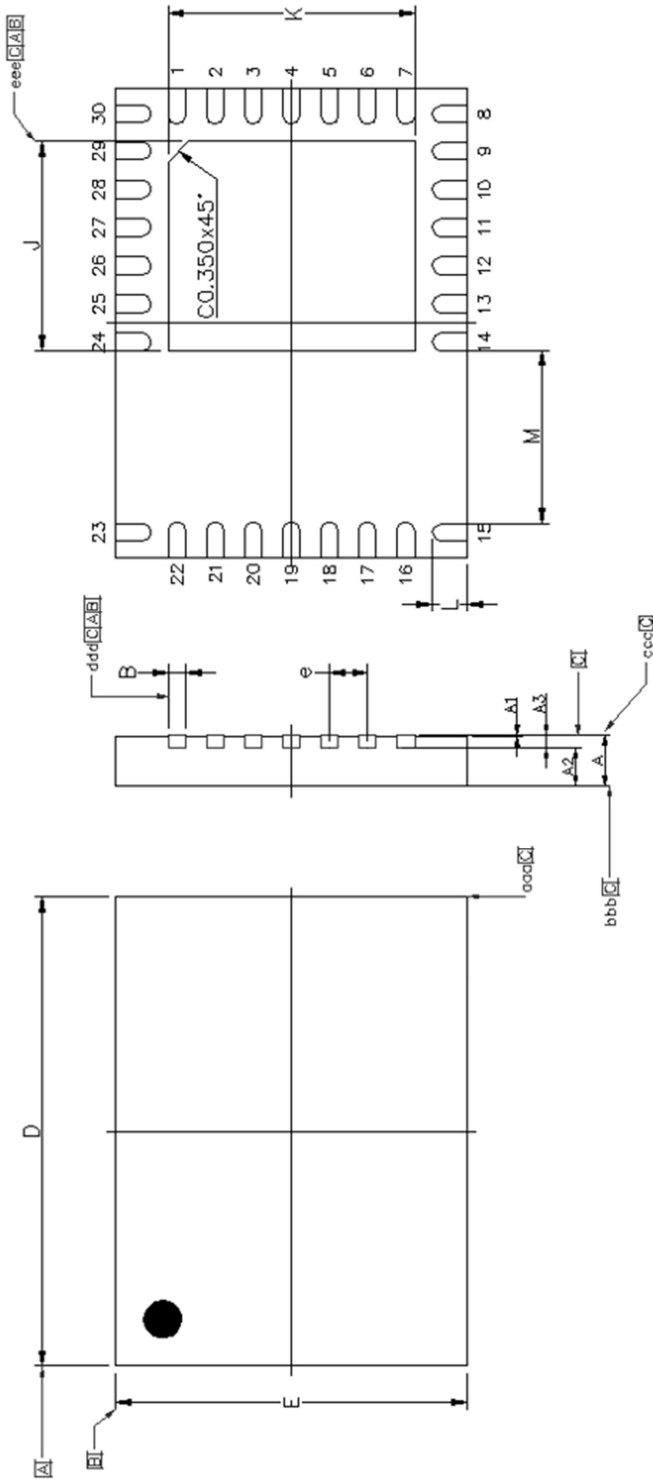
10. PCB Layout Guidelines

Without CS Resistor:



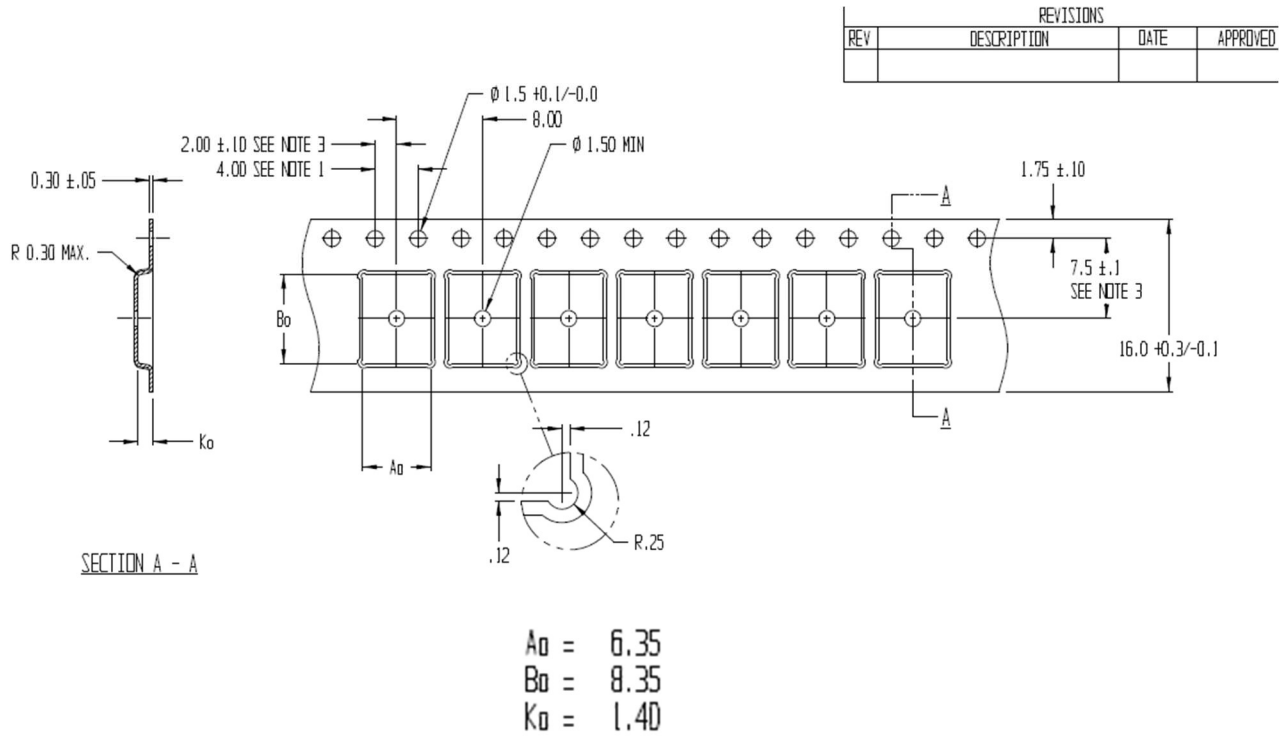
(Top View)

11. QFN Package Outline

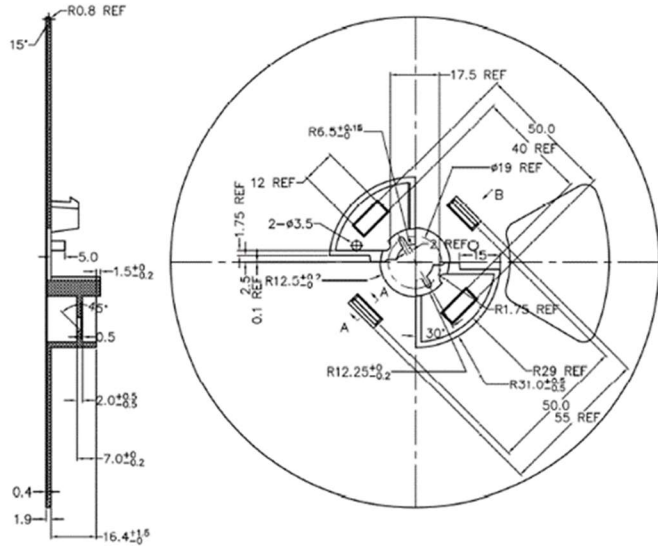
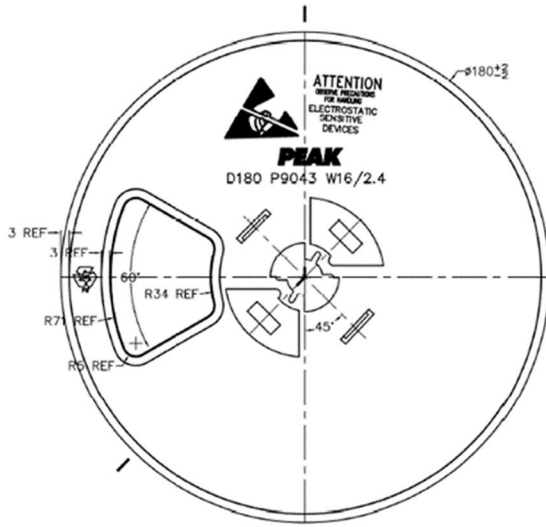


	SYMBOL	MIN	NOM	MAX		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.8	0.85	0.9					
STAND OFF	A1	0.00	0.02	0.05	EP SIZE	X	3.5	3.6	3.7
MOLD THICKNESS	A2	---	0.65	---		Y	4.1	4.2	4.3
L/F THICKNESS	A3	---	0.203 REF	---	LEAD LENGTH	L	0.55	0.6	0.65
LEAD WIDTH	B	0.25	0.3	0.35	HIGH VOLTAGE SPACING	M	2.85	2.95	3.05
BODY SIZE	D	8.00 BSC			PACKAGE EDGE TOLERANCE	aaa	0.1		
		6.00 BSC			MOLD FLATNESS	bbb	0.1		
LEAD PITCH	e	0.65 BSC			COPLANARITY	ccc	0.08		
		0.65 BSC			LEAD OFFSET	ddd	0.1		
					EXPOSED PAD OFFSET	eee	0.1		

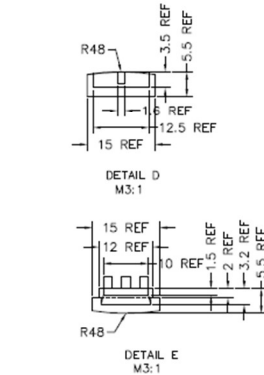
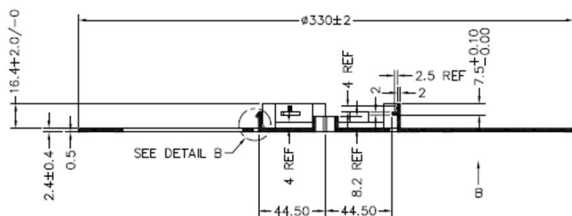
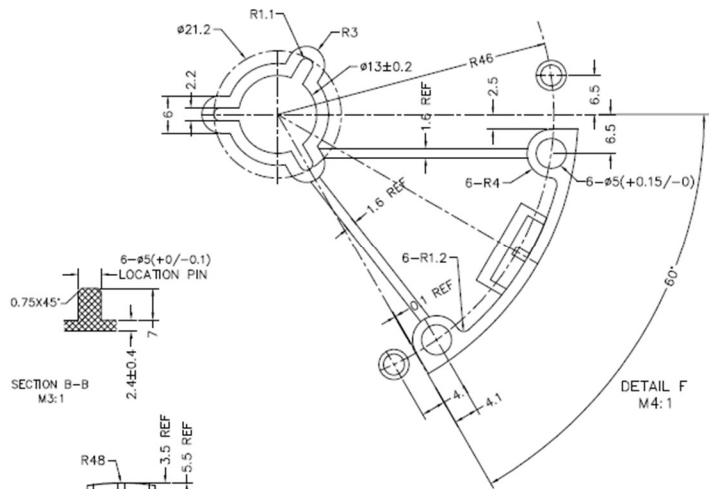
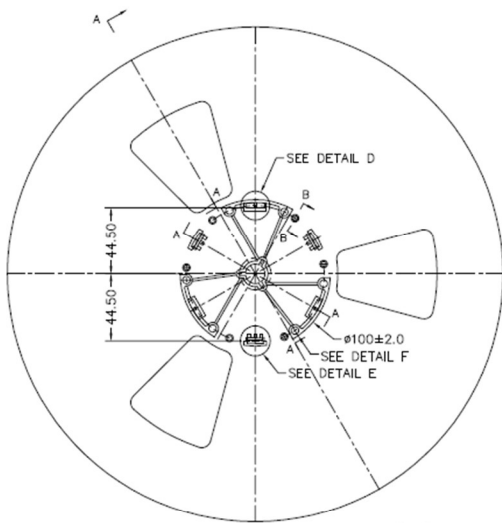
12. Tape and Reel Dimensions



7" Reel



13" Reel



13. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6125-RA	-40 °C to +125 °C T _{CASE}	-55 °C to +150 °C T _{CASE}	6 x 8 mm QFN	3	1,000 : 7" Reel
NV6125	-40 °C to +125 °C TCASE	-55 °C to +150 °C TCASE	6 x 8 mm QFN	3	5,000 : 13" Reel

14. Revision History

Date	Status	Notes
July 19, 2019	Preliminary	First publication
Nov 21, 2019	Initial Release	Updated figures 16&17; added section 8.10
Jun 22, 2020	Revised	Updated guidelines in Section 8.1: Fast startup. Updated R _{DD} specification. This datasheet revision applies to product prior to PCN2020-03-30
Aug 25, 2020	Revised	Datasheet updated in alignment with PCN2020-03-30. Product is marked with Lot Code ending in Z for traceability
Oct 12, 2020	Revised	Updated Section 13 Ordering Information

Additional Information

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