NCE P-Channel Enhancement Mode Power MOSFET

Description

The NCE15P30K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

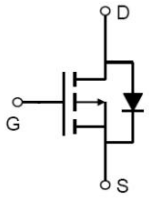
General Features

- V_{DS} =-150V,I_D =-30A
  $R_{DS(ON)}$ <88mΩ @ V_{GS}=-10V (Typ:78mΩ)
  $R_{DS(ON)}$ <95mΩ @ V_{GS}=-4.5V (Typ:81.5mΩ)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

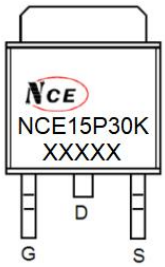
Application

- Portable equipment and battery powered systems

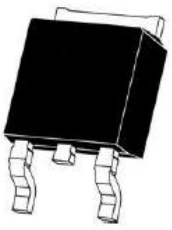
100% UIS TESTED!
100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE15P30K	NCE15P30K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-150	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-30	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-21.2	A
Pulsed Drain Current	I_{DM}	-120	A
Maximum Power Dissipation	P_D	180	W
Single pulse avalanche energy (Note 5)	E_{AS}	338	mJ
Derating factor		1.2	W/℃
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	0.83	℃/W
Thermal Resistance,Junction-to-Ambient (Note 4)	$R_{\theta JA}$	50	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.5	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A	-	78	88	mΩ
		V_{GS}=-4.5V, I_D=-20A	-	81.5	95	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-10V,I_D=-20A	-	50	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-75V,V_{GS}=0V, F=1.0MHz	-	6015	-	pF
Output Capacitance	C_{oss}		-	117	-	pF
Reverse Transfer Capacitance	C_{rss}		-	85	-	pF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-75V,I_D=-20A V_{GS}=-10V,R_{GEN}=9.1Ω	-	17	-	nS
Turn-on Rise Time	t_r		-	80	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	45	-	nS
Turn-Off Fall Time	t_f		-	65	-	nS
Total Gate Charge	Q_g	V_{DS}=-75V,I_D=-20A, V_{GS}=-10V	-	124	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	nC
Gate-Drain Charge	Q_{gd}		-	28	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-20A	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	-30	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =-20A di/dt = 100A/μs(Note3)	-	90	-	nS
Reverse Recovery Charge	Qrr		-	145	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150° C may be used if the PCB allows it.

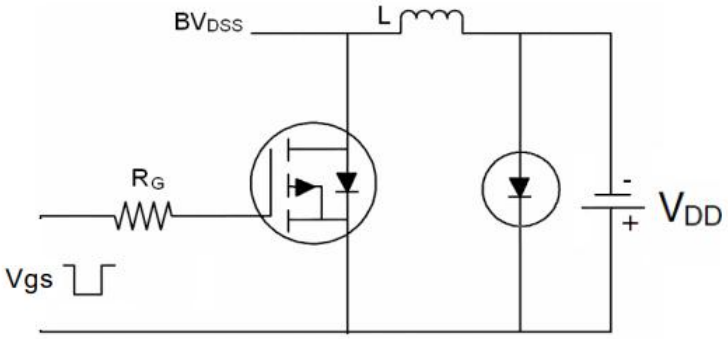
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

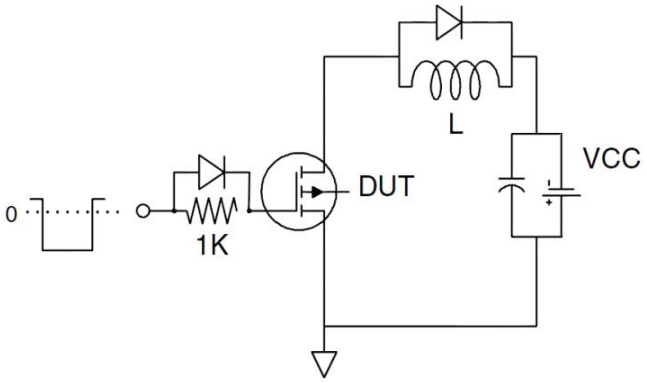
5. EAS condition：Tj=25℃,V_{DD}=-50V,V_G=-10V,L=0.5mH,Rg=25Ω

Test Circuit

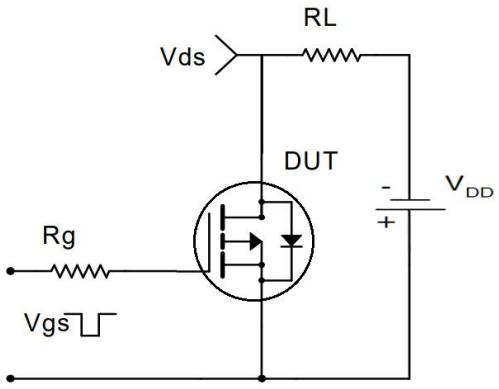
1）E_{AS} test Circuit



2）Gate charge test Circuit



3）Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

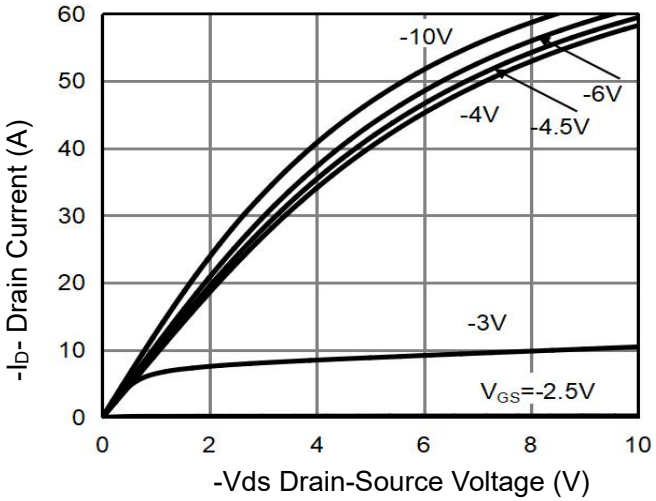


Figure 1 Output Characteristics

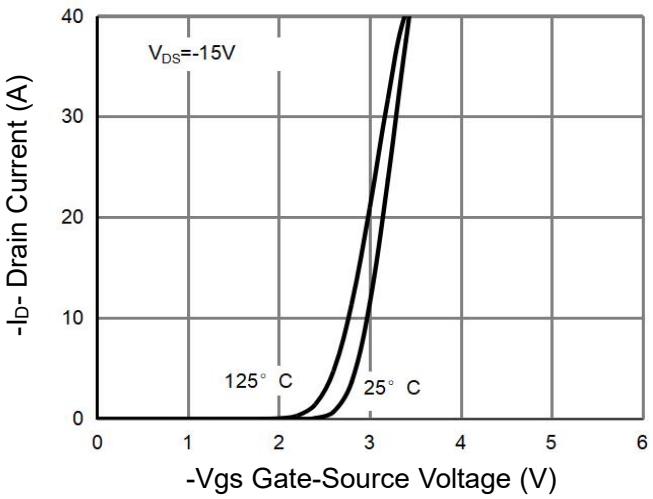


Figure 2 Transfer Characteristics

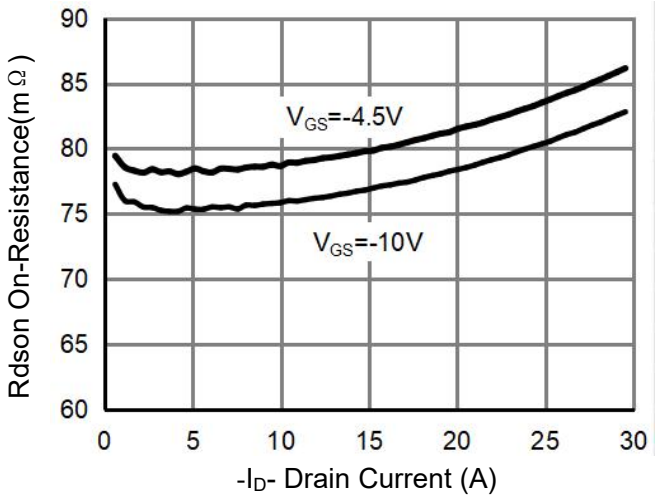


Figure 3 Rdson- Drain Current

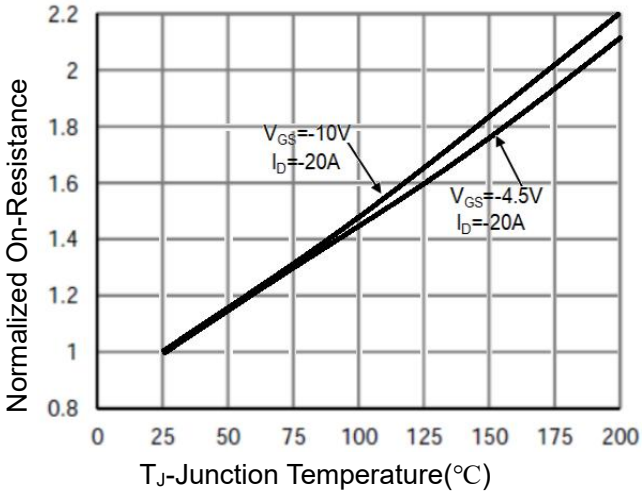


Figure 4 Rdson-JunctionTemperature

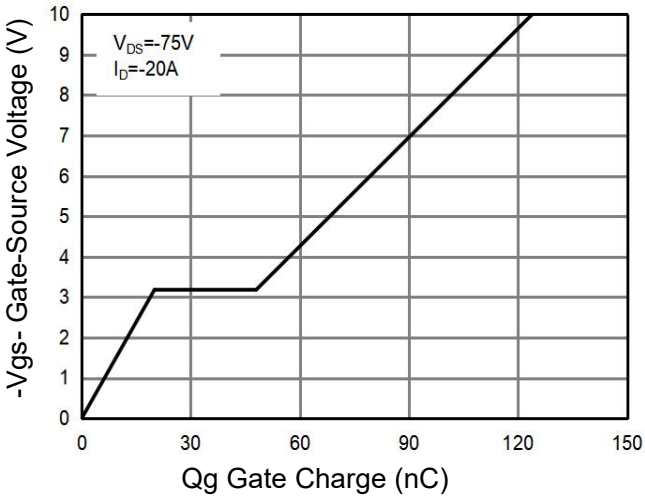


Figure 5 Gate Charge

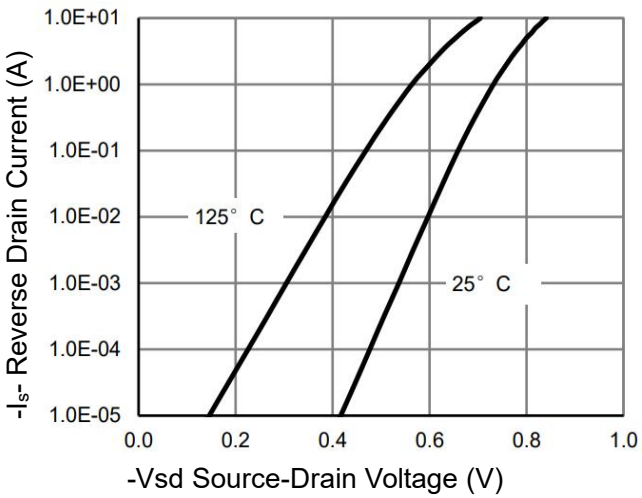


Figure 6 Source- Drain Diode Forward

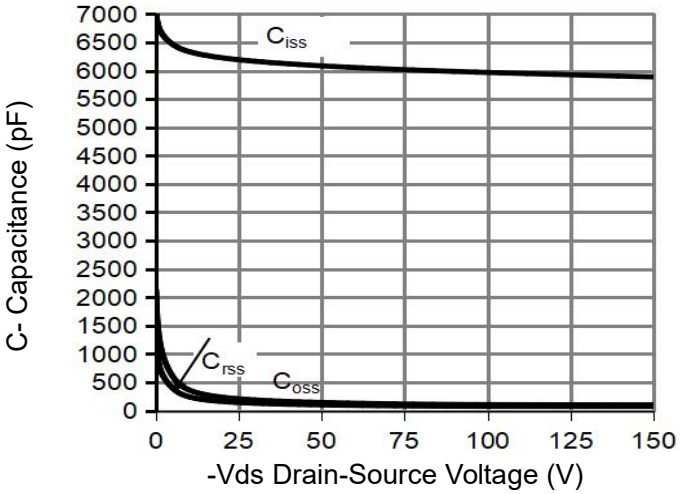


Figure 7 Capacitance vs Vds

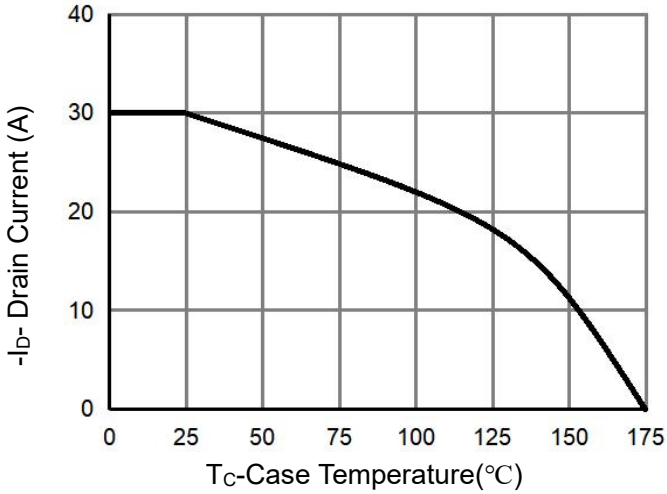


Figure 9 Drain Current vs Case Temperature

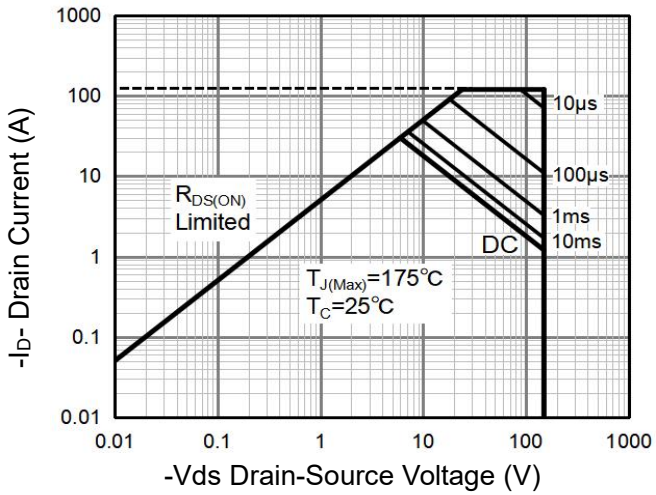


Figure 8 Safe Operation Area

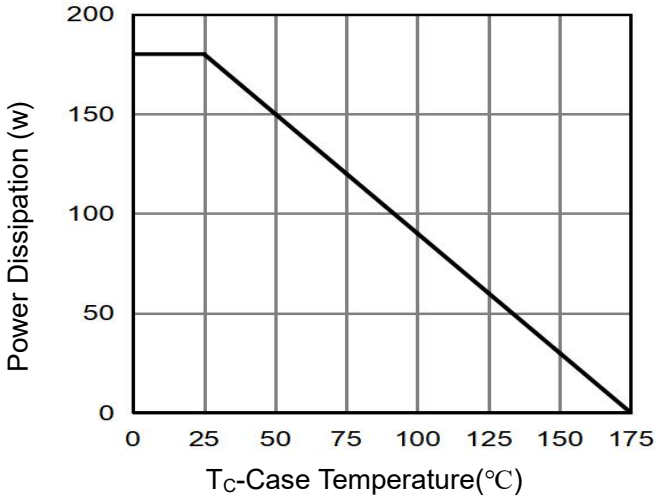


Figure 10 Power De-rating

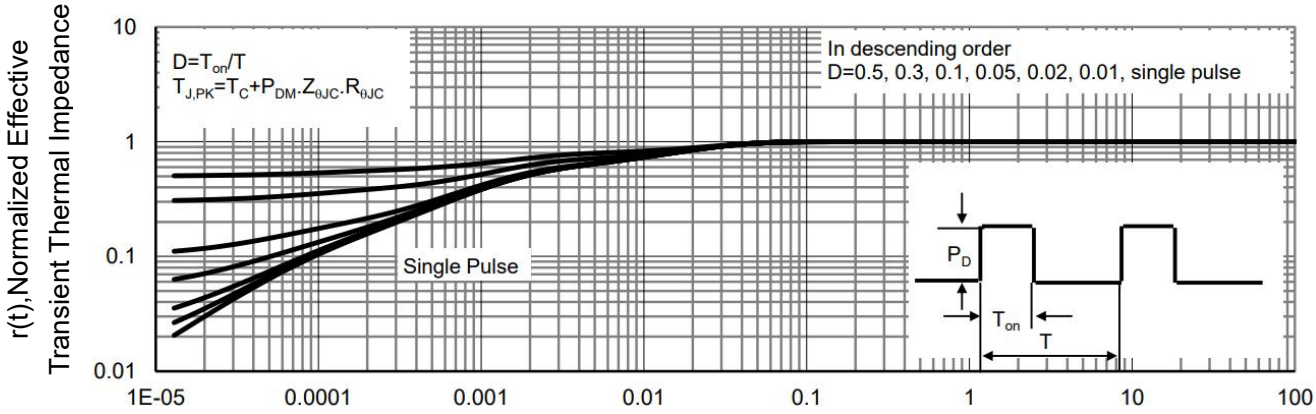
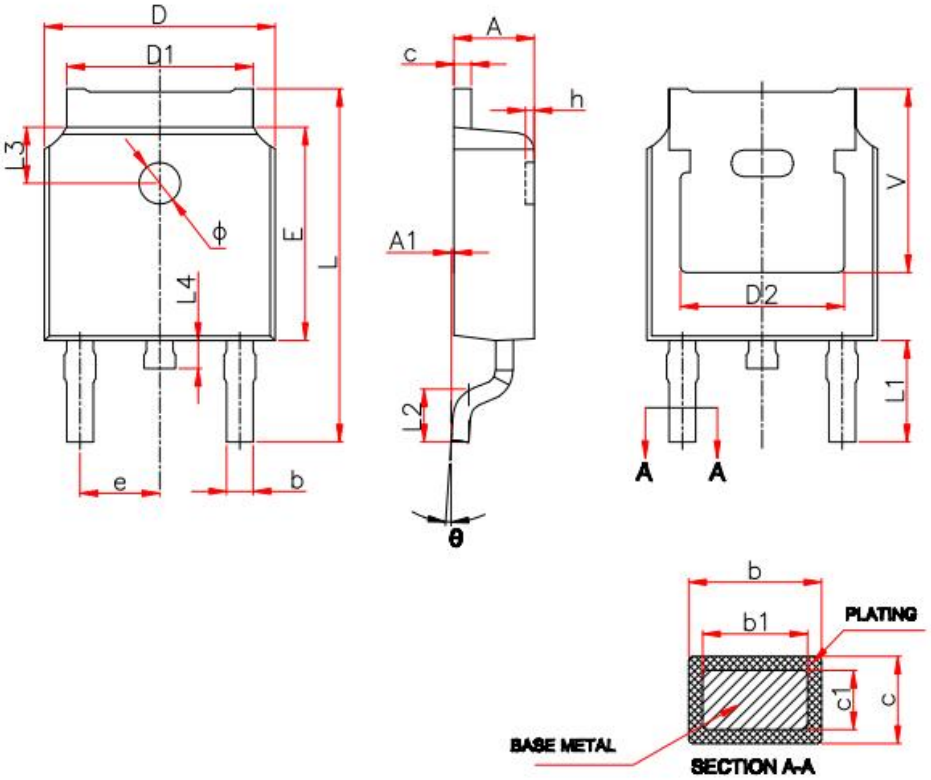


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
Φ	1.10	1.30
θ	0°	8°
h	0.00	0.30
V	5.35 REF.	

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