

NCE Automotive P-Channel Super Trench Power MOSFET

Description

The NCEAP40PT12K uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification

Application

- Automotive application
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

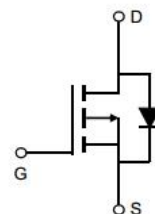
General Features

- $V_{DS} = -40V, I_D = -160A$ (Silicon Limited)
 - $R_{DS(ON)} = 4.1m\Omega$ (typical) @ $V_{GS} = -10V$
 - $R_{DS(ON)} = 5.9m\Omega$ (typical) @ $V_{GS} = -4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested
- 100% ΔV_{ds} tested
- **AEC-Q101 qualified**

TO-252-2L



Top View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AP40PT12K	NCEAP40PT12K	TO-252-2L	Ø330mm	16mm	2500units

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited) ^(Note1)	I_D	-160	A
Drain Current-Continuous (Silicon Limited) ^(Note1)	$I_D(100^\circ C)$	-115	A
Drain Current-Continuous (Package Limited)	I_D	-100	A
Pulsed Drain Current	I_{DM}	-400	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.47	W/°C
Single pulse avalanche energy ^(Note 2)	E_{AS}	1155	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.68	°C/W
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Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.8	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A	-	4.1	5.0	mΩ
		V _{GS} =-4.5V, I _D =-20A	-	5.9	7.5	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-40A	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, F=1.0MHz	-	6100	-	pF
Output Capacitance	C _{oss}		-	1500	-	pF
Reverse Transfer Capacitance	C _{rss}		-	95	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V, I _D =-20A V _{GS} =-10V, R _G =1.6Ω	-	13	-	nS
Turn-on Rise Time	t _r		-	30	-	nS
Turn-Off Delay Time	t _{d(off)}		-	75	-	nS
Turn-Off Fall Time	t _f		-	14	-	nS
Total Gate Charge	Q _g	V _{DS} =-20V, I _D =-20A, V _{GS} =-10V	-	86	-	nC
Gate-Source Charge	Q _{gs}		-	17.5	-	nC
Gate-Drain Charge	Q _{gd}		-	10.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-20A	-	-	-1.2	V
Diode Forward Current	I _S		-	-	-120	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = -60A	-	55	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	75	-	nC

Notes:

1. Defined by design. Not Subject to production test
2. EAS condition : T_J=25°C, V_{DD}=-20V, V_G=-10V, L=0.5mH, R_G=25Ω
3. Guaranteed by design, not subject to production
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

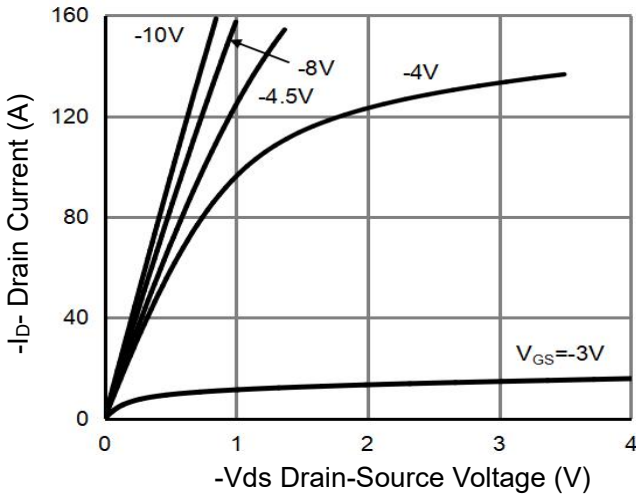


Figure 1 Output Characteristics

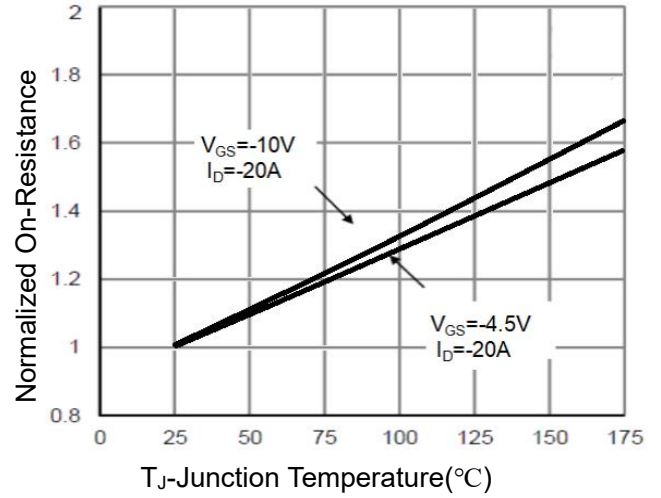


Figure 4 $R_{ds(on)}$ -Junction Temperature

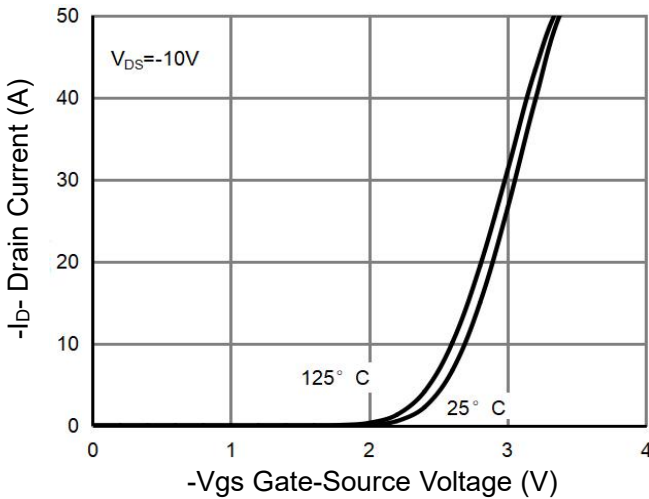


Figure 2 Transfer Characteristics

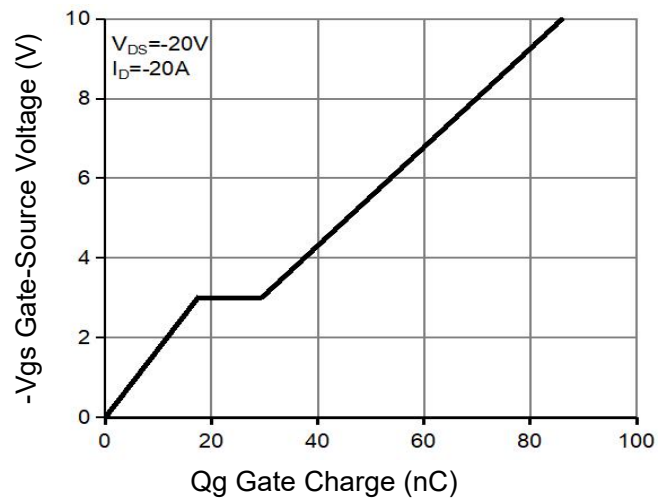


Figure 5 Gate Charge

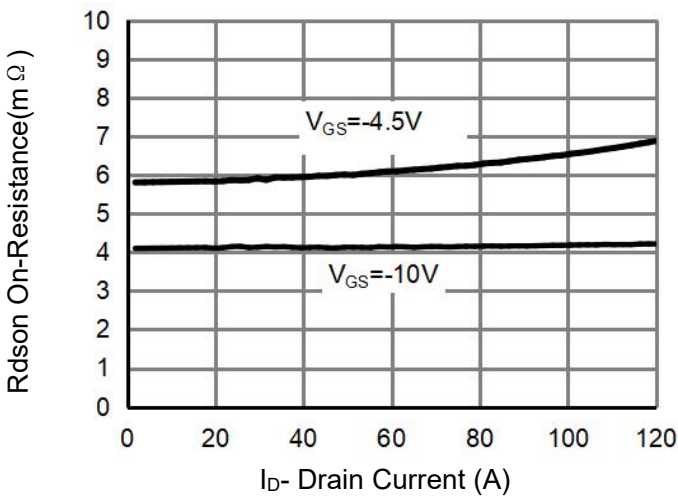


Figure 3 $R_{ds(on)}$ - Drain Current

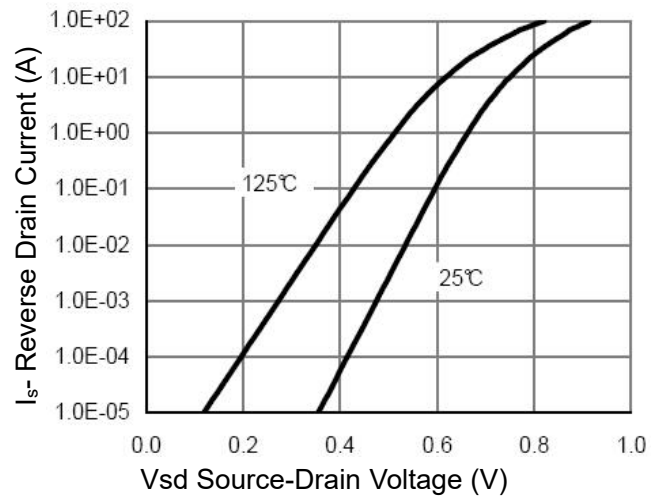


Figure 6 Source- Drain Diode Forward

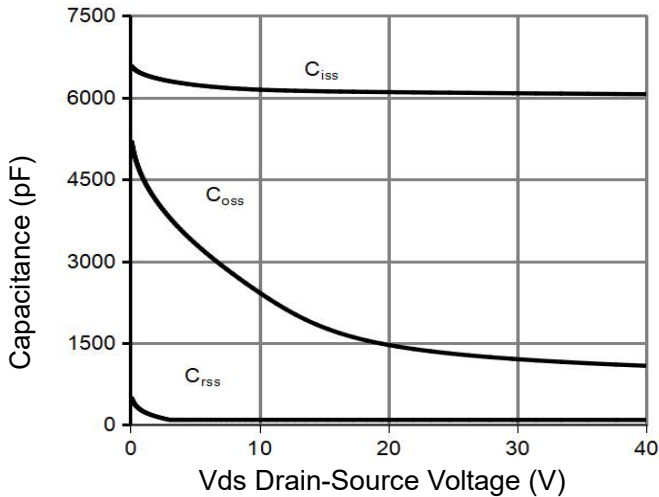


Figure 7 Capacitance vs Vds

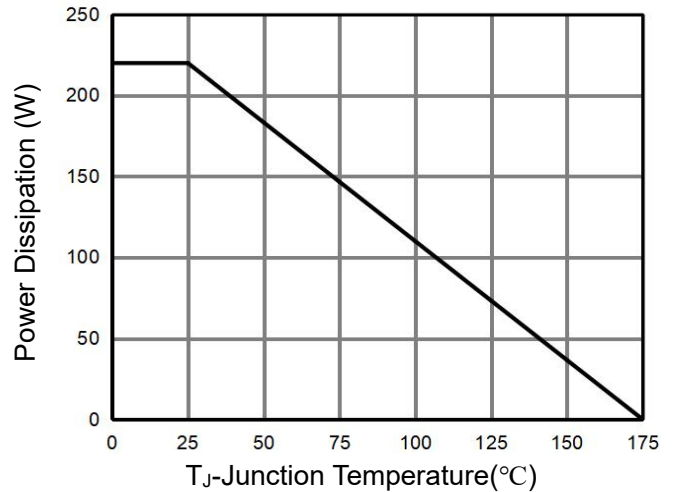


Figure 9 Power De-rating

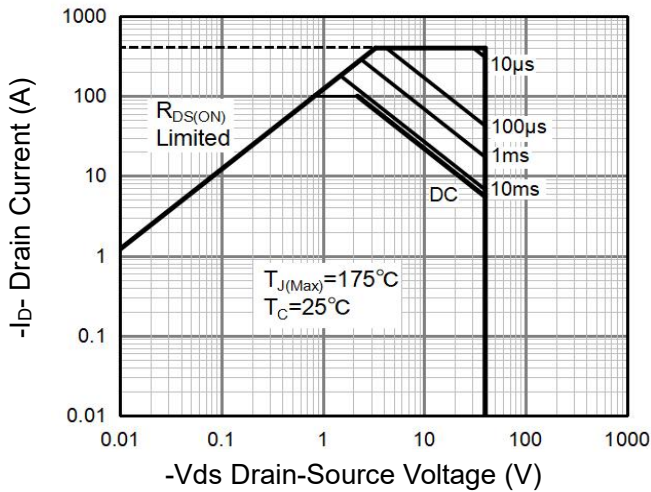


Figure 8 Safe Operation Area^(Note4)

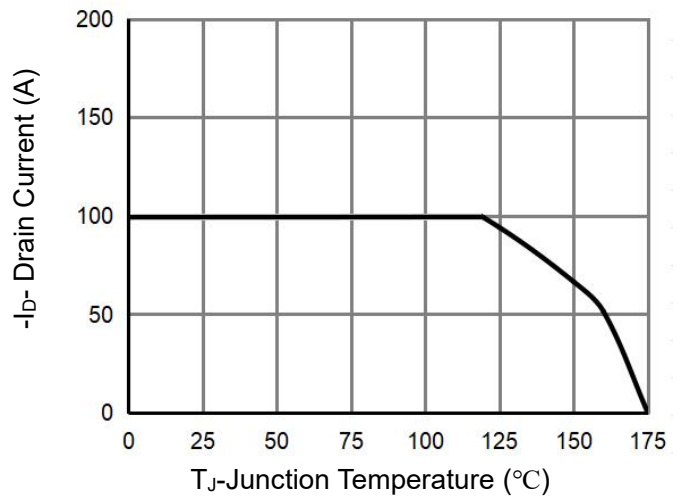


Figure 10 Current De-rating

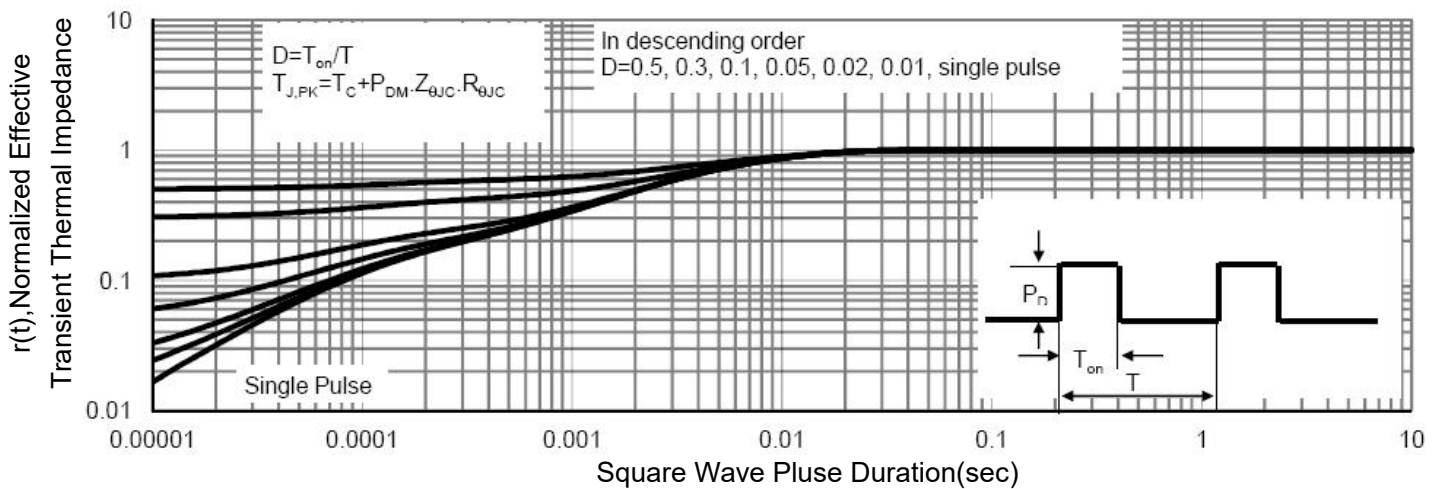
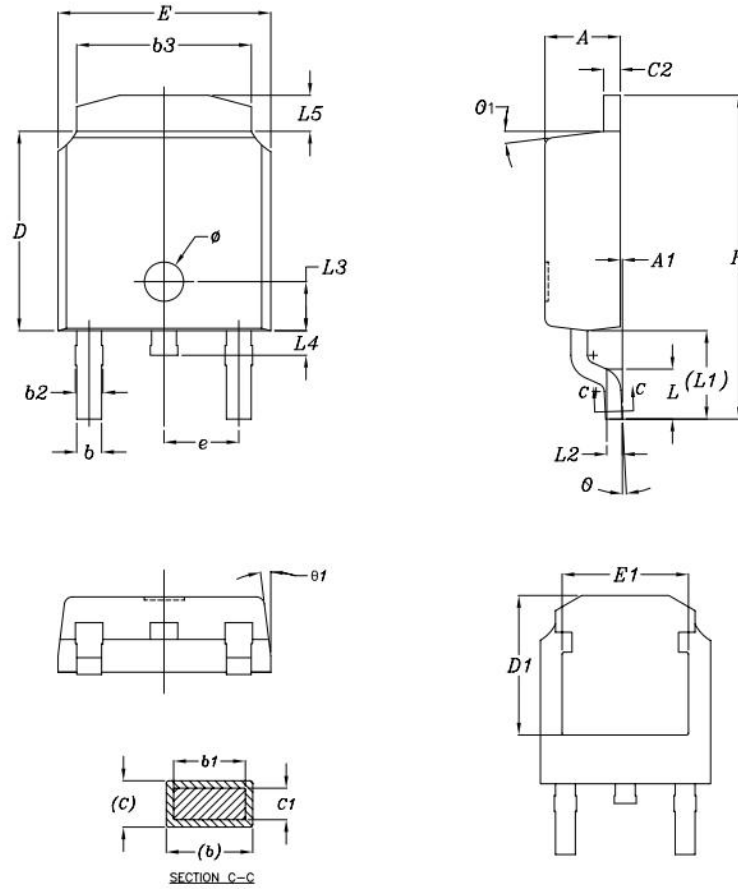


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



I T E M	DIMENSIONS			
	MILLMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	—	0.13	—	0.005
b	0.70	0.89	0.028	0.035
b1	0.70	0.86	0.028	0.034
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	—	0.205	—
E	6.35	6.73	0.250	0.265
E1	4.32	—	0.170	—
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	1.40	1.78	0.055	0.070
L1	2.60	2.90	0.102	0.114
L2	0.51 BSC		0.020 BSC	
L3	1.65	1.95	0.065	0.077
L4	0.60	0.90	0.024	0.035
L5	0.89	1.27	0.035	0.050
φ	1'	5'	1'	5'
φ1	7' REF		7' REF	
φ	1.20 REF		1.20 REF	

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