

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP18N10AR uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

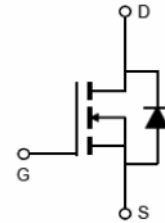
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS} = 100V, I_D = 9.5A$
- $R_{DS(ON)} = 19.2m\Omega$ (typical) @ $V_{GS} = 10V$
- $R_{DS(ON)} = 23.0m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔV_{ds} TESTED!

SOT223



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP18N10AR	NCEP18N10AR	SOT223-3L	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	9.5	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	6.6	A
Pulsed Drain Current ^(Note 1)	I_{DM}	38	A
Maximum Power Dissipation	P_D	2.5	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	115	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	50	$^\circ C/W$
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.7	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =5A	-	19.2	20	mΩ
		V _{GS} =4.5V, I _D =5A	-	23.0	25	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =5A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	1719.5	-	PF
Output Capacitance	C _{oss}		-	147.4	-	PF
Reverse Transfer Capacitance	C _{rss}		-	16	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =5A V _{GS} =10V, R _G =3Ω	-	14	-	nS
Turn-on Rise Time	t _r		-	16	-	nS
Turn-Off Delay Time	t _{d(off)}		-	28	-	nS
Turn-Off Fall Time	t _f		-	8	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =5A, V _{GS} =10V	-	37.6	-	nC
Gate-Source Charge	Q _{gs}		-	6.5		nC
Gate-Drain Charge	Q _{gd}		-	9.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =5A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	9.5	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 5A	-	43	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs (Note3)	-	90	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω

Typical Electrical and Thermal Characteristics

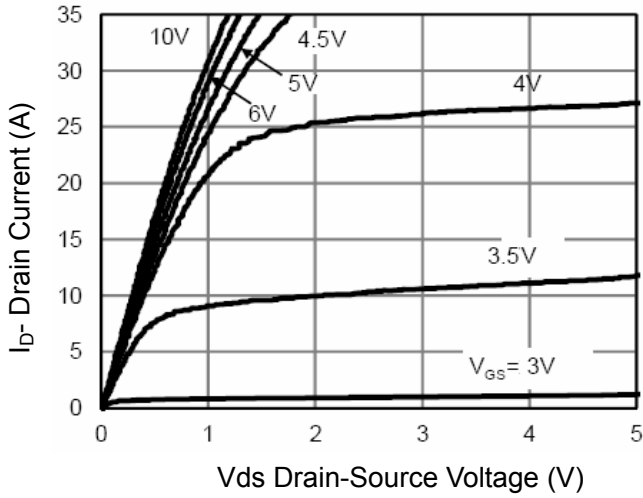


Figure 1 Output Characteristics

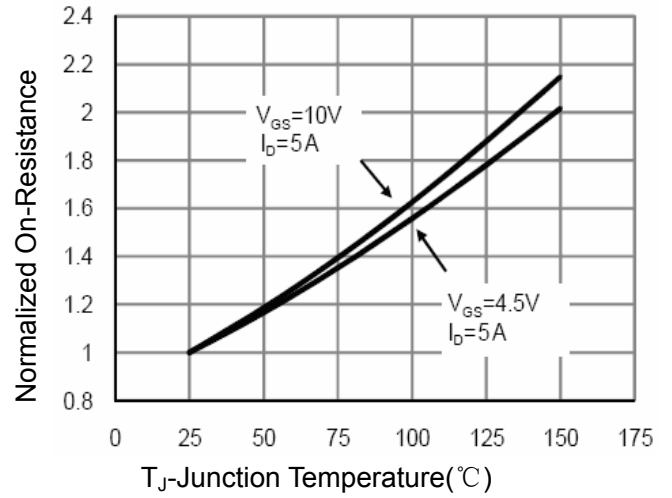


Figure 4 R_{dson} -Junction Temperature

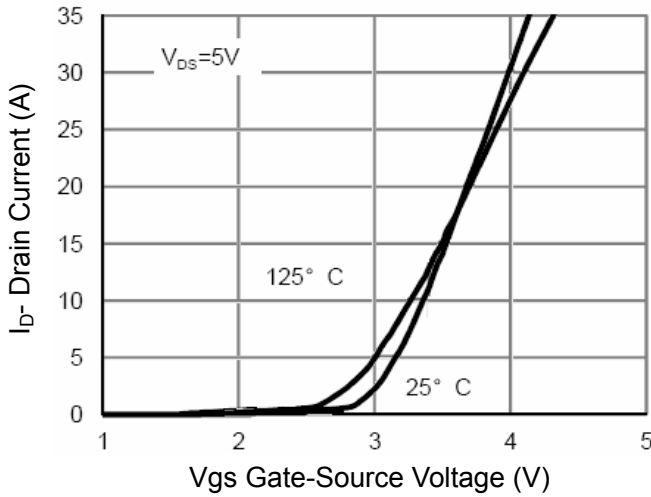


Figure 2 Transfer Characteristics

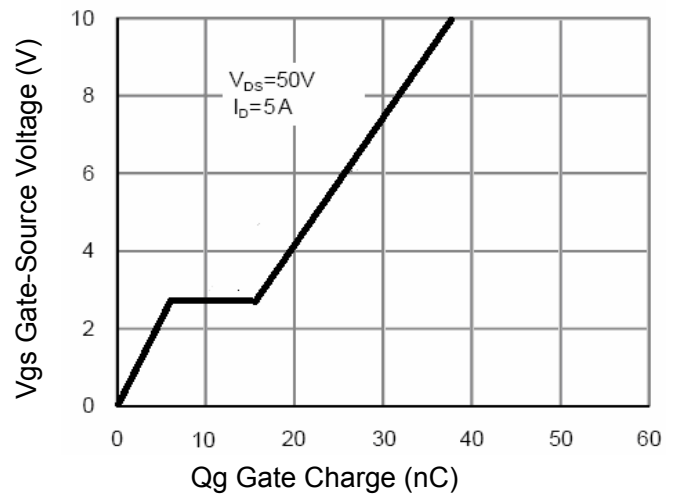


Figure 5 Gate Charge

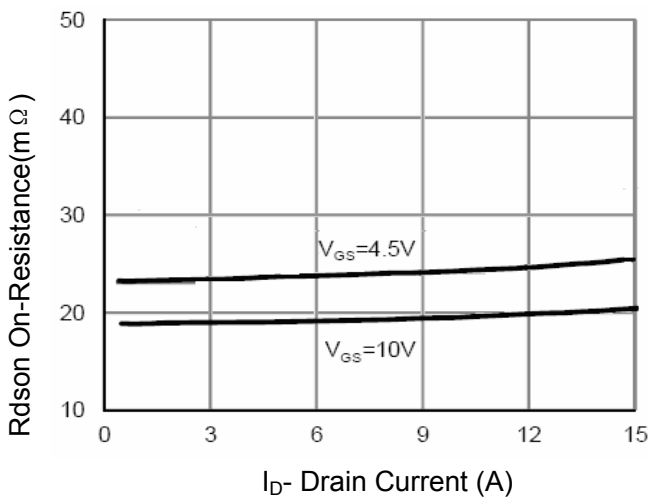


Figure 3 R_{dson} - Drain Current

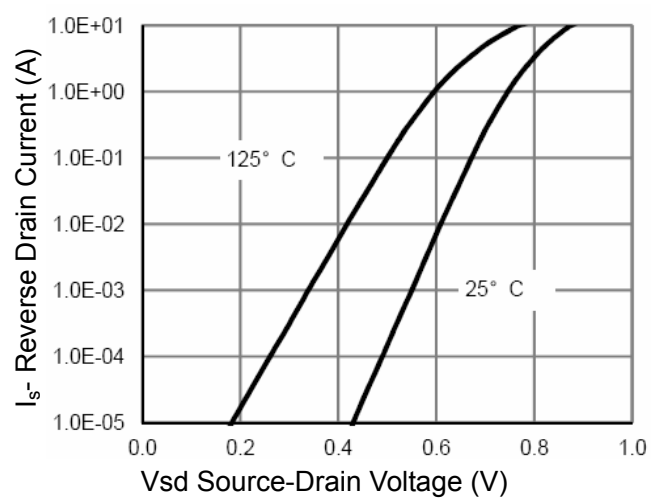


Figure 6 Source- Drain Diode Forward

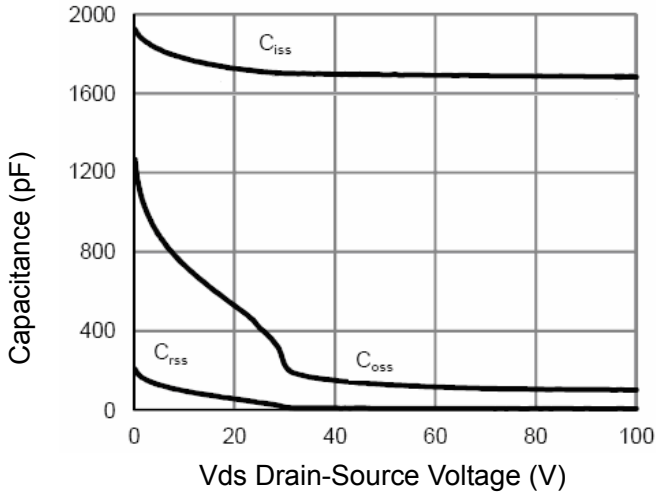


Figure 7 Capacitance vs Vds

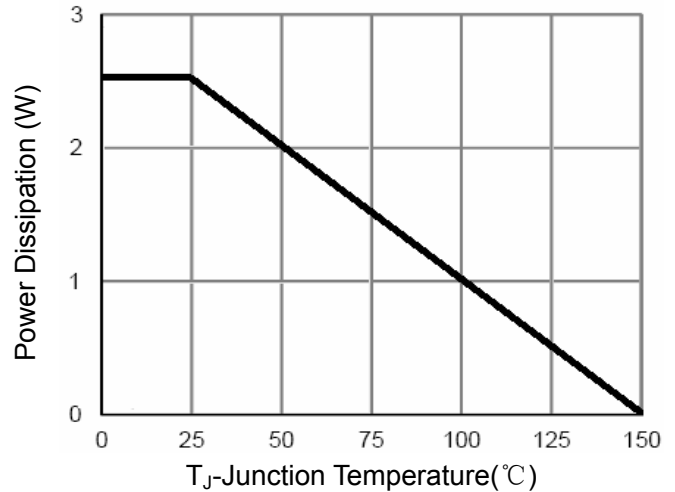


Figure 9 Power De-rating

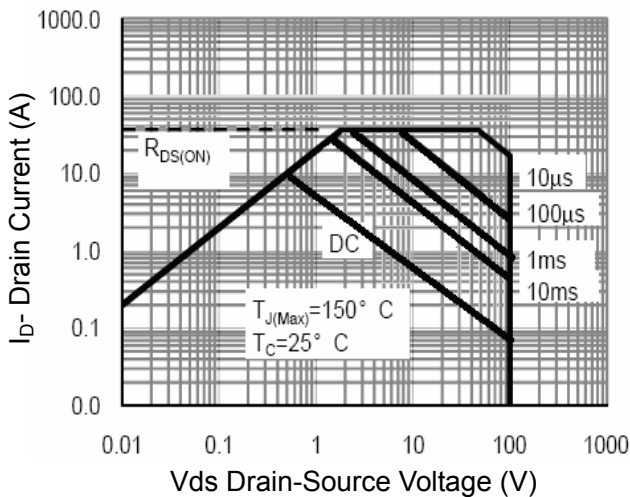


Figure 8 Safe Operation Area

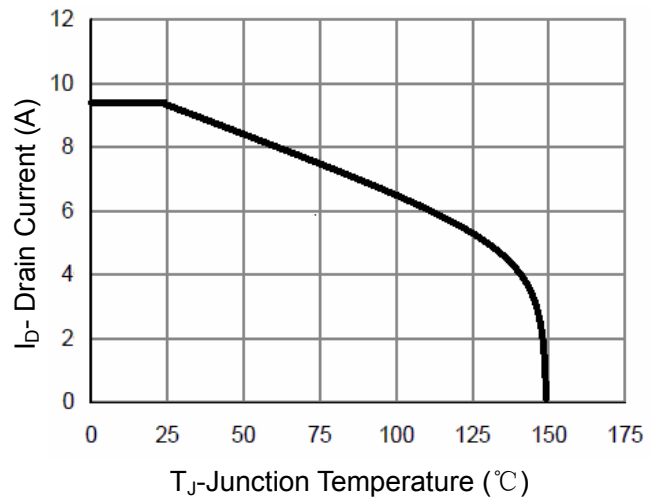


Figure 10 Current De-rating

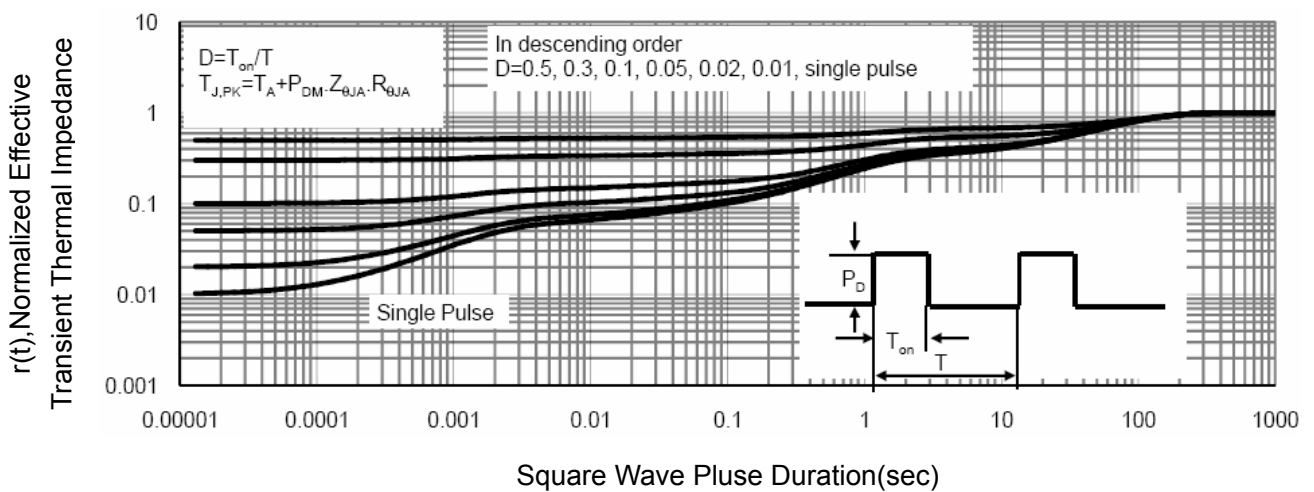
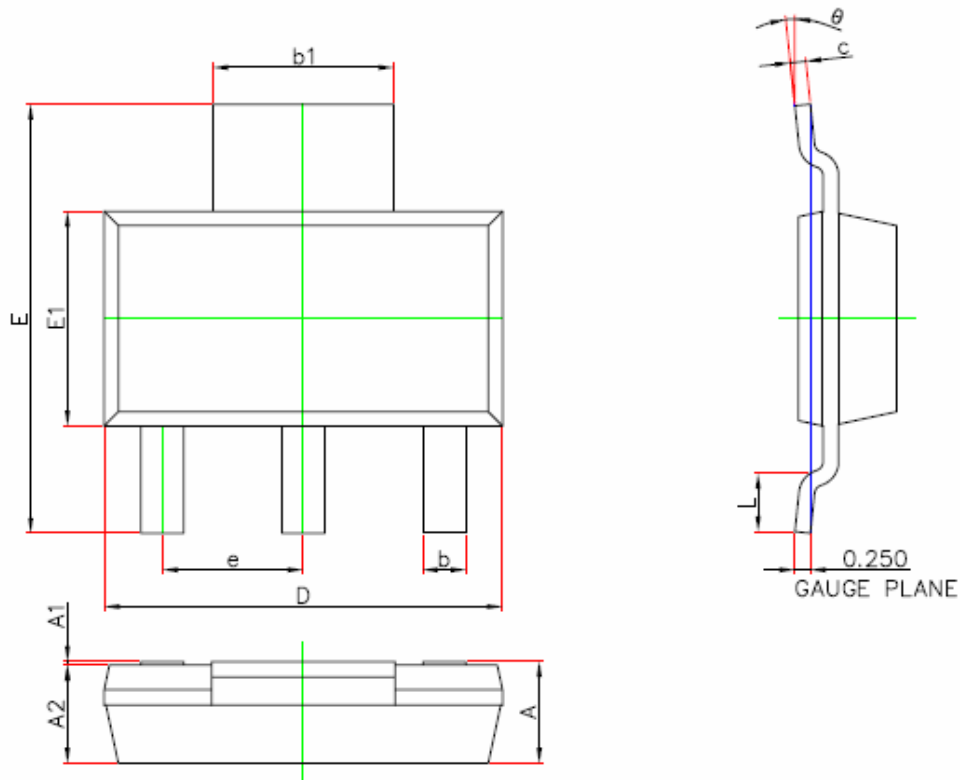


Figure 11 Normalized Maximum Transient Thermal Impedance

SOT-223 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	—	1.800	—	0.071
A1	0.020	0.100	0.001	0.004
A2	1.500	1.700	0.059	0.067
b	0.660	0.840	0.026	0.033
b1	2.900	3.100	0.114	0.122
c	0.230	0.350	0.009	0.014
D	6.300	6.700	0.248	0.264
E	6.700	7.300	0.264	0.287
E1	3.300	3.700	0.130	0.146
e	2.300(BSC)		0.091(BSC)	
L	0.750	—	0.030	—
θ	0°	10°	0°	10°

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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