

#### NCE N-Channel Enhancement Mode Power MOSFET

#### **Description**

The NCE1507AK uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

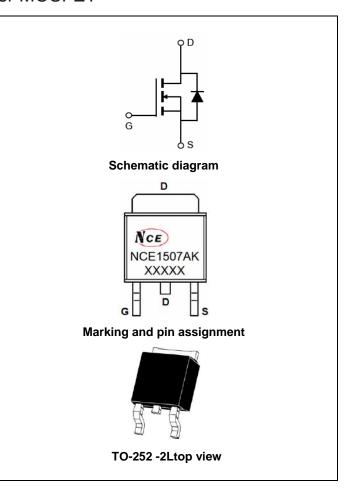
#### **General Features**

- $V_{DS}$  = 150V, $I_D$  = 7A  $R_{DS(ON)}$  < 290mΩ @  $V_{GS}$ =10V (Typ:255mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

# **Application**

- Power switching application
- Hard switched and high frequency circuits

100% UIS TESTED!



#### **Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE1507AK	NCE1507AK	TO-252-2L	-	-	-

#### Absolute Maximum Ratings (T<sub>C</sub>=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	150	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous	I <sub>D</sub>	7	Α
Drain Current-Pulsed (Note 1)	I <sub>DM</sub>	28	Α
Maximum Power Dissipation	P <sub>D</sub>	30	W
Operating Junction and Storage Temperature Range	$T_{J}$ , $T_{STG}$	-55 To 175	$^{\circ}$

#### **Thermal Characteristic**

Thermal Resistance,Junction-to-Case (Note 2)	R <sub>θJC</sub>	5	°C/W
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# Electrical Characteristics (T<sub>C</sub>=25 ℃ unless otherwise noted)

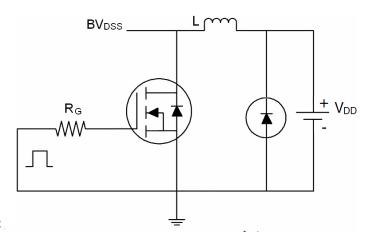
Parameter	Symbol	Condition	Min	Тур	Max	Unit		
Off Characteristics								
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	150	-	-	V		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =150V,V <sub>GS</sub> =0V	-	-	1	μA		
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA		
On Characteristics (Note 3)	<u> </u>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	1.5	2	2.5	V		
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =7A	-	255	290	mΩ		
Gate resistance	$R_{G}$		-	1.7	-	Ω		
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =5V,I <sub>D</sub> =7A	-	3	-	S		
Dynamic Characteristics (Note4)								
Input Capacitance	C <sub>lss</sub>	\/ -75\/\/ -0\/	-	550	-	PF		
Output Capacitance	Coss	$V_{DS}$ =75V, $V_{GS}$ =0V, F=1.0MHz	-	56	-	PF		
Reverse Transfer Capacitance	C <sub>rss</sub>	F-1.0MHZ	-	35	-	PF		
Switching Characteristics (Note 4)								
Turn-on Delay Time	t <sub>d(on)</sub>		-	8	-	nS		
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =75 $V$ , $R_L$ =10 $\Omega$	-	10	-	nS		
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}$ =10 $V$ , $R_{G}$ =6 $\Omega$	-	20	-	nS		
Turn-Off Fall Time	t <sub>f</sub>		-	15	-	nS		
Total Gate Charge	Qg	\/ -75\/  -74	-	17.6		nC		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ =75 $V$ , $I_{D}$ =7 $A$ , $V_{GS}$ =10 $V$	-	2.7	-	nC		
Gate-Drain Charge	$Q_{gd}$	V <sub>GS</sub> =10V	-	4.5	-	nC		
Drain-Source Diode Characteristics								
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =7A	-	-	1.2	V		
Diode Forward Current (Note 2)	I <sub>S</sub>		-	-	7	Α		

#### Notes:

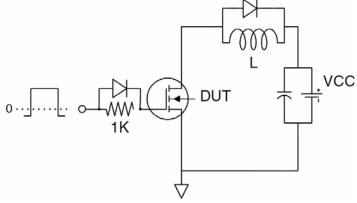
- **1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
- **2.** Surface Mounted on FR4 Board,  $t \le 10$  sec.
- 3. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2%.
- 4. Guaranteed by design, not subject to product

# **Test Circuit**

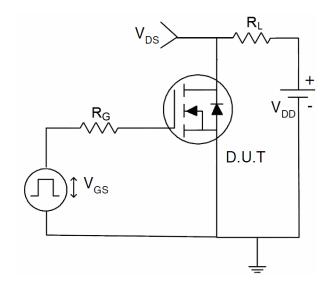
# 1) E<sub>AS</sub> Test Circuit



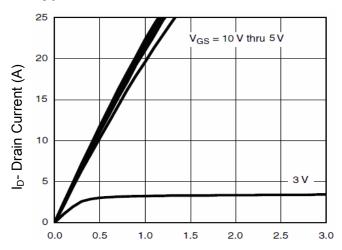
# 2) Gate Charge Test Circuit



#### 3) Switch Time Test Circuit

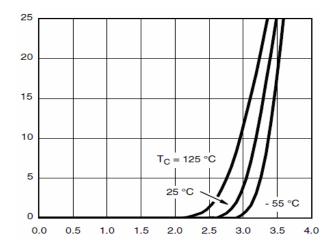


# **Typical Electrical and Thermal Characteristics (Curves)**



Vds Drain-Source Voltage (V)





Ip- Drain Current (A)

Vgs Gate-Source Voltage (V)

**Figure 2 Transfer Characteristics** 

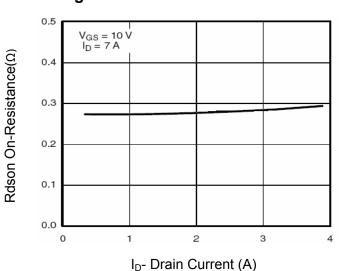
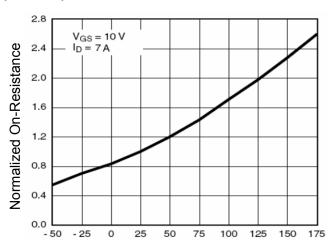
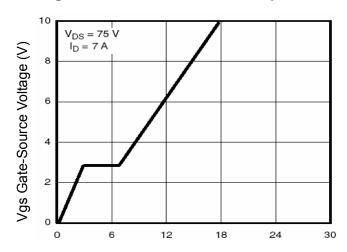


Figure 3 Rdson- Drain Current



T<sub>J</sub>-Junction Temperature(°C)

# **Figure 4 Rdson- Junction Temperature**



Qg Gate Charge (nC)

Figure 5 Gate Charge

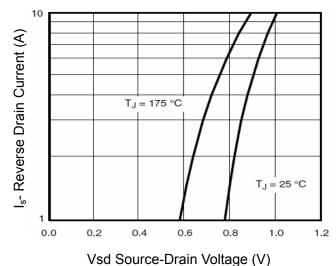


Figure 6 Source- Drain Diode Forward

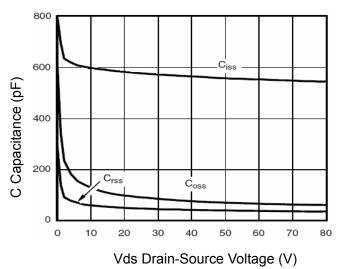
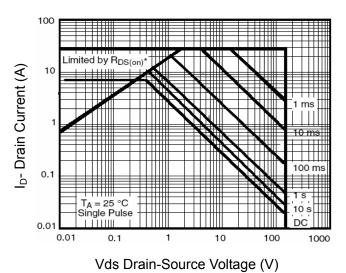
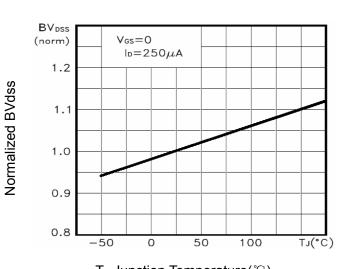


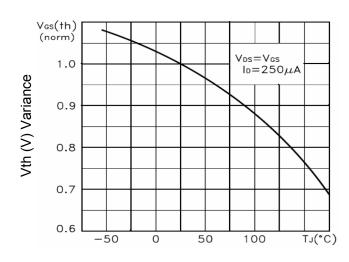
Figure 7 Capacitance vs Vds



**Figure 8 Safe Operation Area** 

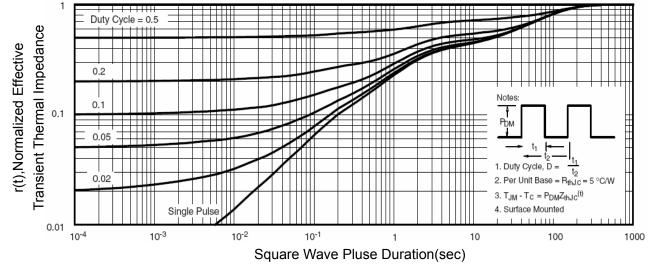


 $\label{eq:TJ-Junction} T_{\text{J}}\text{-Junction Temperature}(^{\circ}\!\mathbb{C}\,)$  Figure 9 BV<sub>DSS</sub> vs Junction Temperature



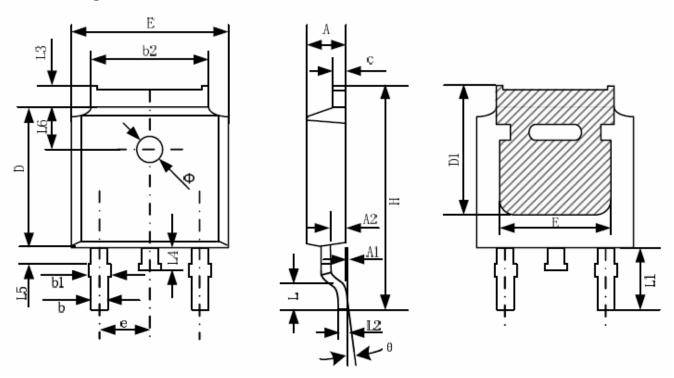
T<sub>J</sub>-Junction Temperature(°C)

Figure 10 V<sub>GS(th)</sub> vs Junction Temperature



**Figure 11 Normalized Maximum Transient Thermal Impedance** 

# **TO-252-2L Package Information**



O. mahad	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	2.20	2.38	0.087	0.094	
A1	0.00	0.10	0.000	0.004	
A2	0.90	1.10	0.035	0.043	
b	0.72	0.85	0.028	0.033	
b1	0.72	0.90	0.028	0.035	
b2	5.13	5.46	0.202	0.215	
С	0.47	0.60	0.019	0.024	
D	6.00	6.20	0.236	0.244	
D1	5.25		0.207	-	
Е	6.50	6.70	0.256	0.264	
E1	4.70		0.185	-	
e	2.19	2.39	0.086	0.094	
Н	9.80	10.40	0.386	0.409	
L	1.40	1.70	0.055	0.067	
L1	2.90 REF		0.114	REF	
L2	0.508	BSC	0.020 BSC		
L3	0.90	1.25	0.035	0.049	
L4	0.60	1.00	0.024	0.039	
L5	0.15	0.75	0.006	0.030	
L6	1.80	REF	0.071 REF		
Φ	1.20	1.40	0.047	0.055	
θ	0°	8°	0°	8°	





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