



N-Channel Super Junction Power MOSFET III

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent R_{DS(ON)} with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

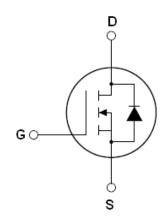
Features

- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- ●Ultra Low Gate Charge cause lower driving requirements
- ●100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)

V _{DS}	700	V
R _{DS(ON)TYP}	540	mΩ
I_D	8	A



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
NCE70T540I	TO-251	NCE70T540I
NCE70T540K	TO-252	NCE70T540K





TO-251

TO-252

Table 1. Absolute Maximum Ratings (T_c=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (Vgs=0V)	V _{DS}	700	V
Gate-Source Voltage (VDS=0V) ,AC (f>1 Hz)	V _G s	±30	V
Continuous Drain Current at Tc=25°C	I _{D (DC)}	8	Α
Continuous Drain Current at Tc=100°C	I _{D (DC)}	5.2	Α
Pulsed drain current (Note 1)	I _{DM (pluse)}	32	А
Maximum Power Dissipation(Tc=25°C)	P _D	69	W
Derate above 25°C		0.55	W/°C
Single pulse avalanche energy (Note2)	Eas	156	mJ
Avalanche current ^(Note 1)	I _{AR}	1.7	A
Repetitive Avalanche energy , t_{AR} limited by T_{jmax} (Note 1)	E _{AR}	0.3	mJ
Parameter	Symbol	Value	Unit



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Drain Source voltage slope, V _{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt, $V_{DS} \le 480 \text{ V}, I_{SD} < I_{D}$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55+150	°C

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R _{thJC}	1.81	°C /W
Thermal Resistance, Junction-to-Ambient (Maximum)	R _{thJA}	62	°C /W

Table 3. Electrical Characteristics (TA=25°Cunless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	700			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =700V,V _{GS} =0V			1	μA
Zero Gate Voltage Drain Current(Tc=125°C)	I _{DSS}	V _{DS} =700V,V _{GS} =0V			100	μΑ
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	3		4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =4A		540	600	mΩ
Dynamic Characteristics						
Input Capacitance	C _{Iss}	\/ -50\/\/ -0\/		590		pF
Output Capacitance	Coss	V_{DS} =50V, V_{GS} =0V, F=1.0MHz		37		pF
Reverse Transfer Capacitance	C _{rss}	Γ-1.UIVIΠZ		0.9		pF
Total Gate Charge	Qg	\/ -490\/ -94		14.6	22	nC
Gate-Source Charge	Q _{gs}	V _{DS} =480V,I _D =8A,		4		nC
Gate-Drain Charge	Q_{gd}	V _{GS} =10V		6.7		nC
Switching times						
Turn-on Delay Time	t _{d(on)}			9		nS
Turn-on Rise Time	t _r	V_{DD} =420 V , I_{D} =4 A ,		6.5		nS
Turn-Off Delay Time	t _{d(off)}	R_G =4.7 Ω , V_{GS} =10 V		61		nS
Turn-Off Fall Time	t _f			10		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T -25°C			8	Α
Pulsed Source-drain current(Body Diode)	I _{SDM}	T _C =25°C			32	Α
Forward On Voltage	V _{SD}	Tj=25°C,I _{SD} =8A,V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}			230		nS
Reverse Recovery Charge	Qrr	Tj=25°C,I _F =4A,di/dt=100A/µs		1.2		uC
Peak Reverse Recovery Current	I _{rrm}			10.5		Α

 ${\color{blue} \textbf{Notes: 1.}} \textbf{Repetitive Rating: Pulse width limited by maximum junction temperature}$

2. Tj=25°C,VDD=50V,VG=10V, R_G=25 Ω





TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure 1. Safe operating area

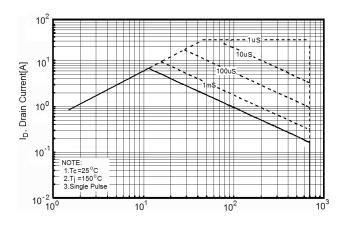


Figure 3. Source-Drain Diode Forward Voltage

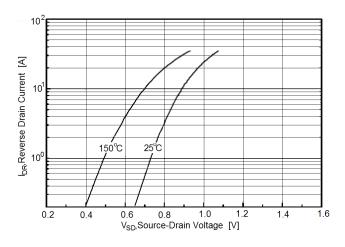


Figure 5. Transfer characteristics

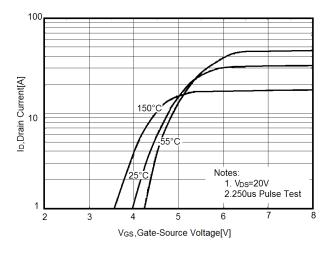


Figure 7. R_{DS(ON)} vs Junction Temperature

Figure 2. Transient Thermal Impedance

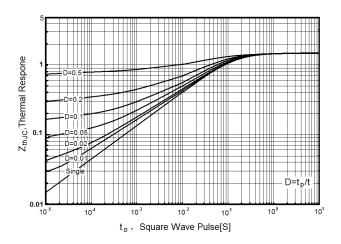


Figure 4. Output characteristics

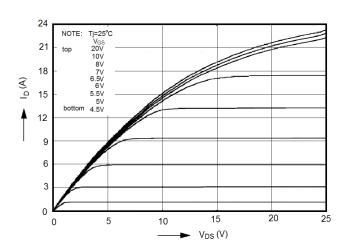


Figure 6. Static drain-source on resistance

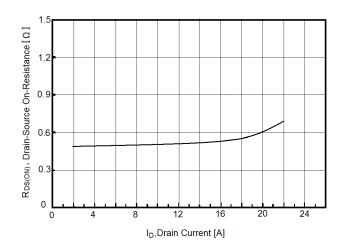
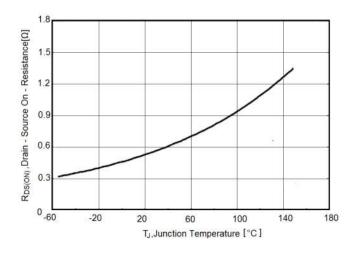


Figure 8. BV_{DSS} vs Junction Temperature



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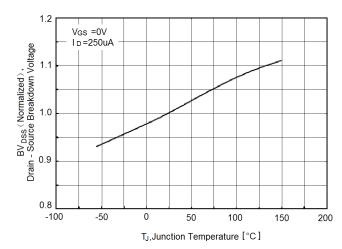


Figure 9. Maximum I_{D} vs Junction Temperature

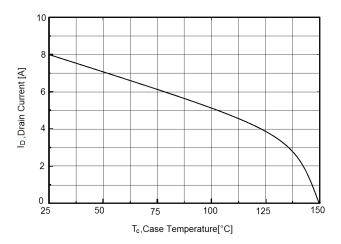


Figure 10. Capacitance

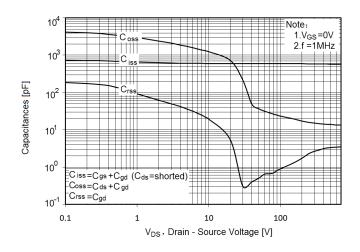
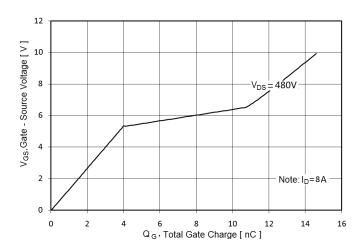


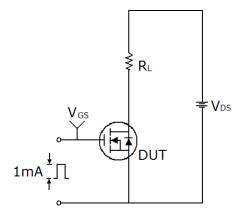
Figure 11. Gate charge waveforms

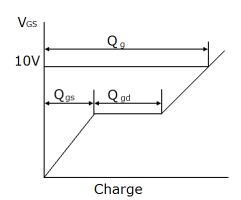




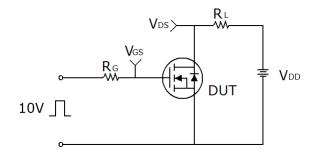
Test circuit

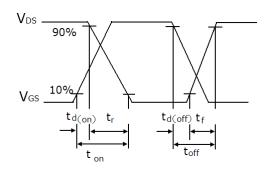
1) Gate charge test circuit & Waveform



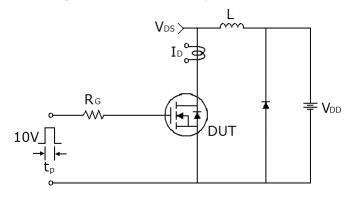


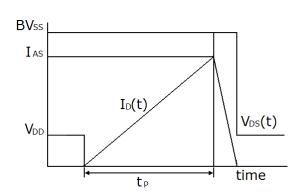
2) Switch Time Test Circuit:





3) Unclamped Inductive Switching Test Circuit & Waveforms

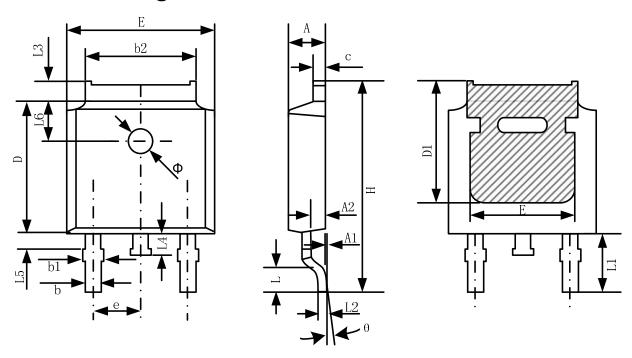




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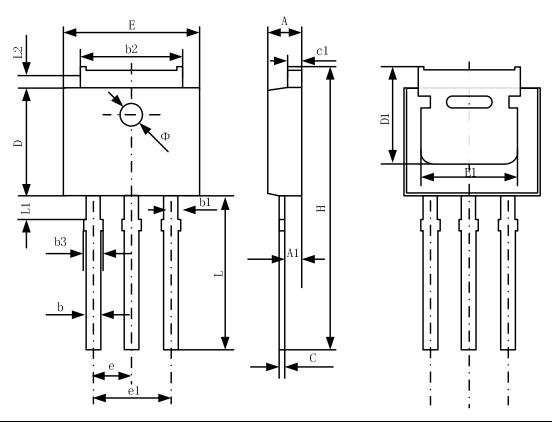
TO-252-2 Package Information



Camela al	Dimension	s In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	2.20	2.38	0.087	0.094	
A1	0.00	0.10	0.000	0.004	
A2	0.90	1.10	0.035	0.043	
b	0.72	0.85	0.028	0.033	
b1	0.72	0.90	0.028	0.035	
b2	5.13	5.46	0.202	0.215	
С	0.47	0.60	0.019	0.024	
D	6.00	6.20	0.236	0.244	
D1	5.25		0.207		
Е	6.50	6.70	0.256	0.264	
E1	4.70		0.185		
e	2.19	2.39	0.086	0.094	
Н	9.80	10.40	0.386	0.409	
L	1.40	1.70	0.055	0.067	
L1	2.9	90 REF	0.114 REF		
L2	0.5	0.508 BSC		D BSC	
L3	0.90	1.25	0.035	0.049	
L4	0.60	1.00	0.024	0.039	
L5	0.15	0.75	0.006	0.030	
L6	1.80 REF		0.071 REF		
Ф	1.20	1.40	0.047	0.055	
θ	0°	8°	0°	8°	



TO-251 Package Information



Symbol	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
Α	2.20	2.35	0.087	0.093	
A1	0.90	1.10	0.035	0.043	
b	0.56	0.69	0.022	0.027	
b1	0.77	0.90	0.030	0.035	
b2	5.23	5.43	0.206	0.214	
b3		1.05	0.000	0.041	
С	0.46	0.59	0.018	0.023	
c1	0.46	0.59	0.018	0.023	
D	6.00	6.20	0.236	0.244	
D1	5.20		0.205		
Е	6.50	6.70	0.256	0.264	
E1	4.60	5.00	0.181		
e	2.24	2.34	0.088	0.092	
e1	4.47	4.67	0.176	0.184	
Н	16.18	16.78	0.637	0.661	
L	9.00	9.60	0.354	0.378	
L1	0.95	1.35	0.037	0.053	
L2	0.90	1.25	0.035	0.049	



NCE70T540I, NCE70T540K

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