

# NCE N-Channel Super Trench Power MOSFET

#### Description

The NCEP0116K uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

#### **General Features**

• V<sub>DS</sub> =100V,I<sub>D</sub> =16A

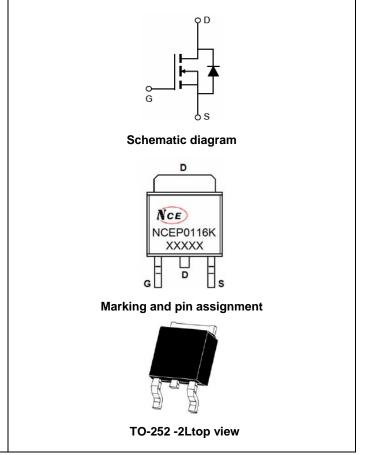
 $R_{DS(ON)}$ =78m $\Omega$  (typical) @ V<sub>GS</sub>=10V

- Excellent gate charge x R<sub>DS(on)</sub> product(FOM)
- Very low on-resistance R<sub>DS(on)</sub>
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

# Application

- LED backlighting
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!



### **Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP0116K	NCEP0116K	TO-252-2L	Ø330mm	12mm	2500 units

# Absolute Maximum Ratings (T<sub>A</sub>=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous	I <sub>D</sub>	16	А
Drain Current-Continuous(T <sub>C</sub> =100℃)	I <sub>D</sub> (100℃)	11.3	А
Pulsed Drain Current	I <sub>DM</sub>	64	А
Maximum Power Dissipation	PD	55	W
Derating factor		0.37	W/°C
Single pulse avalanche energy (Note 5)	E <sub>AS</sub>	26	mJ
Drain Source voltage slope, V⊳s ≤120 V,	dv/dt	50	V/ns
Drain Source voltage slope, V₀s ≤120 V, Is₀ <i₀< td=""><td>dv/dt</td><td>50</td><td>V/ns</td></i₀<>	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> ,T <sub>STG</sub>	-55 To 175	°C



### **Thermal Characteristic**

Thermal Résistance, Junction-to-Case <sup>(Note 2)</sup>	R <sub>ejc</sub>	2.7	°C <b>/W</b>
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#### Electrical Characteristics (T<sub>A</sub>=25<sup>°</sup>C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	·					
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250µA	100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V,V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	$V_{GS}$ =±20V, $V_{DS}$ =0V	-	-	±100	nA
On Characteristics (Note 3)	• •					
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	2.0	3.2	4.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =16A	-	78	95	mΩ
Gate resistance	R <sub>G</sub>		-	10	-	Ω
Forward Transconductance	<b>G</b> FS	V <sub>DS</sub> =5V,I <sub>D</sub> =16A	-	20	-	S
Dynamic Characteristics (Note4)	·					
Input Capacitance	C <sub>lss</sub>		-	322		PF
Output Capacitance	Coss	$V_{DS}$ =50V, $V_{GS}$ =0V,	-	53		PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.0MHz	-	5.1		PF
Switching Characteristics (Note 4)	• •		•			
Turn-on Delay Time	t <sub>d(on)</sub>		-	6	-	nS
Turn-on Rise Time	tr	$V_{DD}$ =50V, RL=3 $\Omega$	-	3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}$ =10V, $R_{G}$ =3 $\Omega$	-	18	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	3	-	nS
Total Gate Charge	Qg		-	5.6	-	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =50V,I <sub>D</sub> =10A, V <sub>GS</sub> =10V	-	2.4	-	nC
Gate-Drain Charge	Q <sub>gd</sub>	V <sub>GS</sub> =10V	-	1.3	-	nC
Drain-Source Diode Characteristics	· ·					
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =10A	-	-	1.2	V
Diode Forward Current (Note 2)	Is		-	-	16	Α
Reverse Recovery Time	t <sub>rr</sub>	$T_J$ = 25°C, $I_F$ = $I_S$	-	15	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs <sup>(Note3)</sup>	-	53	-	nC

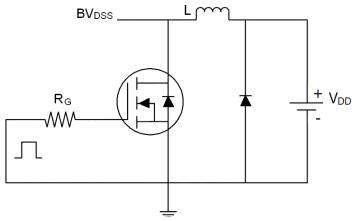
#### Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board,  $t \le 10$  sec.
- 3. Pulse Test: Pulse Width ≤ 300 $\mu$ s, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- 5. EAS condition : Tj=25  $^\circ \! \mathrm{C}$  ,V\_DD=50V,V\_G=10V,L=0.5mH,Rg=25 $\Omega$

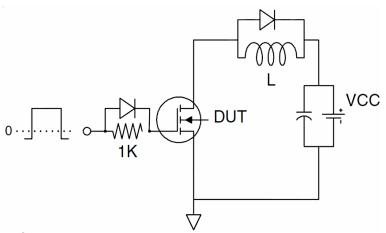


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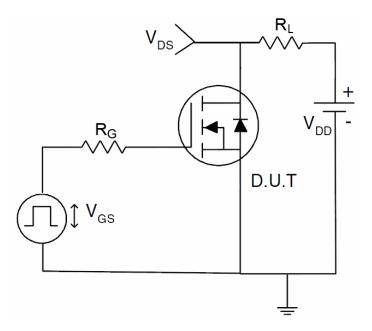
# Test Circuit 1) E<sub>AS</sub> test Circuit



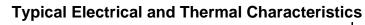
## 2) Gate charge test Circuit

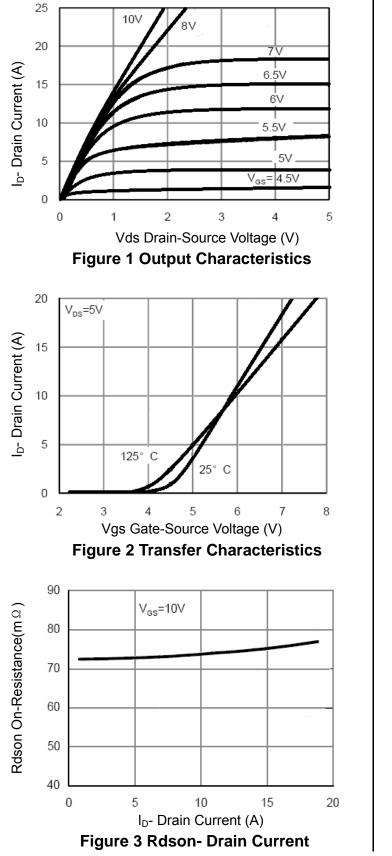


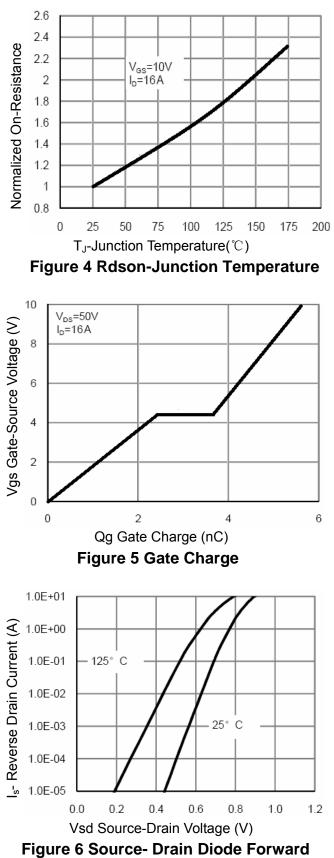
3) Switch Time Test Circuit













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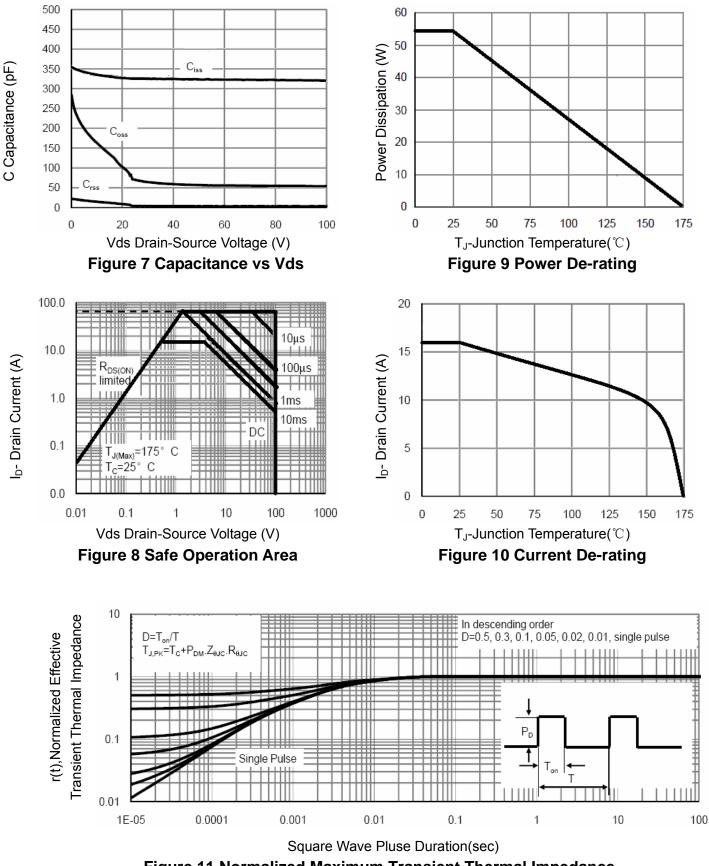


Figure 11 Normalized Maximum Transient Thermal Impedance



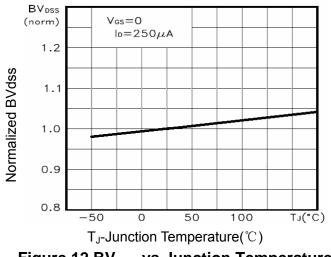
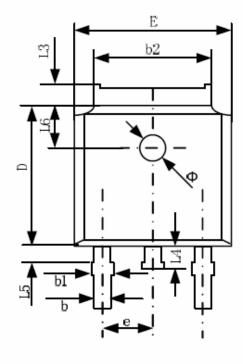
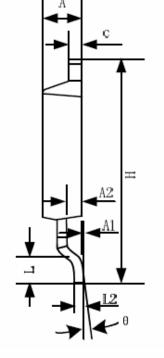


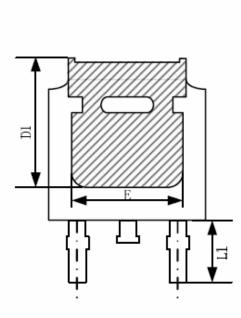
Figure 12 BV<sub>DSS</sub> vs Junction Temperature



# **TO-252-2L Package Information**







Querra ha a l	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	2.20	2.38	0.087	0.094	
A1	0.00	0.10	0.000	0.004	
A2	0.90	1.10	0.035	0.043	
b	0.72	0.85	0.028	0.033	
b1	0.72	0.90	0.028	0.035	
b2	5.13	5.46	0.202	0.215	
с	0.47	0.60	0.019	0.024	
D	6.00	6.20	0.236	0.244	
D1	5.25		0.207		
E	6.50	6.70	0.256	0.264	
E1	4.70		0.185		
e	2.19	2.39	0.086	0.094	
н	9.80	10.40	0.386	0.409	
L	1.40	1.70	0.055	0.067	
L1	2.9	0 REF	0.114 REF		
L2	0.50	8 BSC	0.020 BSC		
L3	0.90	1.25	0.035	0.049	
L4	0.60	1.00	0.024	0.039	
L5	0.15	0.75	0.006	0.030	
L6	1.80 REF		0.071 REF		
Φ	1.20	1.40	0.047	0.055	
θ	0°	8°	0°	8°	



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