

NCE N-Channel Super Trench II Power MOSFET

Description

The series of devices uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

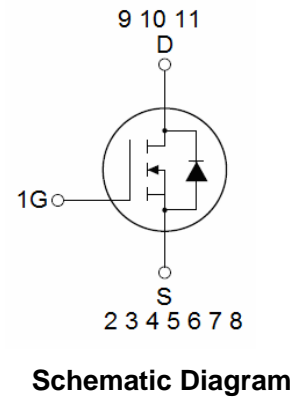
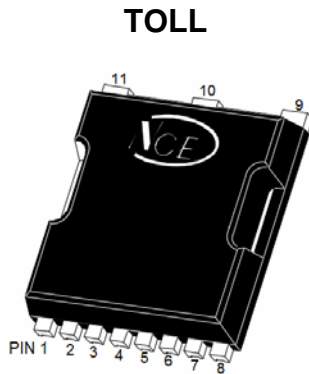
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS} = 85V, I_D = 360A$
 $R_{DS(ON)} = 1.2m\Omega$, typical @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔVds TESTED!



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP016N85LL	NCEP016N85LL	TOLL	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	85	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	360	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	252	A
Pulsed Drain Current	I_{DM}	1440	A
Maximum Power Dissipation	P_D	460	W
Derating factor		3.1	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	2850	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.33	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	85		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=85V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=180A$	-	1.2	1.6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=180A$		210	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	15800	-	PF
Output Capacitance	C_{oss}		-	2450	-	PF
Reverse Transfer Capacitance	C_{rss}		-	111	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=180A$ $V_{GS}=10V, R_G=1.6\Omega$	-	43	-	nS
Turn-on Rise Time	t_r		-	39	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	108	-	nS
Turn-Off Fall Time	t_f		-	40	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=180A,$ $V_{GS}=10V$	-	245	-	nC
Gate-Source Charge	Q_{gs}		-	66		nC
Gate-Drain Charge	Q_{gd}		-	65		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=180A$	-		1.2	V
Diode Forward Current	I_S		-	-	360	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 180A$ $di/dt = 100A/\mu s$ (Note 3)	-	109	-	nS
Reverse Recovery Charge	Q_{rr}		-	315	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=40V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

Typical Electrical and Thermal Characteristics

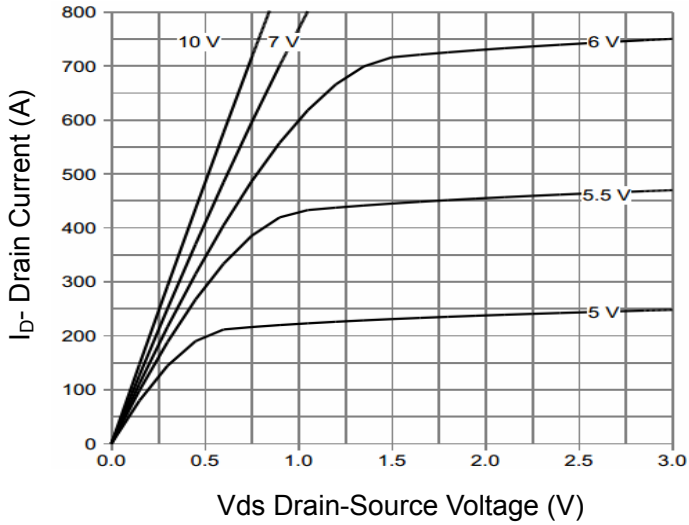


Figure 1 Output Characteristics

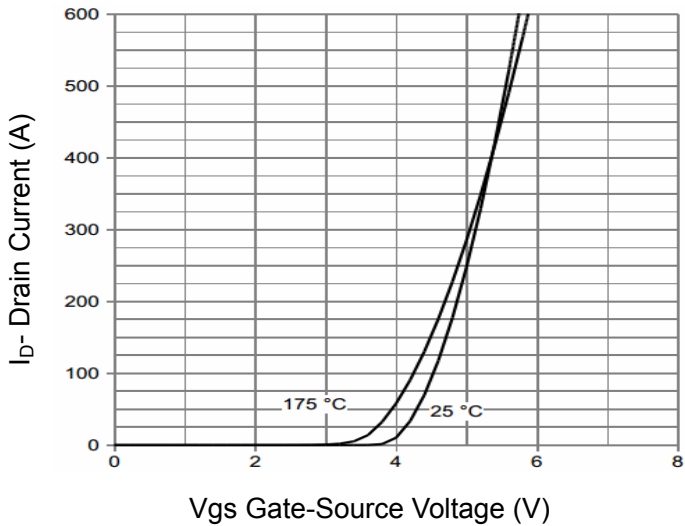


Figure 2 Transfer Characteristics

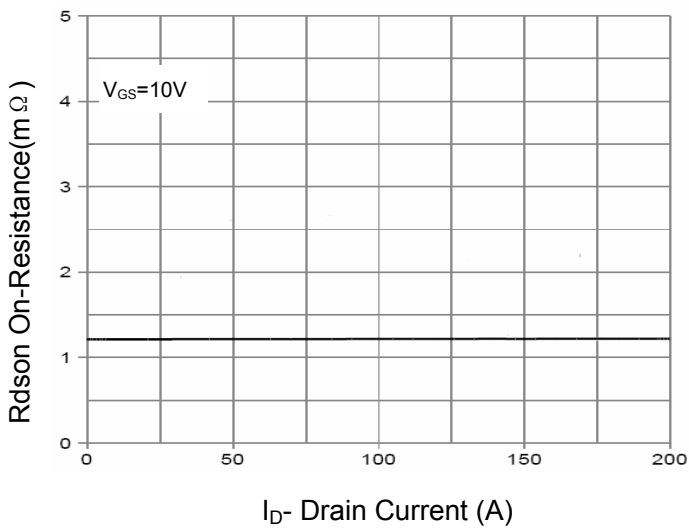


Figure 3 $R_{DS(on)}$ - Drain Current

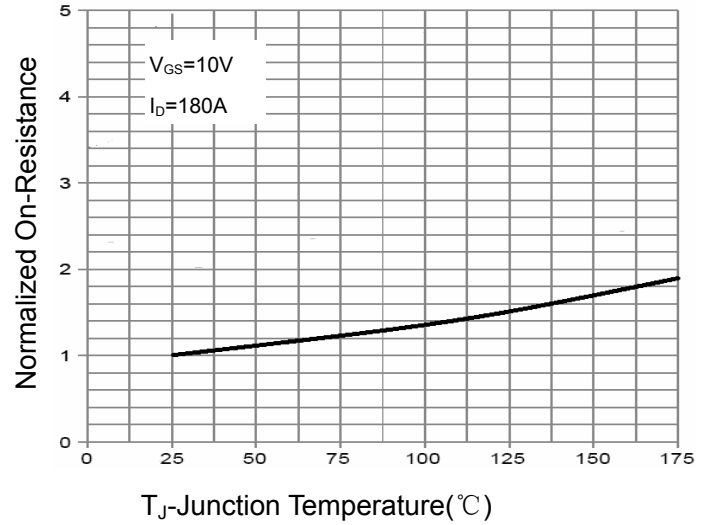


Figure 4 $R_{DS(on)}$ -Junction Temperature

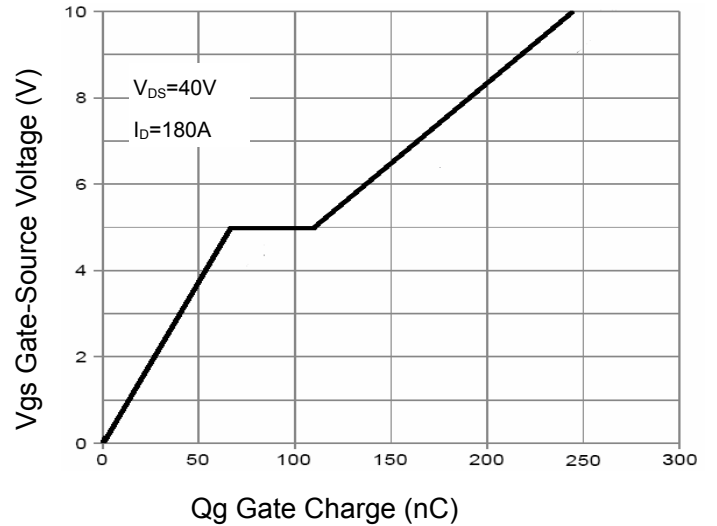


Figure 5 Gate Charge

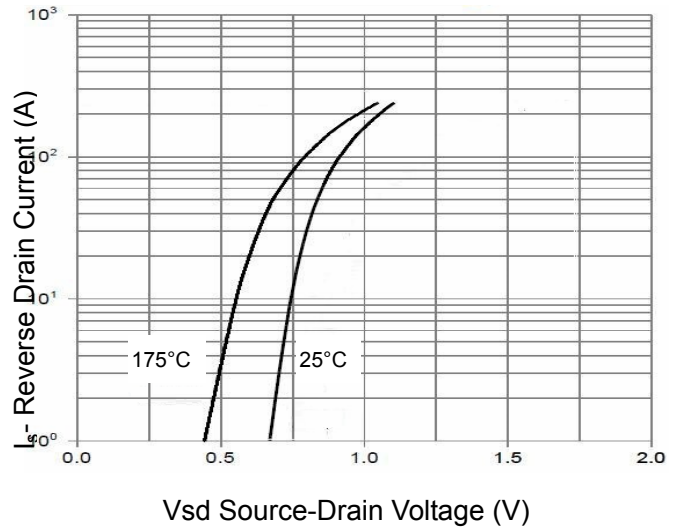
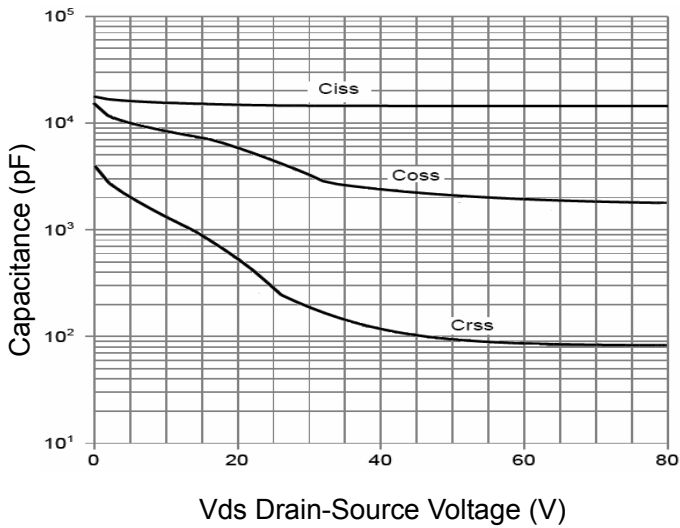
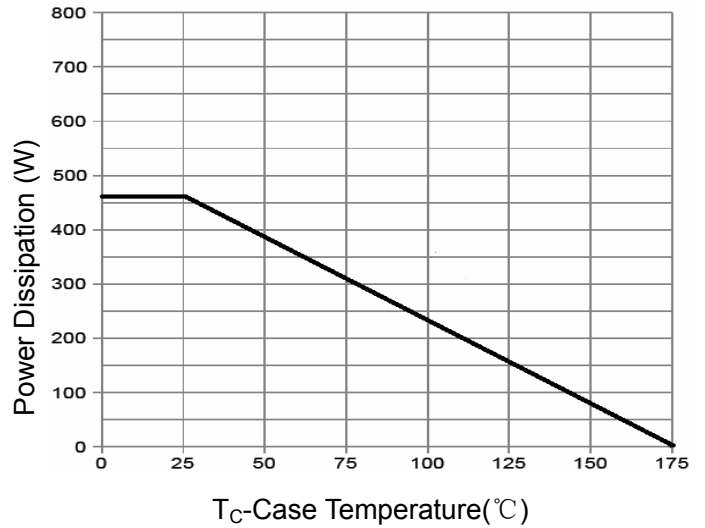


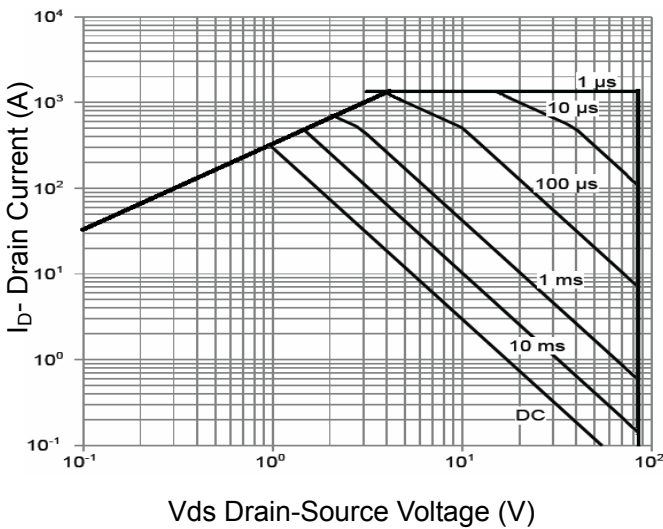
Figure 6 Source- Drain Diode Forward



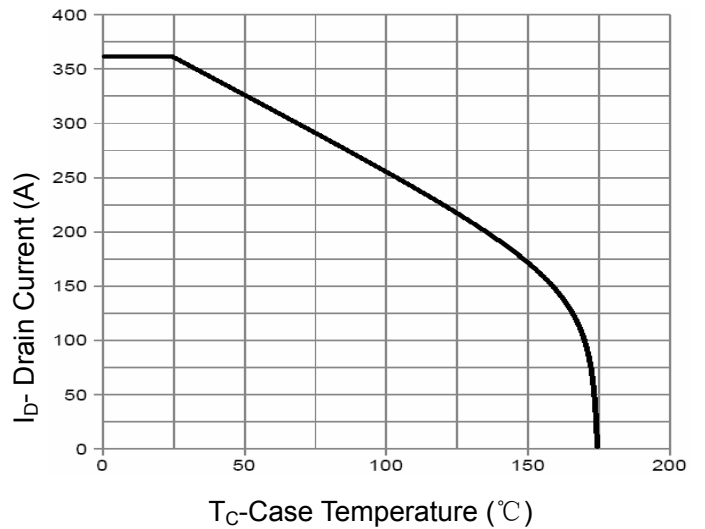
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_C-Case Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_C-Case Temperature (°C)
Figure 10 Current De-rating

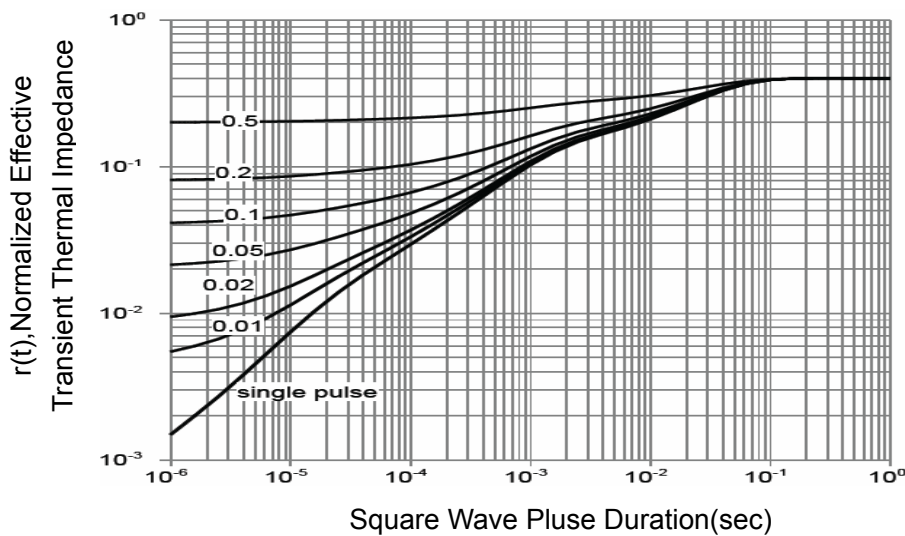
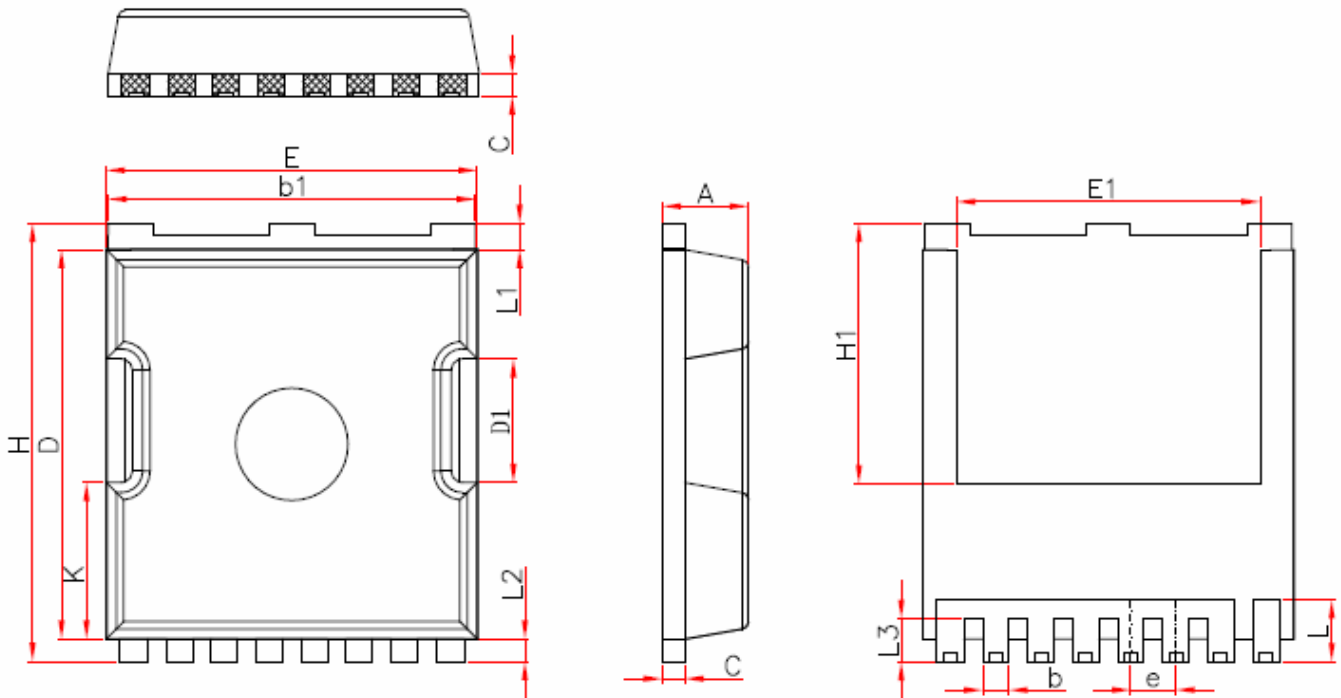


Figure 11 Normalized Maximum Transient Thermal Impedance

TOLL Package Information



Symbol	Millimeters		
	Min.	Nom.	Max.
A	2.20	2.30	2.40
b	0.65	0.75	0.85
b1	9.70	9.80	9.90
C	0.50	0.60	0.70
D	10.30	10.40	10.50
D1	3.15	3.3	3.45
E	9.70	9.90	10.10
E1	8.00	8.10	8.20
e	1.10	1.20	1.30
H	11.6	11.7	11.8
H1	6.85	6.95	7.05
K	4.08	4.18	4.28
L	1.60	1.65	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.05	1.20	1.30

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