

NCE N-Channel Super Trench II Power MOSFET

Description

The series of devices uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

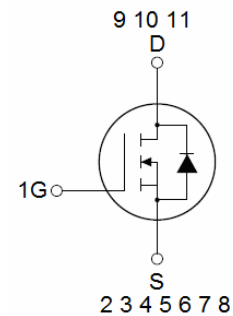
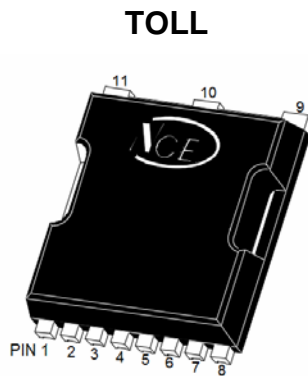
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS} = 100V, I_D = 300A$
 $R_{DS(ON)} = 1.7m\Omega$, typical @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!

100% ΔVds TESTED!



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP023N10LL	NCEP023N10LL	TOLL	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	300	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	220	A
Pulsed Drain Current	I_{DM}	1200	A
Maximum Power Dissipation	P_D	380	W
Derating factor		2.5	W/°C
Single pulse avalanche energy ^(Note 4)	E_{AS}	2800	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.4	°C/W
Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	60	°C/W

Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 2)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =150A	-	1.7	2.3	mΩ
Gate resistance	R _G		-	2.0	-	Ω
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =150A		200	-	S
Dynamic Characteristics (Note3)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	14000	-	PF
Output Capacitance	C _{oss}		-	1100	-	PF
Reverse Transfer Capacitance	C _{rss}		-	74	-	PF
Switching Characteristics (Note 3)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =150A V _{GS} =10V, R _G =1.6Ω	-	34	-	nS
Turn-on Rise Time	t _r		-	27	-	nS
Turn-Off Delay Time	t _{d(off)}		-	78	-	nS
Turn-Off Fall Time	t _f		-	30	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =150A, V _{GS} =10V	-	240	-	nC
Gate-Source Charge	Q _{gs}		-	62		nC
Gate-Drain Charge	Q _{gd}		-	73		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =150A	-		1.2	V
Diode Forward Current	I _S		-	-	300	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 150A	-	101	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note2)	-	280	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.
3. Guaranteed by design, not subject to production
4. EAS condition : T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω

Typical Electrical and Thermal Characteristics

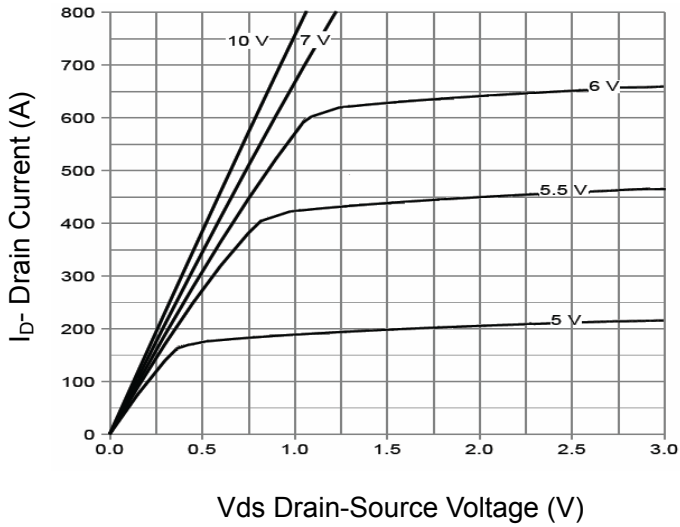


Figure 1 Output Characteristics

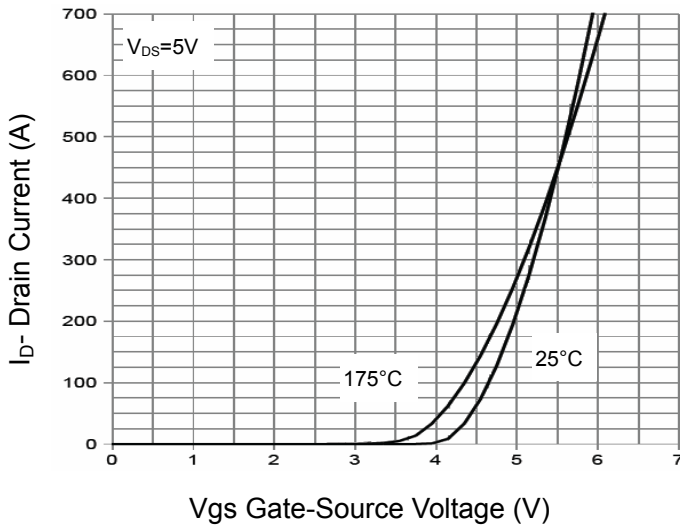


Figure 2 Transfer Characteristics

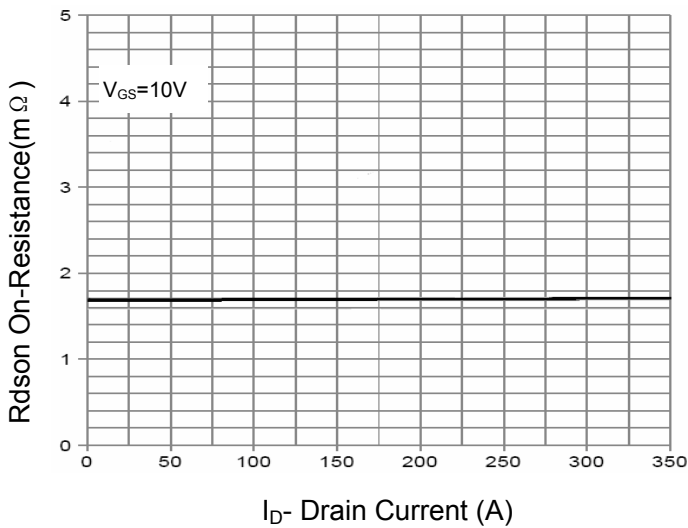


Figure 3 $R_{DS(on)}$ - Drain Current

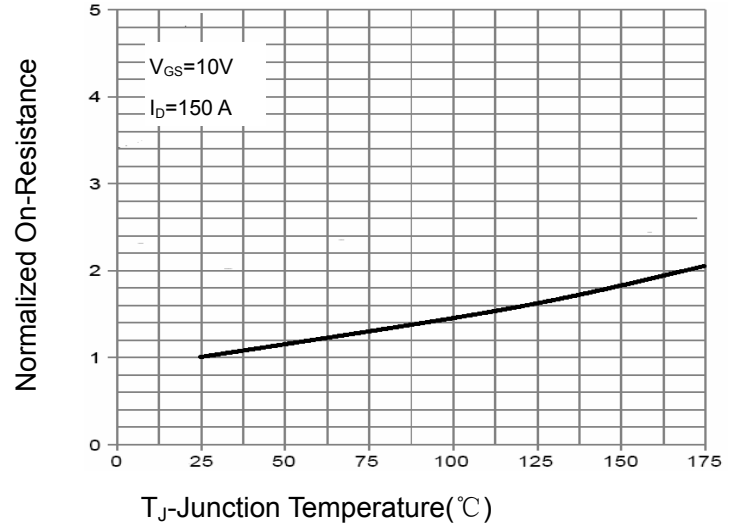


Figure 4 $R_{DS(on)}$ -Junction Temperature

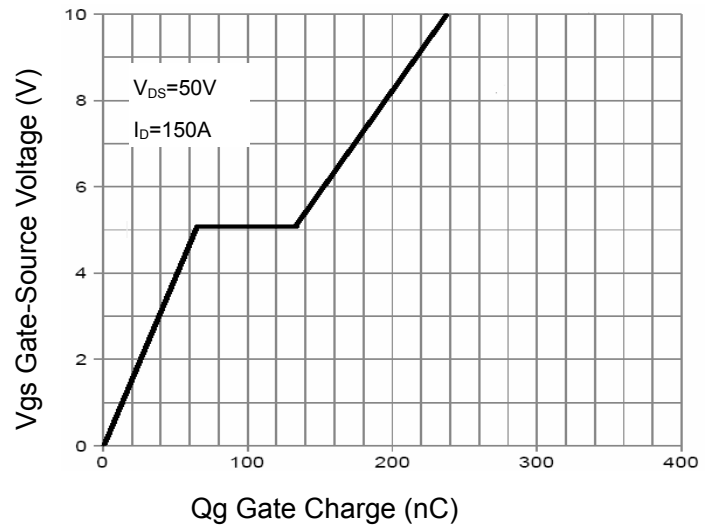


Figure 5 Gate Charge

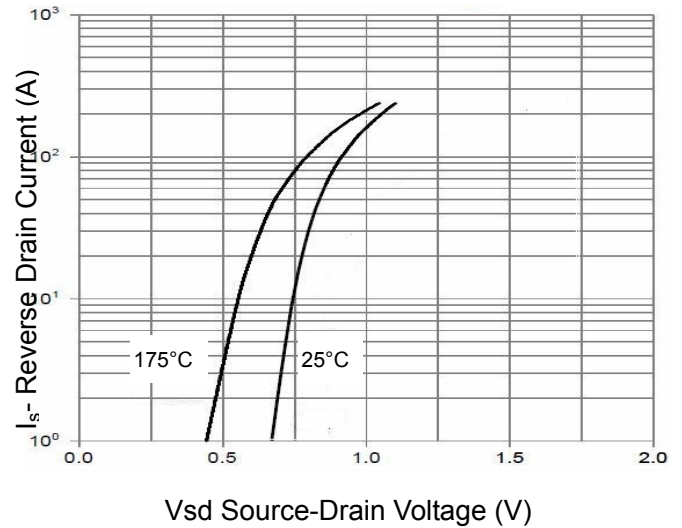
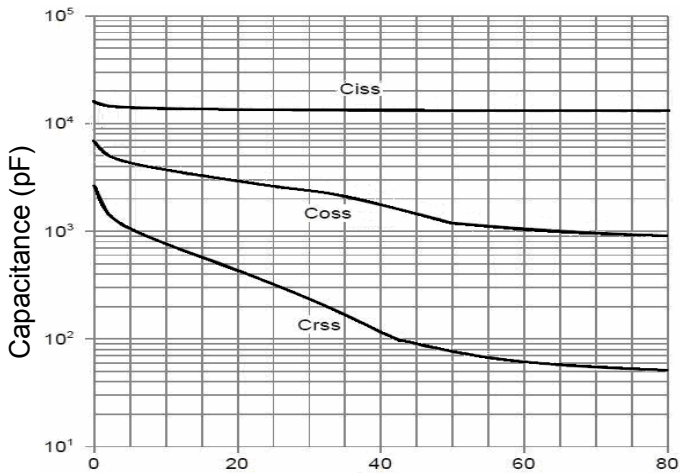
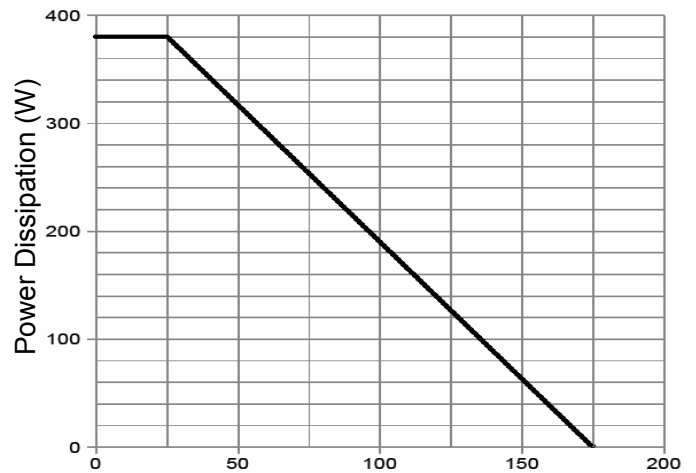


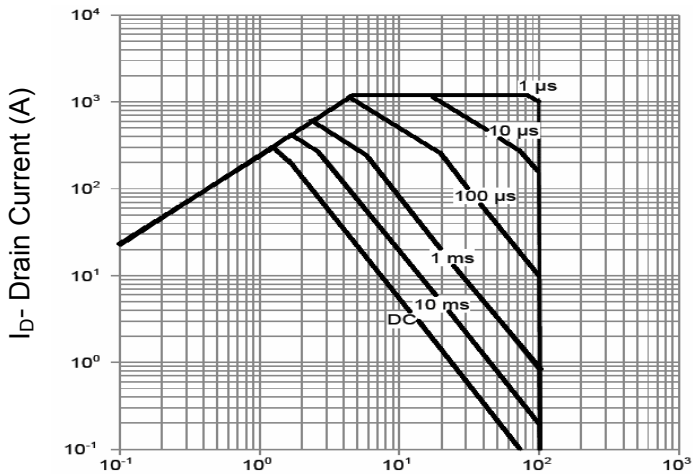
Figure 6 Source- Drain Diode Forward



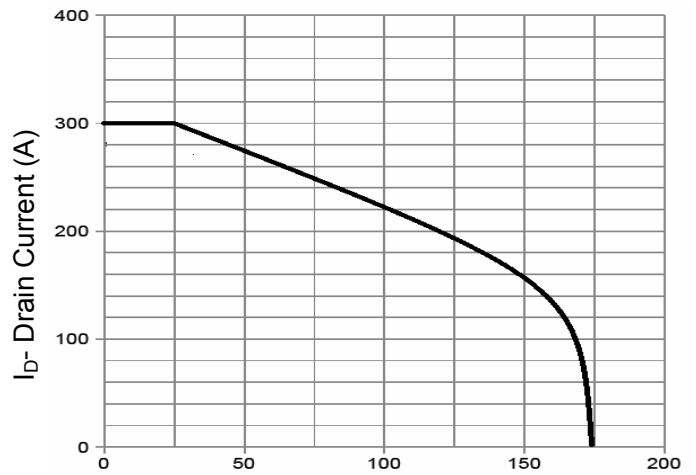
V_{ds} Drain-Source Voltage (V)
Figure 7 Capacitance vs V_{ds}



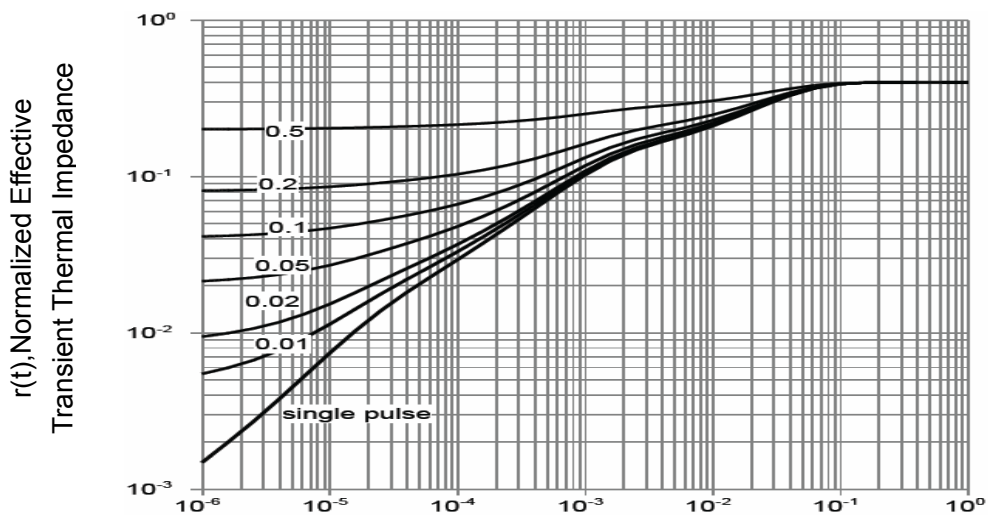
T_C-Case Temperature(°C)
Figure 9 Power De-rating



V_{ds} Drain-Source Voltage (V)
Figure 8 Safe Operation Area

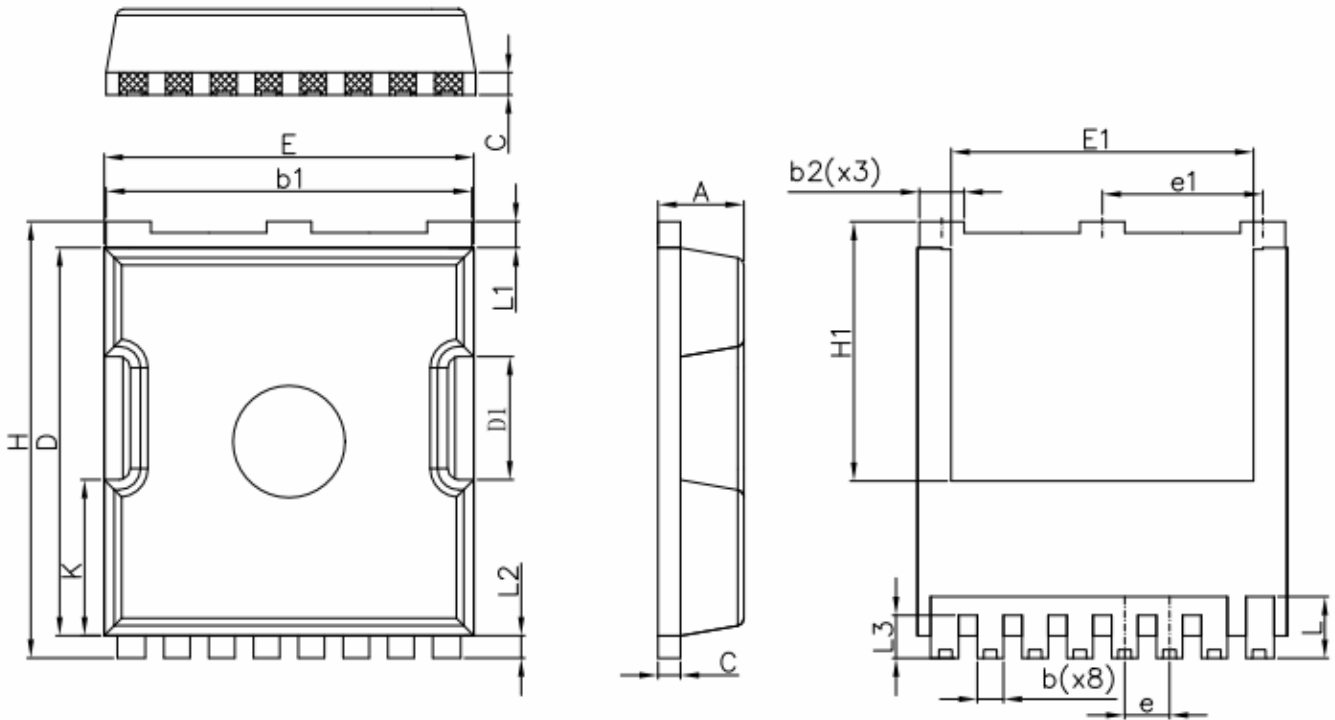


T_C-Case Temperature (°C)
Figure 10 Current De-rating



Square Wave Pulse Duration(sec)
Figure 11 Normalized Maximum Transient Thermal Impedance

TOLL Package Information



TOLL-8L			
DIM.	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
b	0.65	0.75	0.85
b1	9.70	9.80	9.90
b2	1.10	1.20	1.30
C	0.50	0.60	0.70
D	10.30	10.40	10.50
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	8.00	8.10	8.20
e	1.10	1.20	1.30
e1	4.20	4.30	4.40
H	11.60	11.70	11.80
H1	6.85	6.95	7.05
K	4.08	4.18	4.28
L	1.60	1.65	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.05	1.20	1.30
All dimensions in millimeters			

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