NCE N-Channel Super Trench Power MOSFET

Description

The NCEP1505S uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g. This device is ideal for high-frequency switching and synchronous rectification.

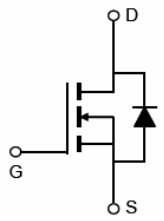
General Features

- V_{DS} =150V,I_D =5.1A
  $R_{DS(ON)}$ < 65mΩ @ V_{GS}=10V (Typ: 55mΩ)
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature

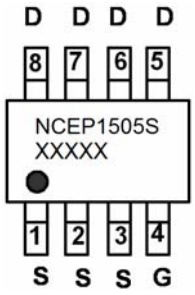
Application

- DC/DC converters and Off-Line UPS
- High Voltage Synchronous Rectifier
- Hard switched and high frequency circuits
- Uninterruptible power supply

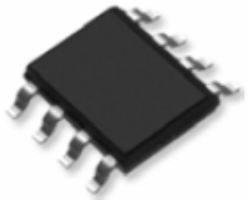
100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP1505S	NCEP1505S	SOP-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous		I_D	5.1	A
Drain Current-Continuous(T_C=100℃)		I_D (100℃)	3.6	A
Pulsed Drain Current(Note 1)		I_{DM}	20	A
Single pulse avalanche energy (Note 5)		E_{AS}	60	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	5	W
	T_A = 25 °C		3	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	41.7	℃/W
Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	25	

Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	150	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.3	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.1A	-	55	65	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=5.1A	-	12.5	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=75V,V_{GS}=0V, F=1.0MHz	-	550	730	PF
Output Capacitance	C_{oss}		-	62	80	PF
Reverse Transfer Capacitance	C_{rss}		-	2.5	4.5	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=75V, I_D=5.1A V_{GS}=10V,R_G=3Ω	-	7.5	14	nS
Turn-on Rise Time	t_r		-	1.4	8.5	nS
Turn-Off Delay Time	$t_{d(off)}$		-	12.5	21	nS
Turn-Off Fall Time	t_f		-	2.5	8	nS
Total Gate Charge	Q_g	V_{DS}=75V,I_D=5.1A, V_{GS}=10V	-	8.5	12	nC
Gate-Source Charge	Q_{gs}		-	2.8		nC
Gate-Drain Charge	Q_{gd}		-	1.9		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=5.1A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	5.1	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F = I_S di/dt = 100A/μs (Note3)	-	58	95	nS
Reverse Recovery Charge	Qrr		-	69	110	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design.

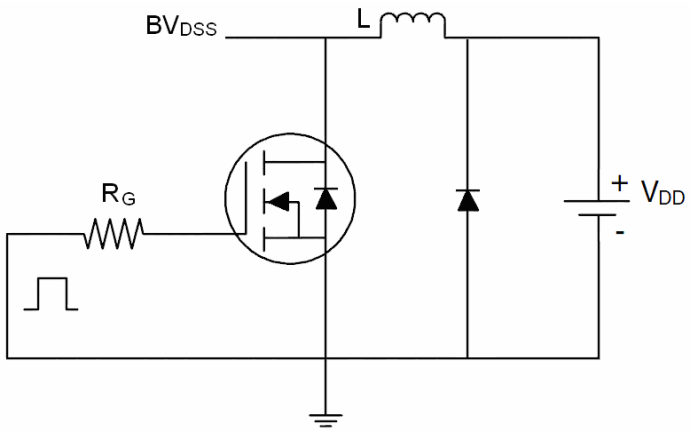
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

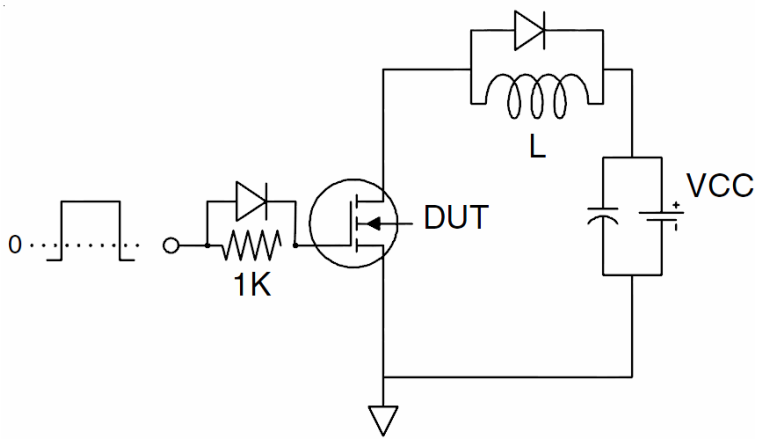
5. EAS condition : Tj=25℃,V_{DD}=50V,V_G=10V,L=0.5mH,Rg=25Ω

Test Circuit

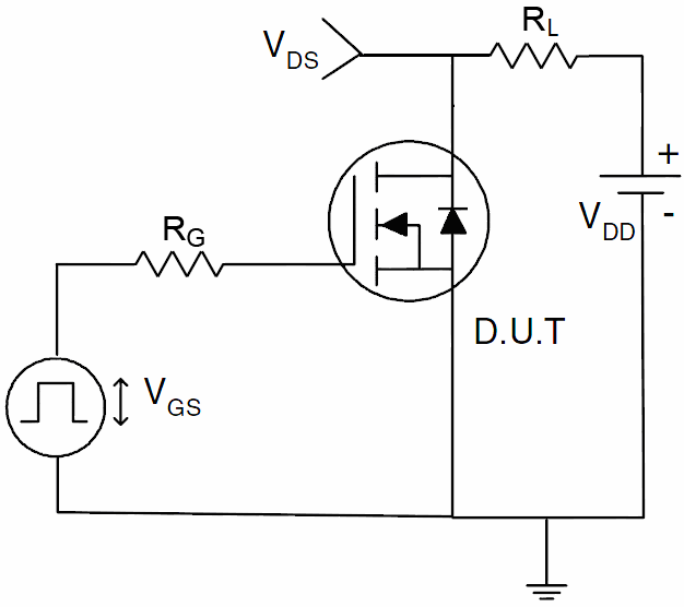
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

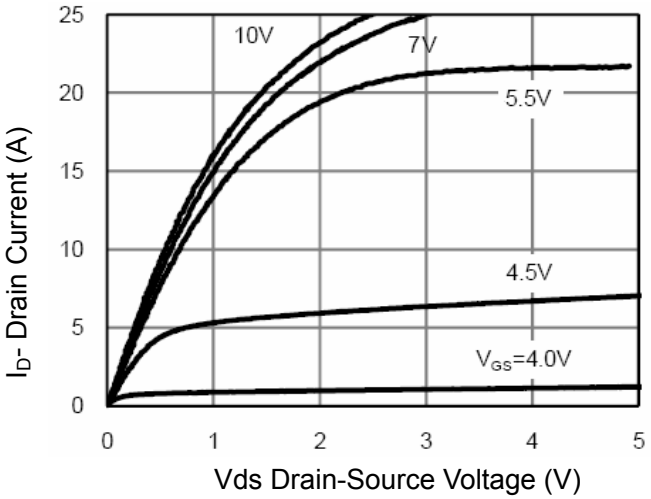


Figure 1 Output Characteristics

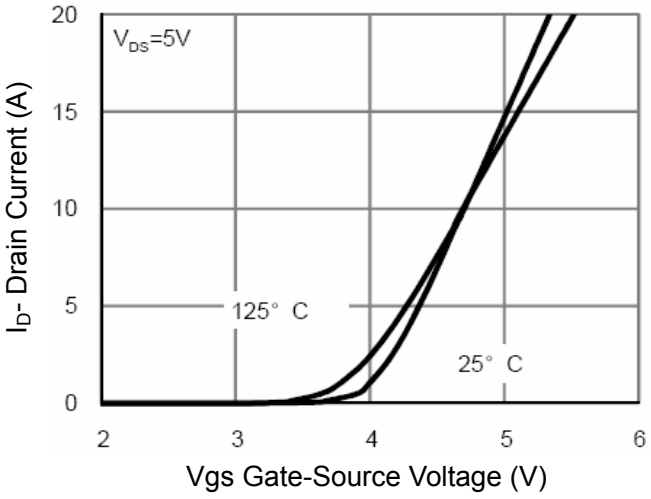


Figure 2 Transfer Characteristics

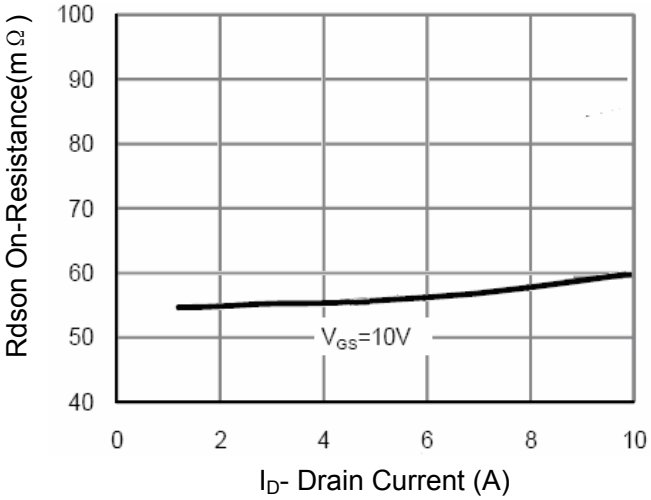


Figure 3 Rdson- Drain Current

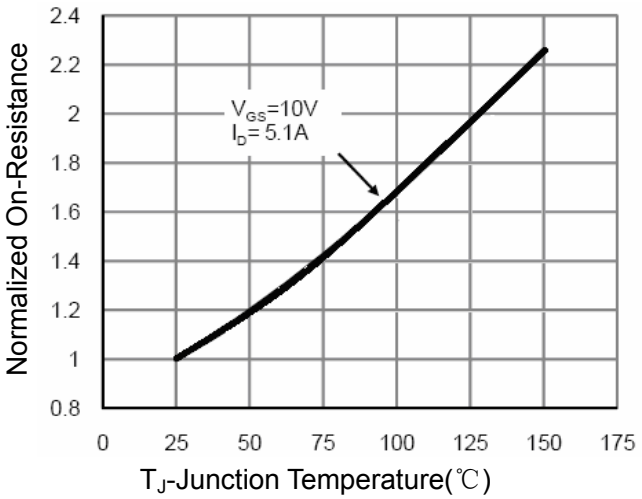


Figure 4 Rdson-JunctionTemperature

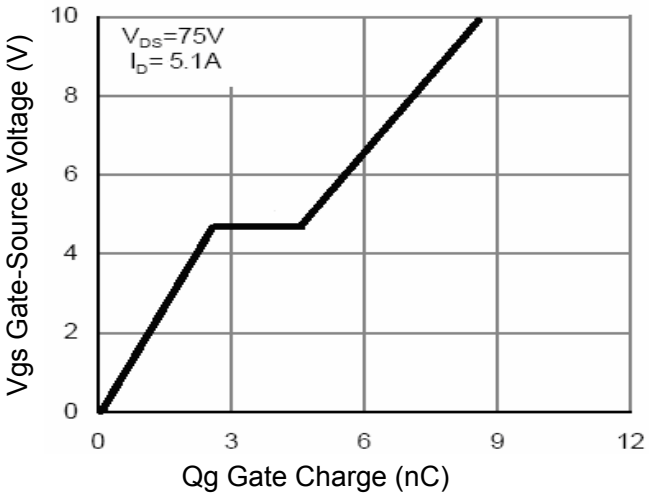


Figure 5 Gate Charge

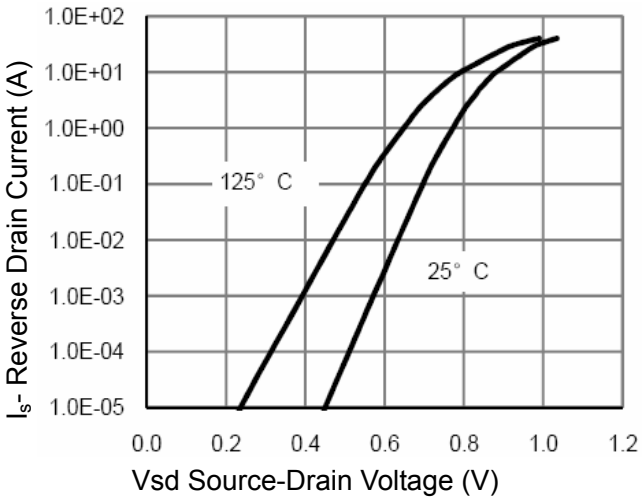


Figure 6 Source- Drain Diode Forward

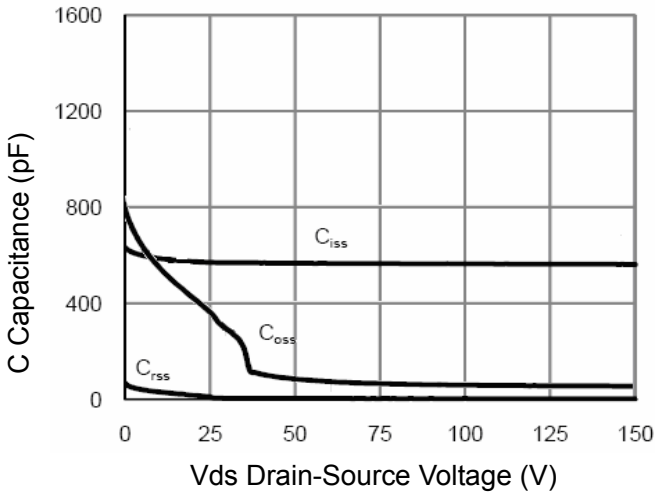


Figure 7 Capacitance vs Vds

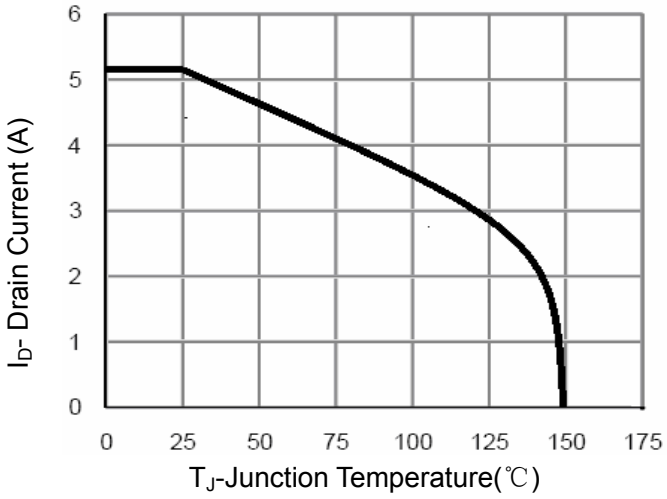


Figure 9 Current De-rating

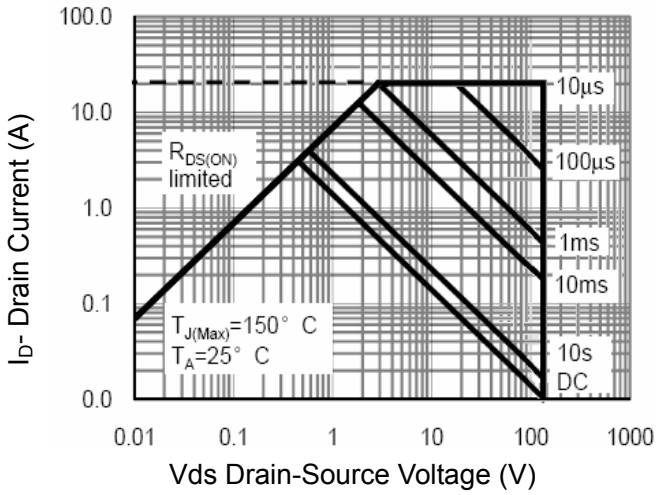


Figure 8 Safe Operation Area

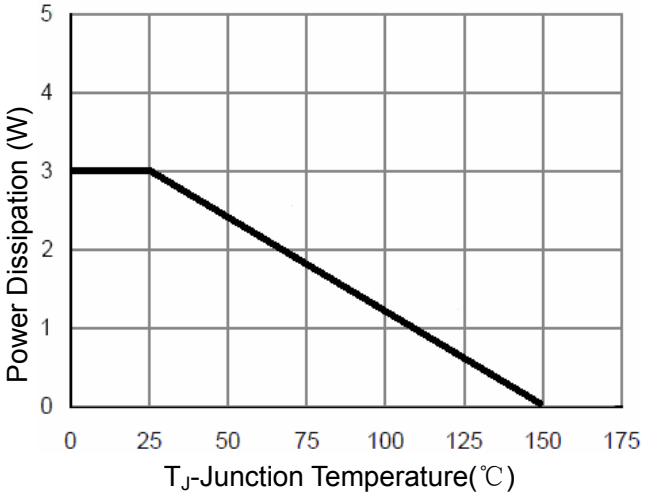


Figure 10 Power De-rating

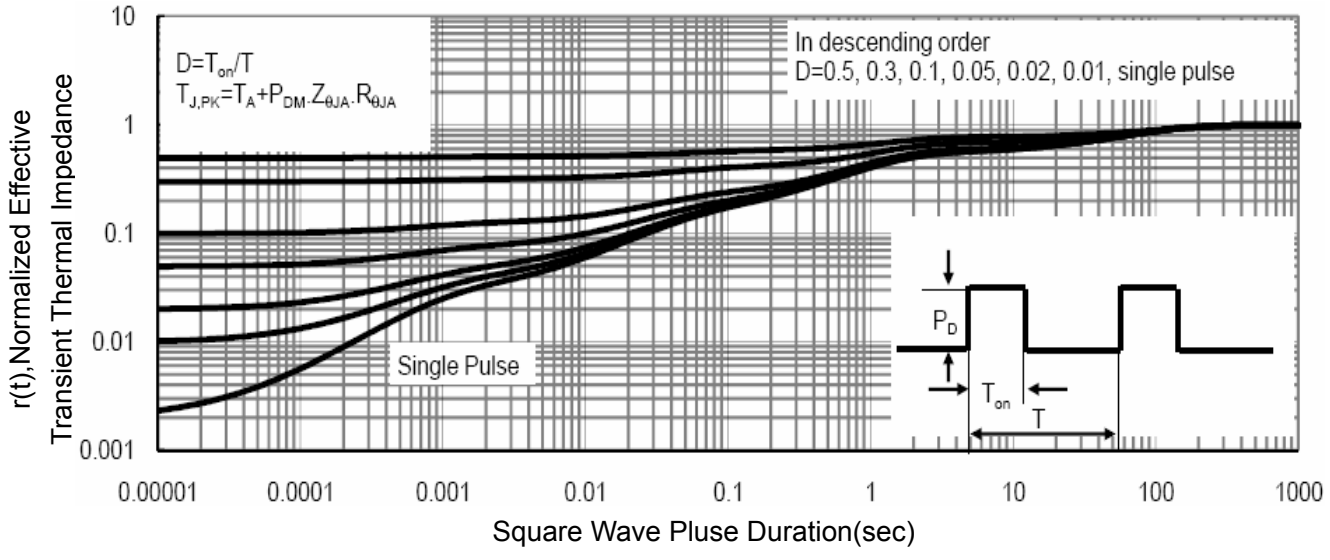
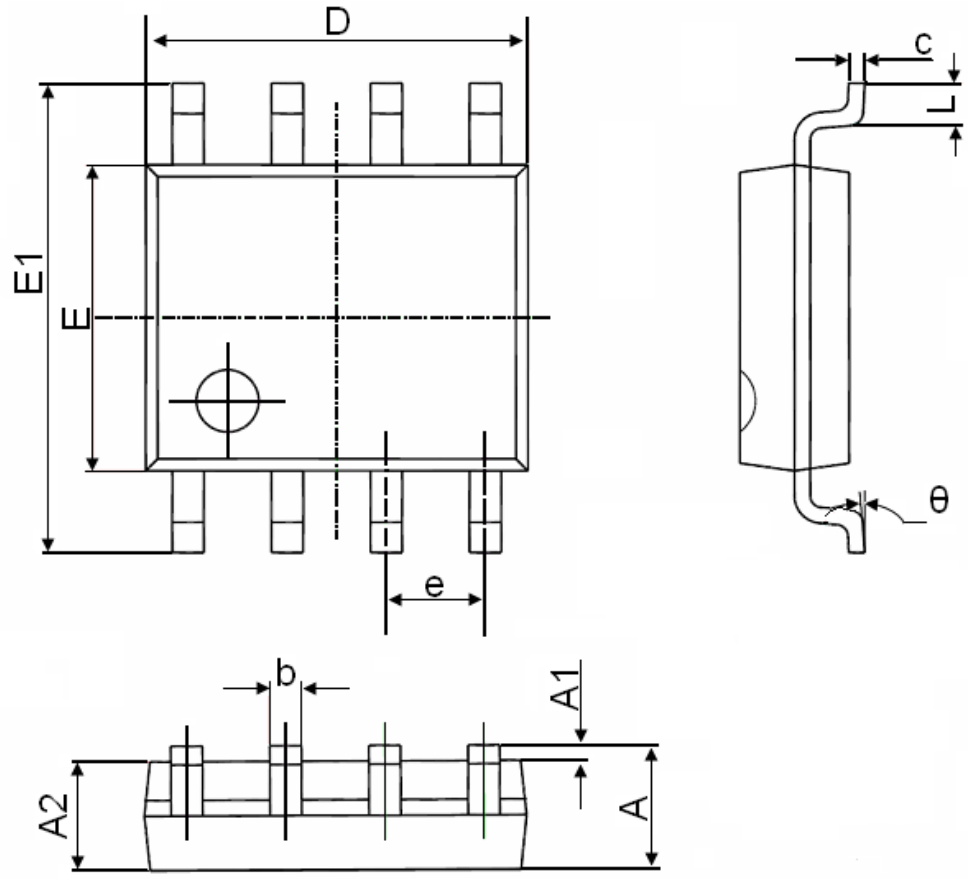


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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