

NCE N-Channel Super Trench Power MOSFET

Description

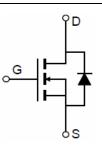
The NCEP60T12T uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{\text{DS(ON)}}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

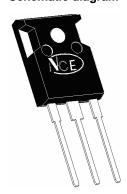
- $V_{DS} = 60V, I_{D} = 120A$
 - $R_{DS(ON)} < 4.0 \text{m}\Omega$ @ $V_{GS} = 10 \text{V}$ (Typ:3.6m Ω)
- Excellent gate charge x R_{DS(on)} product
- Very low on-resistance R_{DS(on)}
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic diagram



TO-247 top view

100% UIS TESTED! 100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity	
NCEP60T12T	NCEP60T12T	TO-247-3L	-	-	-	

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Gate-Source Voltage Drain Current-Continuous (Silicon Limited) Drain Current-Continuous(T _C =100°C) Pulsed Drain Current Maximum Power Dissipation Derating factor Single pulse avalanche energy (Note 5)	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	±20	V	
Drain Current-Continuous (Silicon Limited)	I _D	120	Α	
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	100	Α	
Pulsed Drain Current	I _{DM}	480	Α	
Maximum Power Dissipation	P _D	155	W	
Derating factor		1.03	W/℃	
Single pulse avalanche energy (Note 5)	E _{AS}	500	mJ	
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 175	$^{\circ}$	

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	R _{eJC}	0.97	°C/W
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Electrical Characteristics (T_C=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	,		1	Į.		
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} =60V, V_{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	V_{GS} =±20 V , V_{DS} =0 V	-	-	±100	nA
On Characteristics (Note 3)	<u> </u>			•		•
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =60A	-	3.6	4.0	mΩ
Forward Transconductance	g FS	V _{DS} =10V,I _D =60A	40	-	-	S
Dynamic Characteristics (Note4)	<u> </u>			•		•
Input Capacitance	C _{lss}	\/ 00\/\/ 0\/	-	3400	-	PF
Output Capacitance	C _{oss}	V_{DS} =30V, V_{GS} =0V,	-	650	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz	-	20	-	PF
Switching Characteristics (Note 4)	<u> </u>			•		•
Turn-on Delay Time	t _{d(on)}		-	11	-	nS
Turn-on Rise Time	t _r	V_{DD} =30 V , I_{D} =60 A	-	5	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10 V , R_{G} =4.7 Ω	-	56	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Qg	V 20VI 00A	-	51		nC
Gate-Source Charge	Q _{gs}	$V_{DS}=30V,I_{D}=60A,$	-	12		nC
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	7.3		nC
Drain-Source Diode Characteristics	,		1	Į.		
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =120A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	120	Α
Reverse Recovery Time	t _{rr}	$T_J = 25^{\circ}C$, $I_F = I_S$	-	47		nS
Reverse Recovery Charge	Qrr	$di/dt = 100A/\mu s^{(Note3)}$	-	59		nC

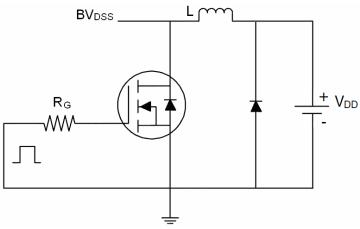
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- 5. EAS condition : Tj=25 $^{\circ}\text{C}$,V_DD=30V,V_G=10V,L=0.5mH,Rg=25 Ω

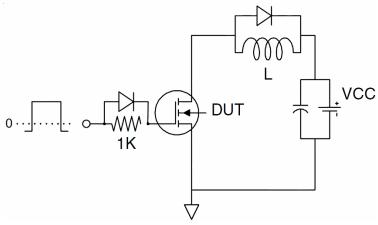


Test Circuit

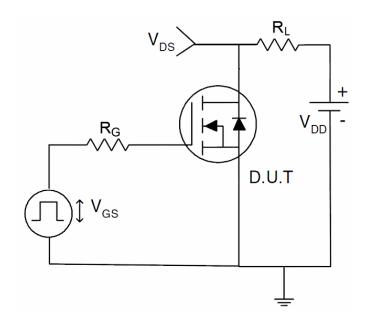
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit







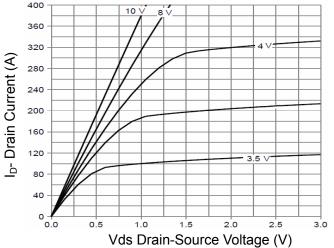


Figure 1 Output Characteristics

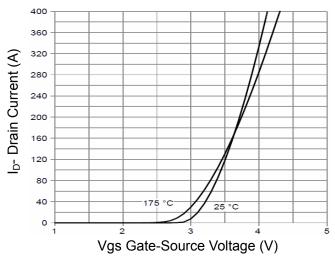


Figure 2 Transfer Characteristics

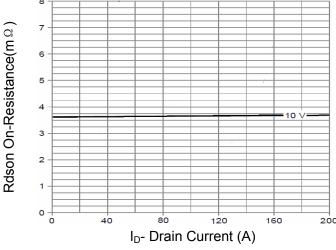


Figure 3 Rdson- Drain Current

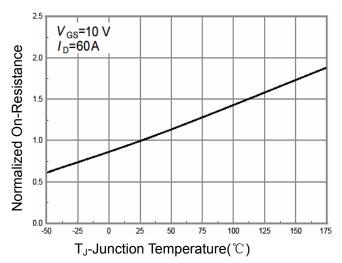


Figure 4 Rdson-JunctionTemperature

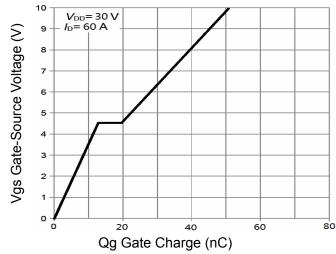


Figure 5 Gate Charge

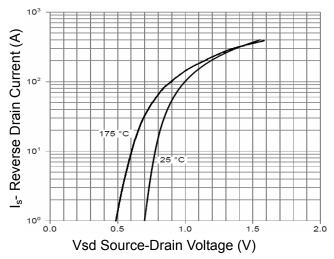
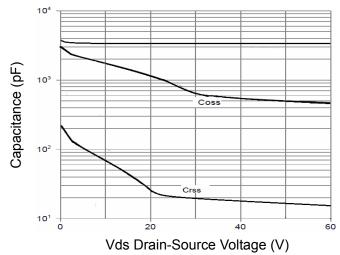


Figure 6 Source- Drain Diode Forward





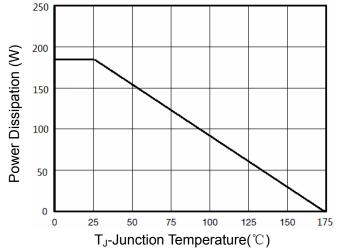
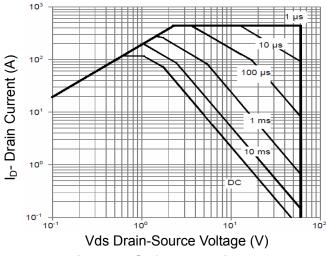


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating



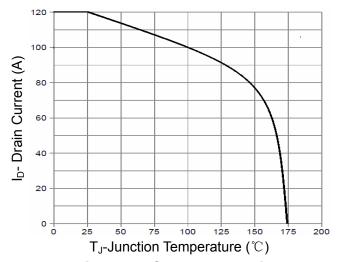


Figure 8 Safe Operation Area

Figure 10 Current De-rating

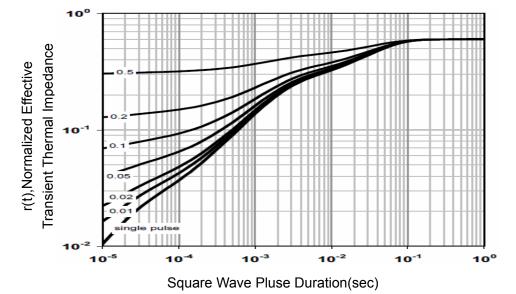
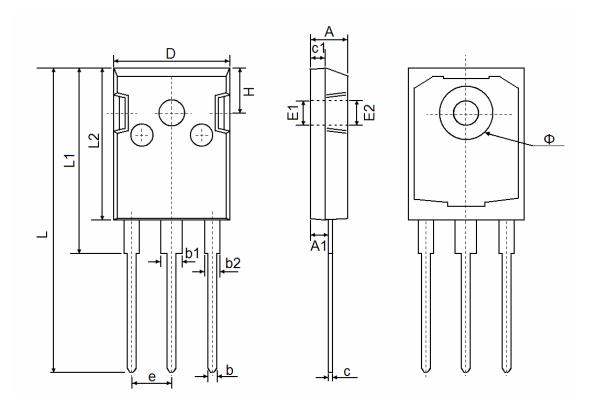


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-247 Package Information



O-mak at	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
Α	4.850	5.150	0.191	0.200	
A1	2.200	2.600	0.087	0.102	
b	1.000	1.400	0.039	0.055	
b1	2.800	3.200	0.110	0.126	
b2	1.800	2.200	0.071	0.087	
С	0.500	0.700	0.020	0.028	
c1	1.900	2.100	0.075	0.083	
D	15.450	15.750	0.608	0.620	
E1	3.500	REF	0.138	REF	
E2	3.600	3.600 REF		REF	
L	40.900	41.300	1.610	1.626	
L1	24.800	25.100	0.976	0.988	
L2	20.300	20.600	0.799	0.811	
Ф	7.100	7.300	0.280	0.287	
е	5.450) TYP	0.215 TYP		
Н	5.980) REF	0.235 REF		



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