

NCE N-Channel Super Trench Power MOSFET

Description

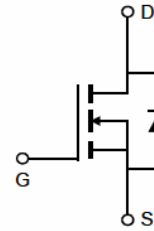
The NCEP60T20LL uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

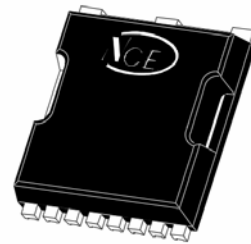
- $V_{DS} = 60V, I_D = 300A$
 $R_{DS(ON)} = 1.2m\Omega$ (typical) @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic diagram



TOLL top view

100% UIS TESTED!
100% ΔVds TESTED!

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP60T20LL	NCEP60T20LL	TOLL	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	300	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	225	A
Pulsed Drain Current	I_{DM}	1200	A
Maximum Power Dissipation	P_D	350	W
Derating factor		2.33	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	2000	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.43	°C/W
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Electrical Characteristics ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	60		-	V

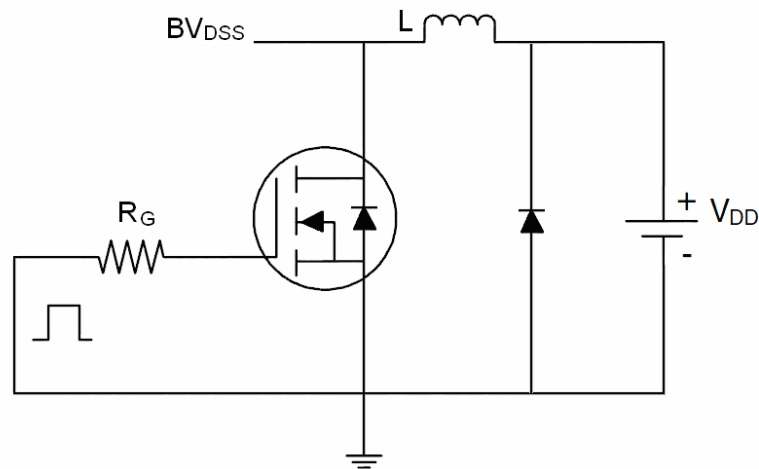
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.2	2.7	3.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=150A$	-	1.2	1.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=150A$	-	60	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	8600	-	PF
Output Capacitance	C_{oss}		-	1800	-	PF
Reverse Transfer Capacitance	C_{rss}		-	54	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=150A$ $V_{GS}=10V, R_G=4.7\Omega$	-	19	-	nS
Turn-on Rise Time	t_r		-	31	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	58	-	nS
Turn-Off Fall Time	t_f		-	23	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=150A,$ $V_{GS}=10V$	-	129		nC
Gate-Source Charge	Q_{gs}		-	40.6		nC
Gate-Drain Charge	Q_{gd}		-	23.9		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=300A$	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	300	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, I_F = 150A$ $di/dt = 100A/\mu s$ (Note3)	-	67		nS
Reverse Recovery Charge	Q_{rr}		-	112		nC

Notes:

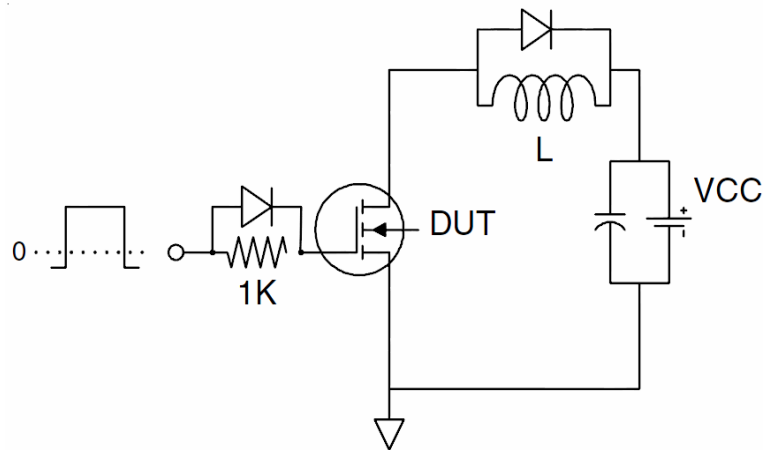
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ C, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

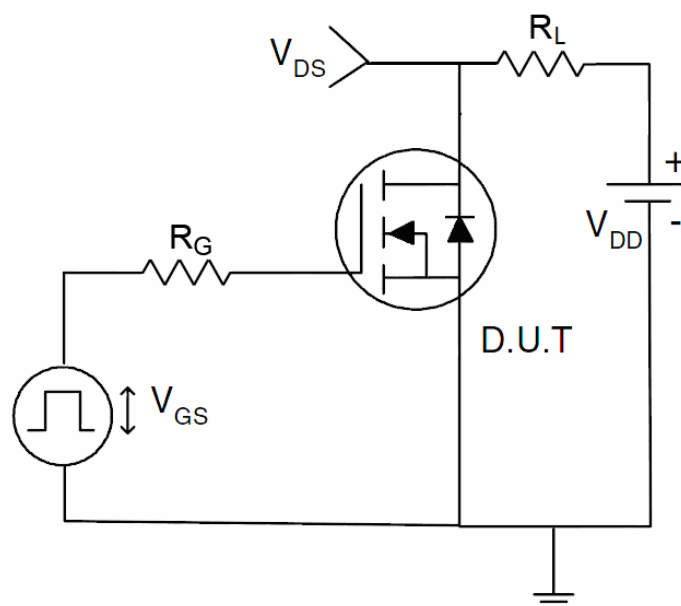
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

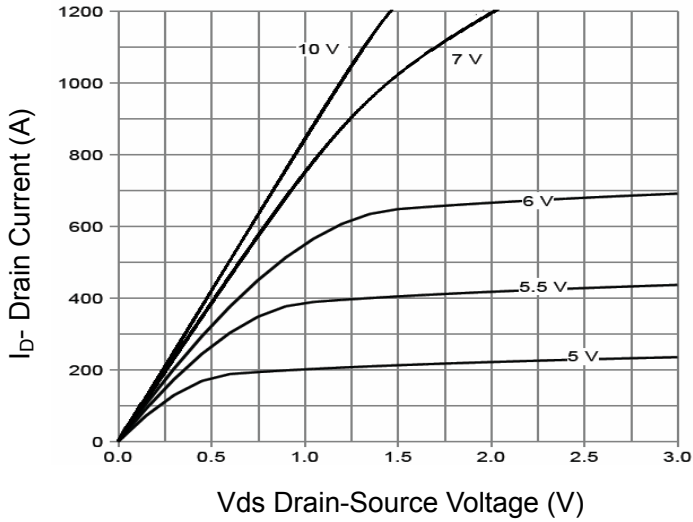


Figure 1 Output Characteristics

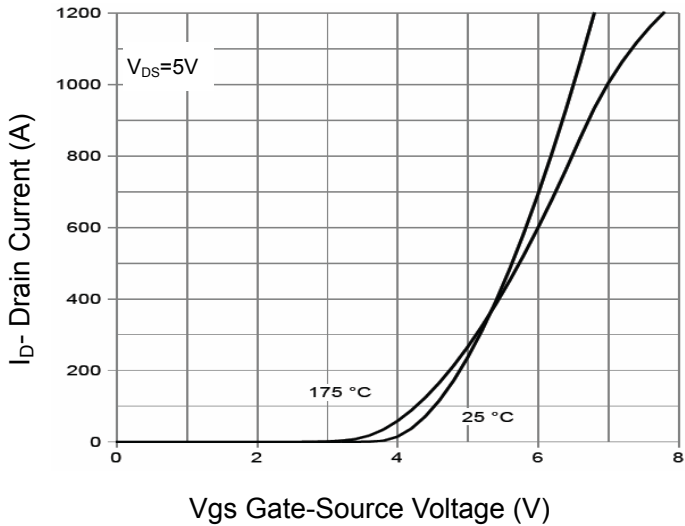


Figure 2 Transfer Characteristics

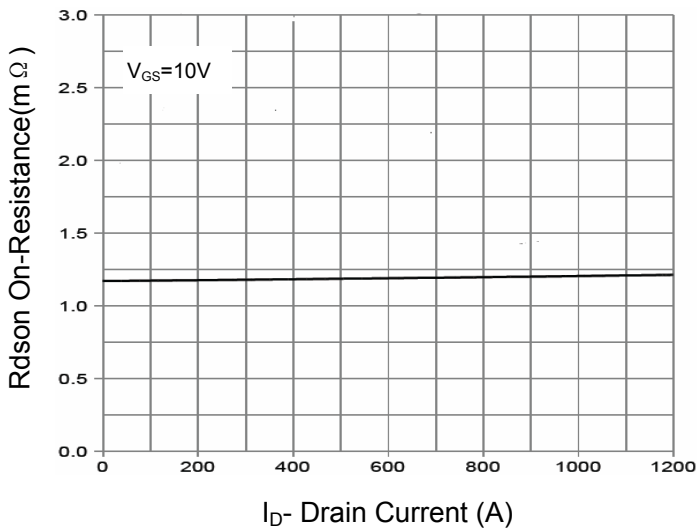


Figure 3 Rdson- Drain Current

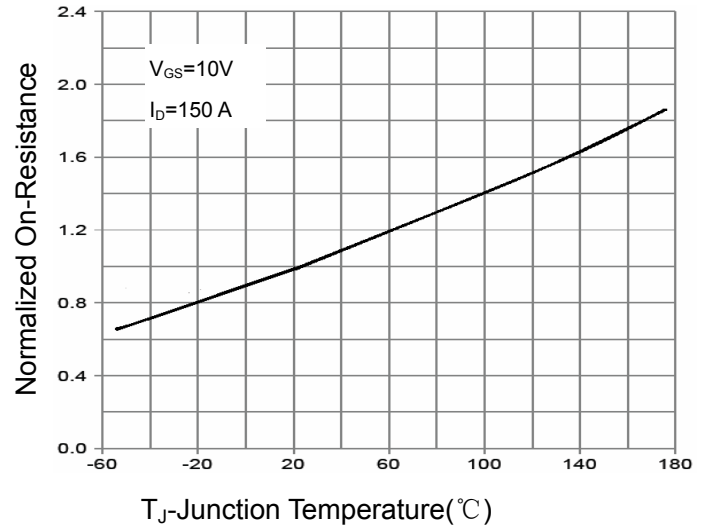


Figure 4 Rdson-Junction Temperature

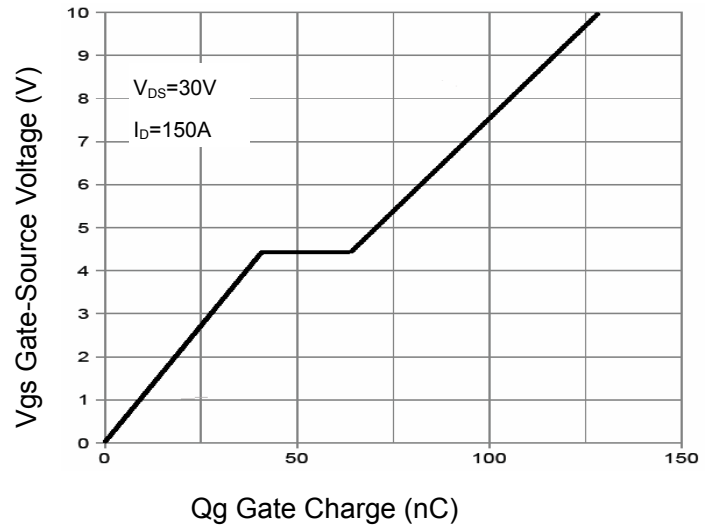


Figure 5 Gate Charge

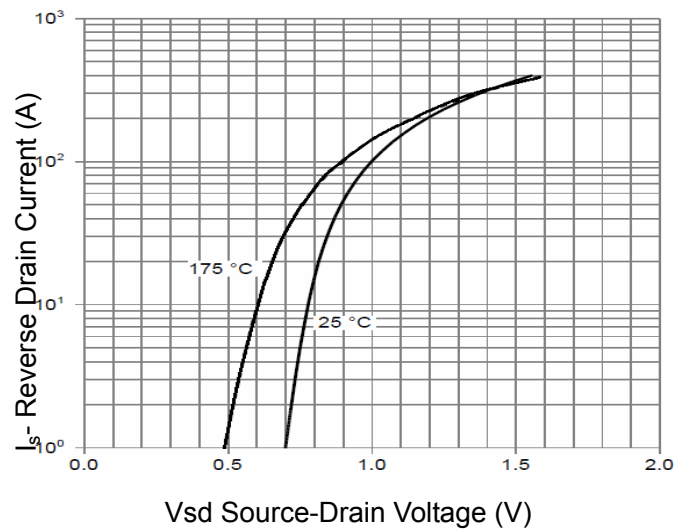
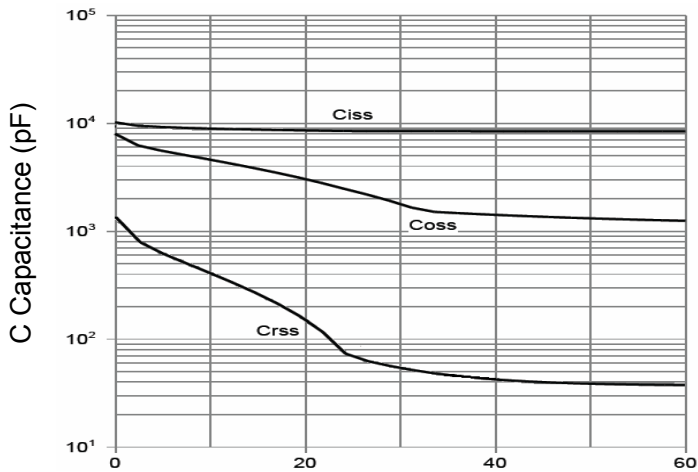
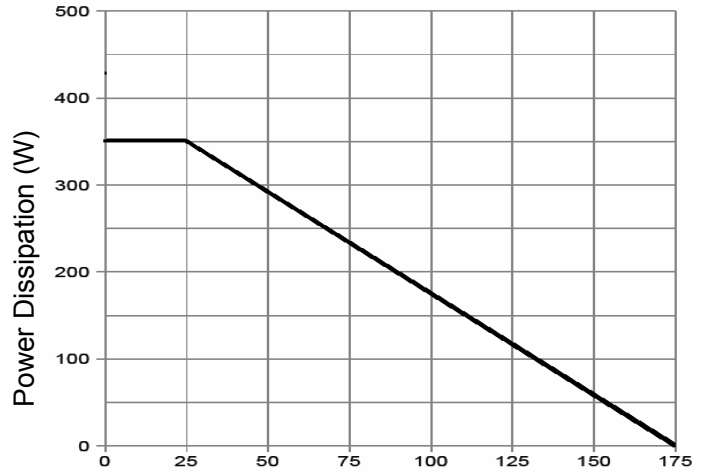


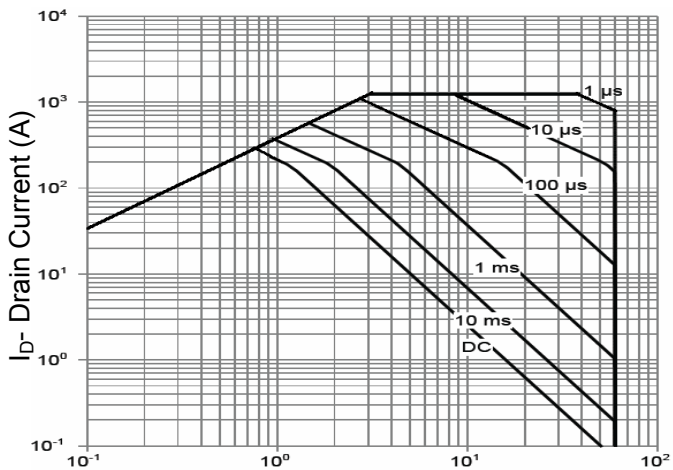
Figure 6 Source- Drain Diode Forward



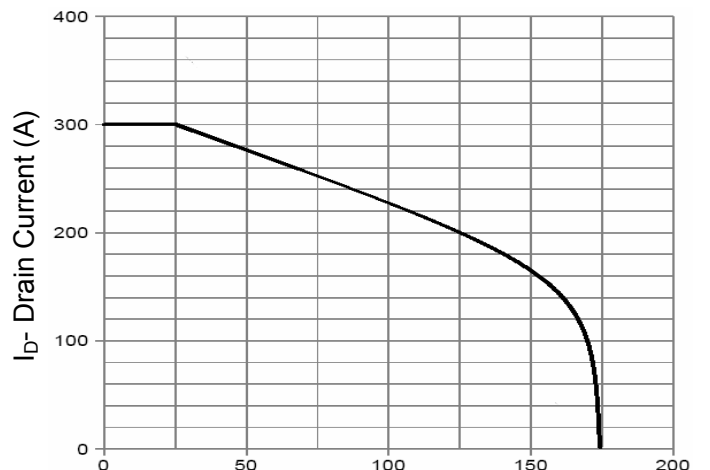
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature (°C)
Figure 10 Current De-rating

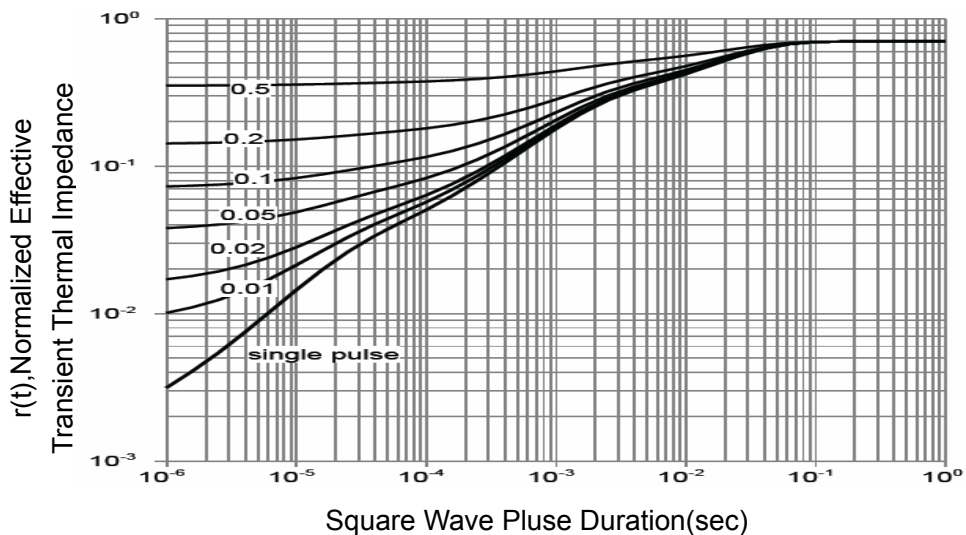
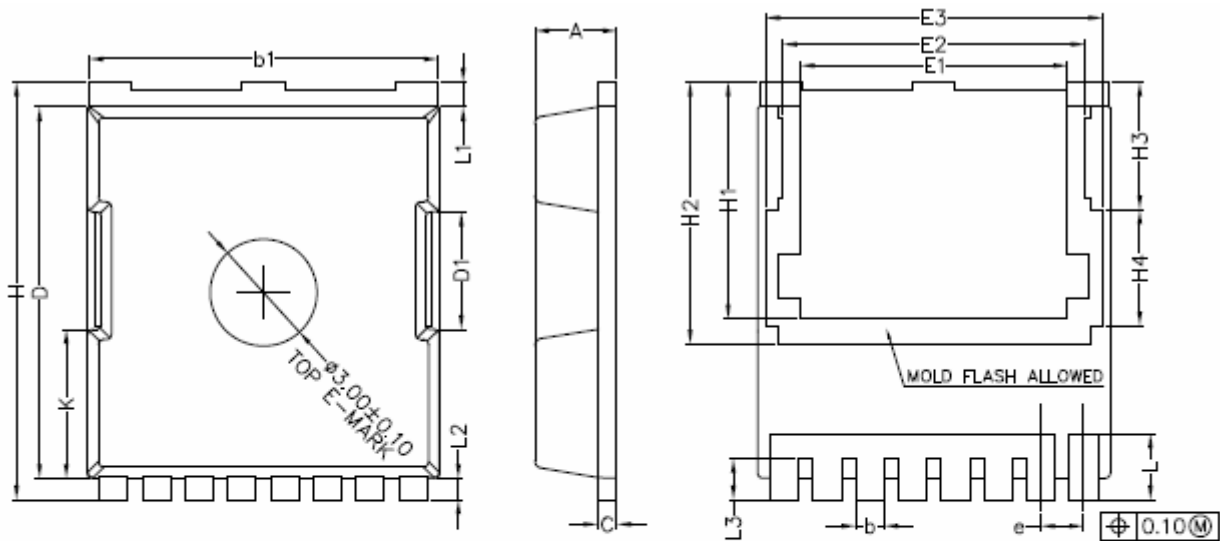


Figure 11 Normalized Maximum Transient Thermal Impedance

TOLL Package Information



TOP VIEW

SIDE VIEW

BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS (UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b_1	9.70	9.80	9.90
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	7.35	7.50	7.65
E2	8.35	8.50	8.65
E3	9.31	9.46	9.61
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	6.55	6.65	6.75
H2	7.20	7.35	7.50
H3	3.44	3.59	3.74
H4	3.11	3.26	3.41
K	4.03	4.18	4.33
L	1.60	1.85	2.10
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30

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