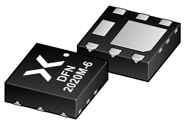

PSMN071-100NSE

N-channel 100 V, 81 mOhm standard level 'ASFET with enhanced SOA' in DFN2020 package, designed specifically for Power-over-ethernet (PoE) applications

3 May 2022 — Objective data sheet

1. General description

New standards and proprietary approaches are enabling Power-over-Ethernet (PoE) systems capable of delivering up to 90 W to each powered device (PD). Such solutions place increased demands on the power sourcing equipment (PSE) in terms of "soft-start", thermal management and power density requirements. PSMN071-100NSE is designed specifically for low power PoE applications.

2. Features and benefits

- Enhanced safe operating area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- 2 mm x 2 mm space-saving DFN2020 package, 60% smaller footprint than LFPAK33
- Very low I_{DSS} leakage

3. Applications

- PoE applications (<60 W)
- IEEE802.3at and proprietary PoE solutions
- Fault tolerant load switch - inrush management and eFuse applications
- Battery management applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	13	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	28	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	58	81	mΩ

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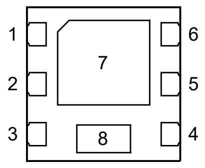
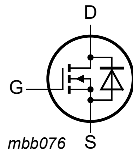
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	Transparent top view **DFN2020M-6 (SOT1220-2)**	
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN071-100NSE	DFN2020M-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN071-100NSE	ZU

8. Limiting values

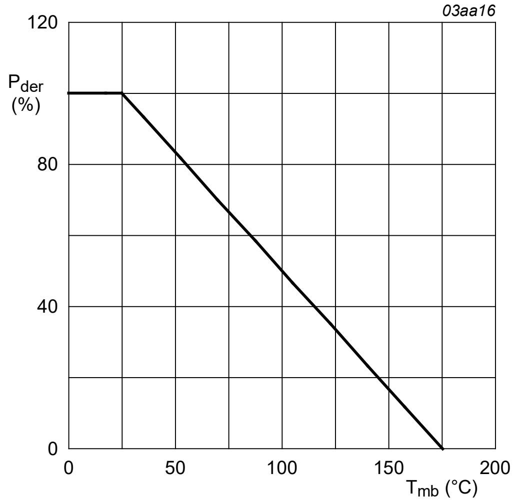
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	28	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	13	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	9	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 2		-	51	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	13	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	51	A

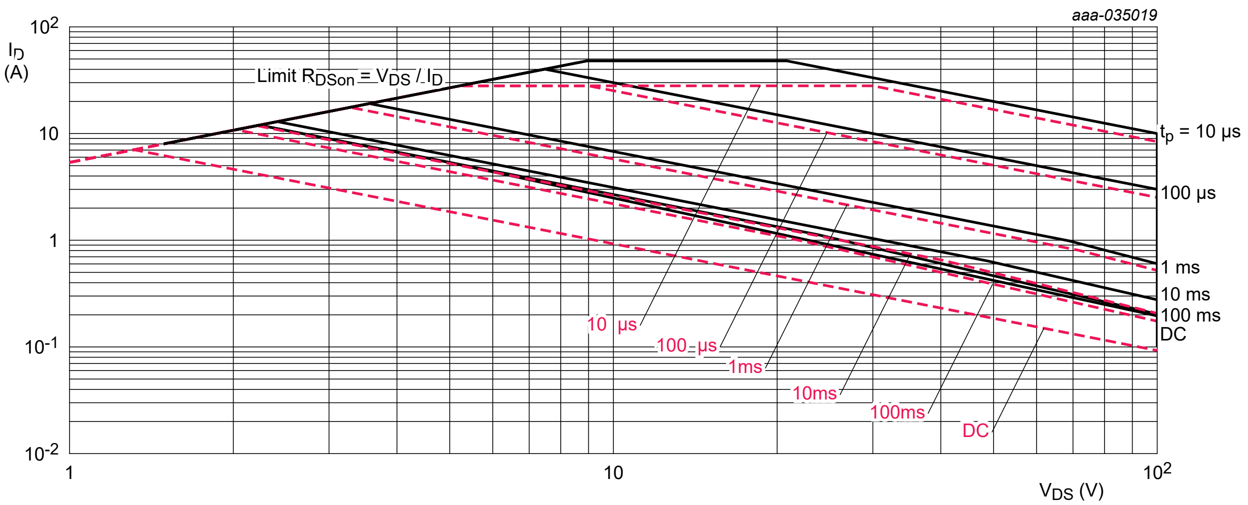
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 6.6 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	10.8	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[1]	-	6.6	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



T_{mb} = 25 °C (solid black line); T_{mb} = 125 °C (red dashed line); I_{DM} is a single pulse

Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

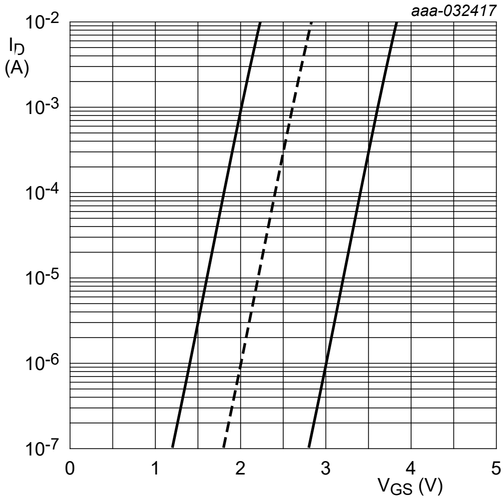
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	5.4	K/W

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 3		2	2.6	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	[tbd]	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	[tbd]	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	1	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{DS} = 20 V; T_j = 25 °C		-	2	100	nA
		V_{DS} = -20 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C		-	58	81	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 100 °C		-	90	129	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 175 °C		-	128	184	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	0.8	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	4.7	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	2.5	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	1.4	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	0.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.5	-	nC
Q_{GD}	gate-drain charge			[tbd]	0.9	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; T_j = 25 °C		-	4.5	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	330	[tbd]	pF
C_{oss}	output capacitance			[tbd]	72	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	2.3	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	1.2	-	ns
t_r	rise time			-	1	-	ns
$t_{d(off)}$	turn-off delay time			-	2.9	-	ns
t_f	fall time			-	1.4	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	-	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; Fig. 4		-	30	-	ns
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; T_j = 25 °C; Fig. 4		-	21	-	nC



T_j = 25 °C; V_{DS} = 5 V

Fig. 3. Sub-threshold drain current as a function of gate-source voltage

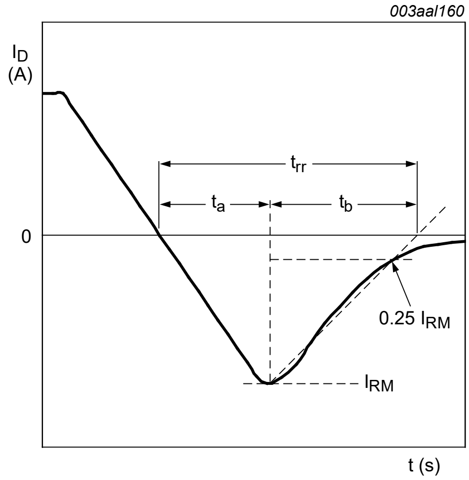
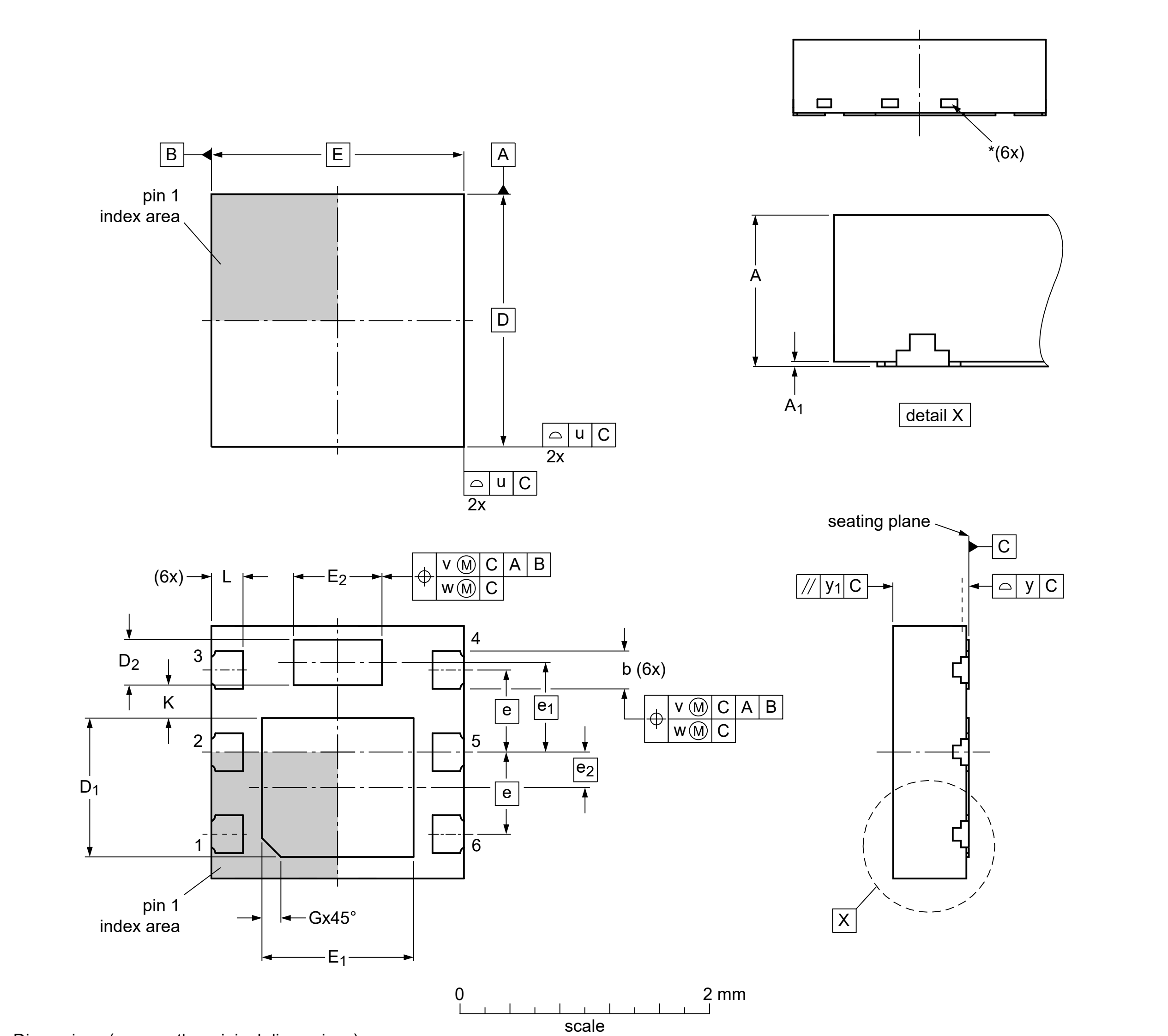


Fig. 4. Reverse recovery timing definition

11. Package outline

DFN2020M-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm **SOT1220-2**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	D	D_1	D_2	E	E_1	E_2	e	e_1	e_2	G	K	L	u	v	w	y	y_1
mm	min	0.55	0	0.25		1.0	0.31		1.1	0.6					0.2	0.20					
	nom	0.60	0.02	0.30	2	1.1	0.36	2	1.2	0.7	0.65	0.71	0.28	0.15 (ref)		0.25	0.05	0.1	0.05	0.05	0.05
	max	0.65	0.04	0.35		1.2	0.41		1.3	0.8						0.30					

Note
1. Dimension A is including plating thickness.
2. * Visible depend upon used manufacturing technology.

sot1220-2_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT1220-2		- - -				~~20-03-31~~ 20-04-01

Fig. 5. Package outline DFN2020M-6 (SOT1220-2)

12. Soldering

Footprint information for reflow soldering of DFN2020M-6 package **SOT1220-2**

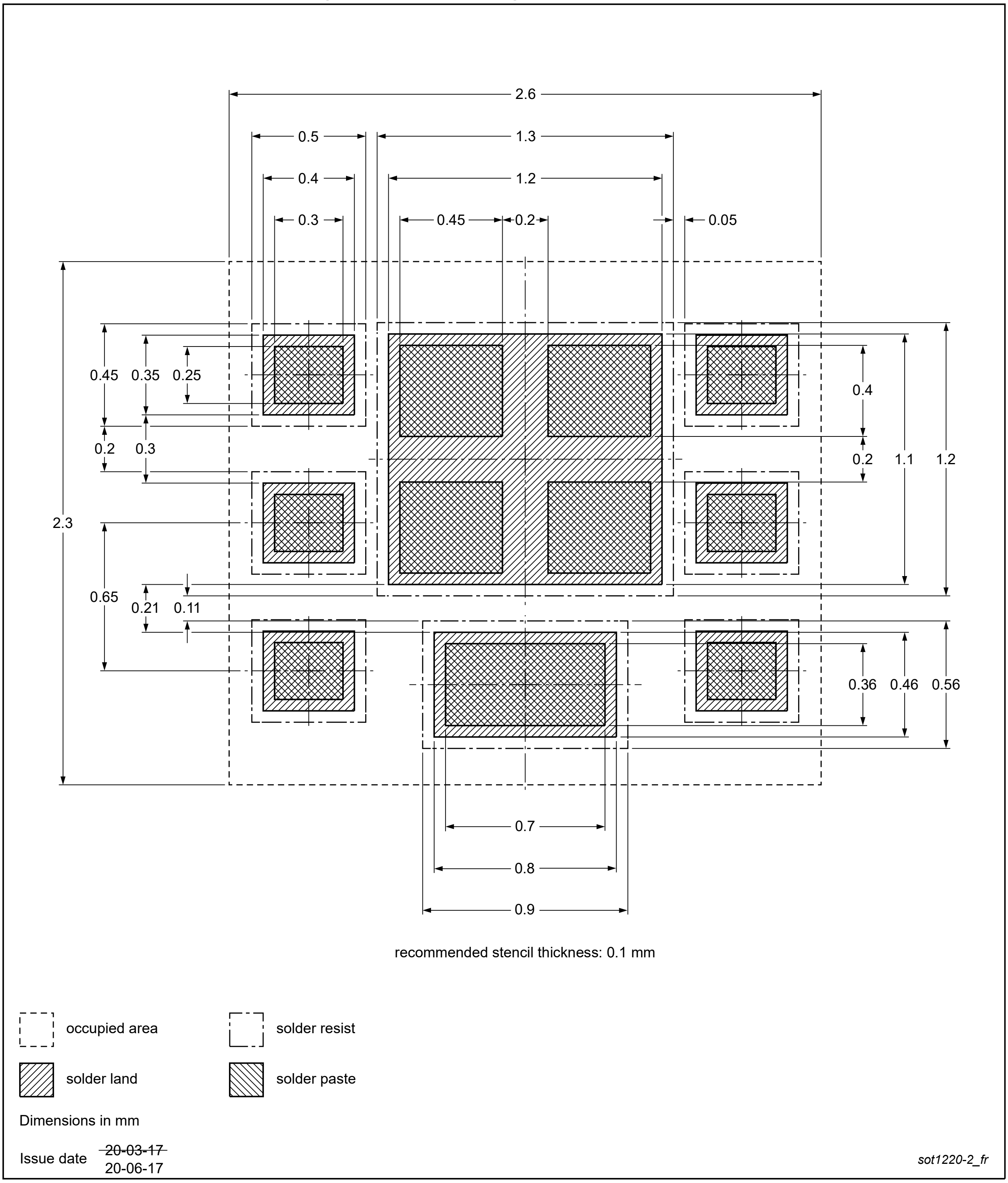


Fig. 6. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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