



PMN48XP

20 V, 4.1 A P-channel Trench MOSFET

Rev. 1 — 21 April 2011

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Low R_{DSon}
- Very fast switching
- Trench MOSFET technology

1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-4.1	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -2.4\text{ A}; T_j = 25\text{ °C}$	-	48	55	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	<p>SOT457 (TSOP6)</p>	<p>017aaa094</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

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3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMN48XP	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PMN48XP	ZV

5. Limiting values

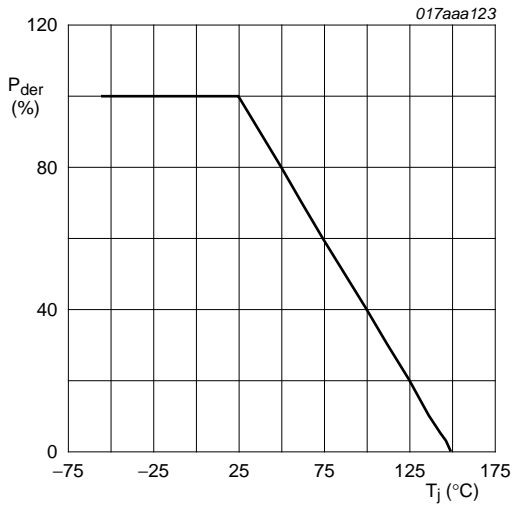
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-20	V	
V_{GS}	gate-source voltage		-12	12	V	
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-4.1	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-2.5	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-20	A	
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	530	mW
			[1]	-	1285	mW
		$T_{sp} = 25\text{ °C}$		-	6250	mW
T_j	junction temperature		-55	150	°C	
T_{amb}	ambient temperature		-55	150	°C	
T_{stg}	storage temperature		-65	150	°C	
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1.4	A

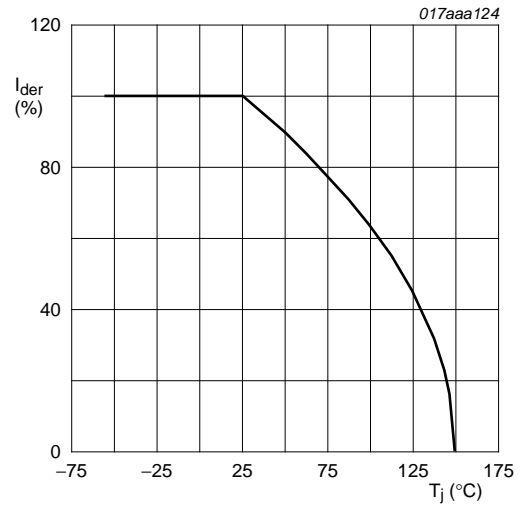
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



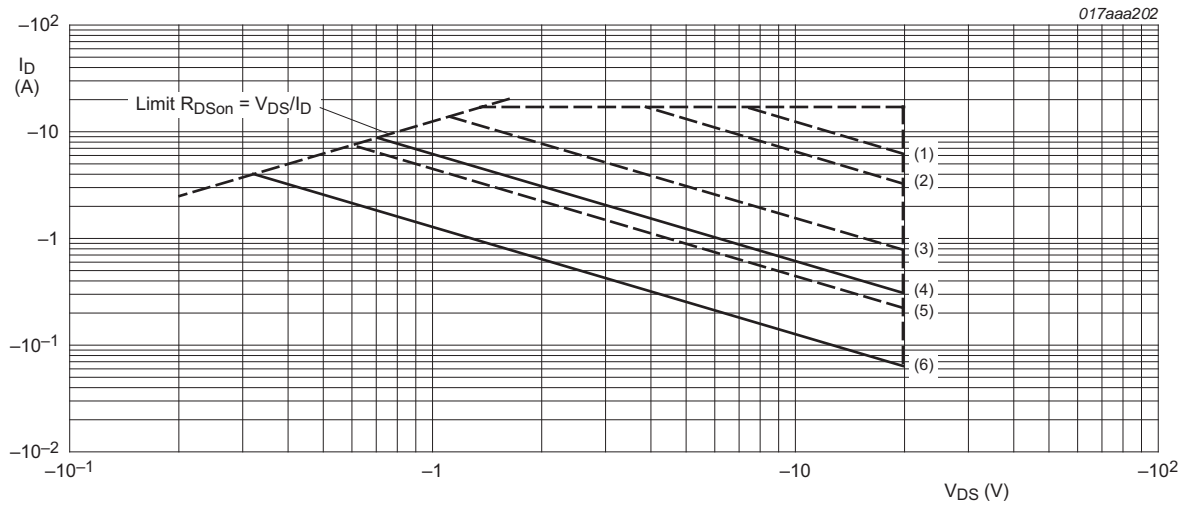
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

Fig 1. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

Fig 2. Normalized continuous drain current as a function of junction temperature



I_{DM} = single pulse

(1) $t_p = 100 \mu s$

(2) $t_p = 1 ms$

(3) $t_p = 10 ms$

(4) DC; $T_{sp} = 25 \text{ }^\circ\text{C}$

(5) $t_p = 100 ms$

(6) DC; $T_{amb} = 25 \text{ }^\circ\text{C}$; drain mounting pad 6 cm^2

Fig 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	204	235	K/W
		[2]	-	84	97	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	17	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

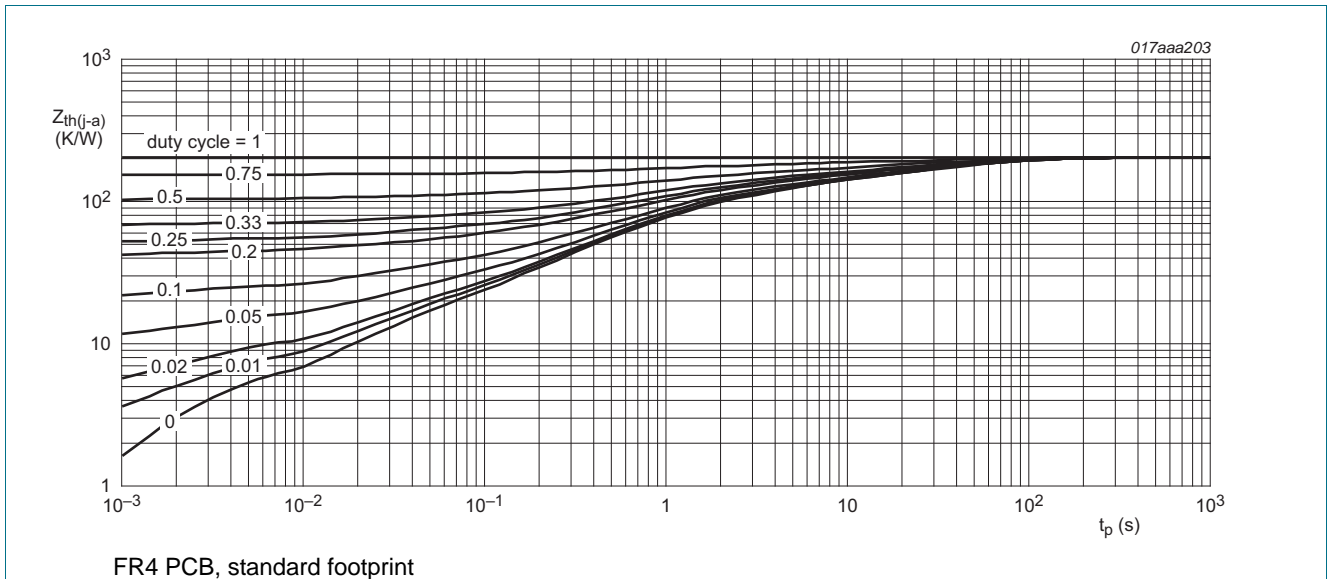


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

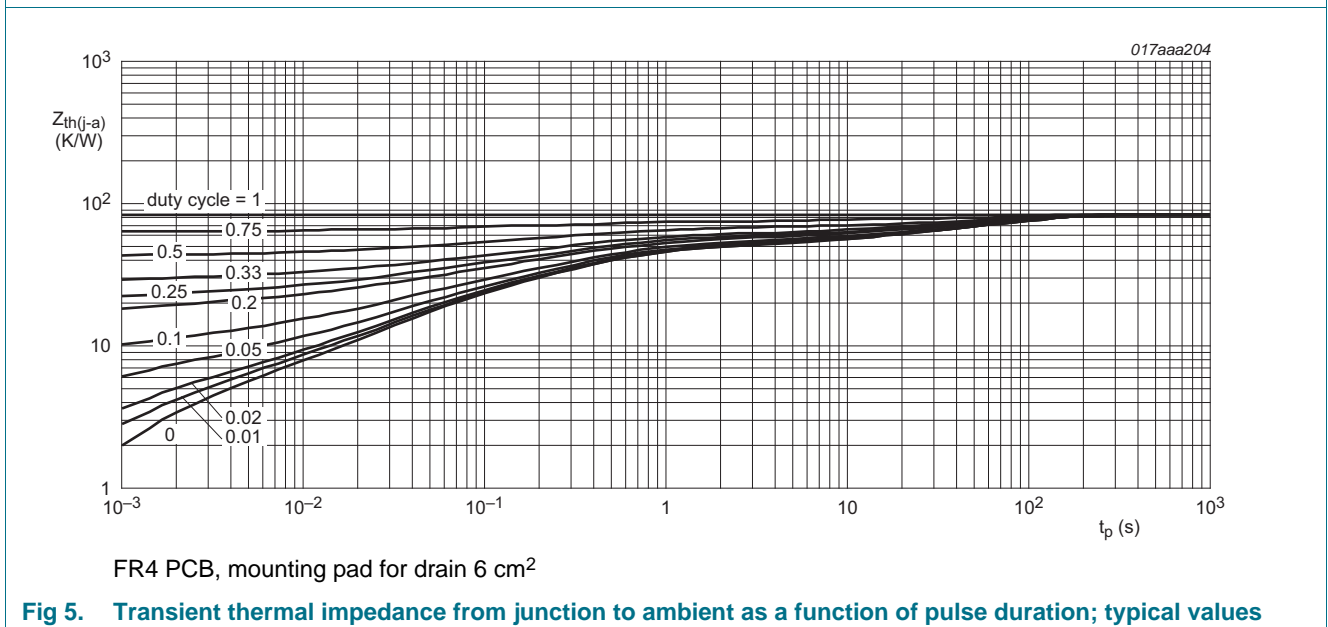
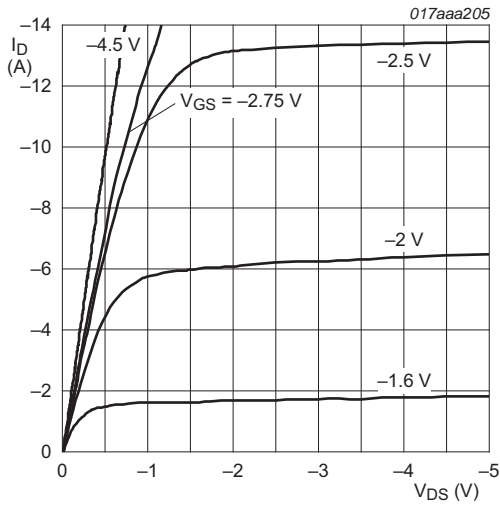


Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

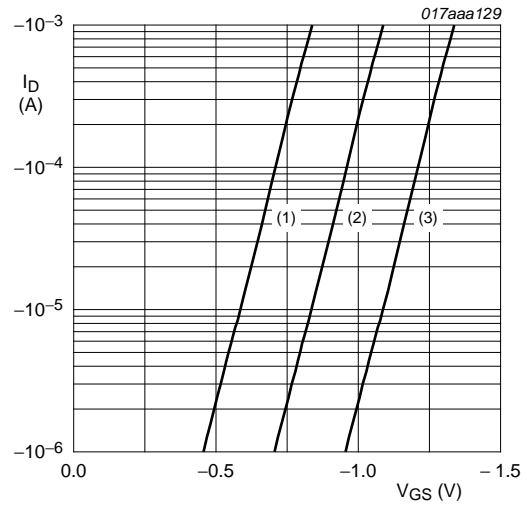
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	-0.75	-1	-1.25	V
I_{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	μA
		$V_{DS} = -20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = -12 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$; $I_D = -2.4 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	48	55	m Ω
		$V_{GS} = -4.5 \text{ V}$; $I_D = -2.4 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	70	80	m Ω
		$V_{GS} = -2.5 \text{ V}$; $I_D = -2 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	72	82	m Ω
g_{fs}	forward transconductance	$V_{DS} = -5 \text{ V}$; $I_D = -2.4 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	10	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = -1 \text{ A}$; $V_{DS} = -10 \text{ V}$; $V_{GS} = -4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	8.7	13	nC
Q_{GS}	gate-source charge		-	1.8	-	nC
Q_{GD}	gate-drain charge		-	1.7	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}$; $V_{DS} = -10 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$	-	1000	-	pF
C_{oss}	output capacitance		-	130	-	pF
C_{rss}	reverse transfer capacitance		-	90	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$; $V_{GS} = -5 \text{ V}$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$; $I_D = -1 \text{ A}$	-	15	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	51	-	ns
t_f	fall time		-	22	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -2.4 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.75	-1	V



$T_j = 25\text{ }^\circ\text{C}$

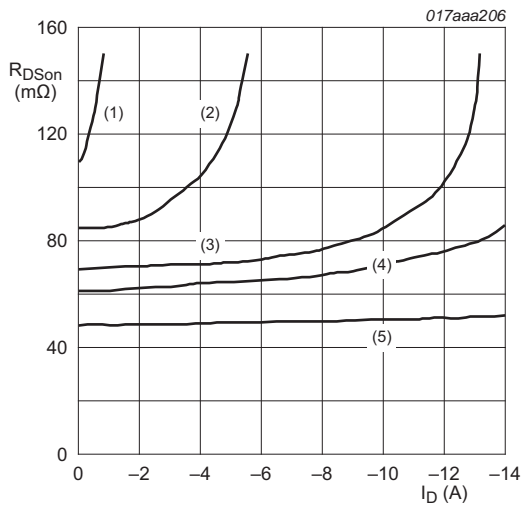
Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -3\text{ V}$

- (1) minimum values
- (2) typical values
- (3) maximum values

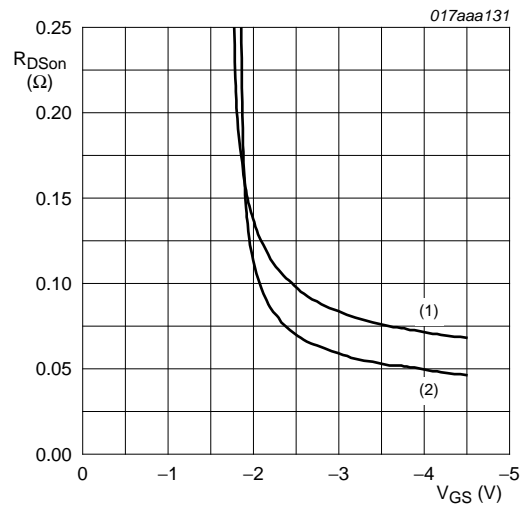
Fig 7. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^\circ\text{C}$

- (1) $V_{GS} = -1.6\text{ V}$
- (2) $V_{GS} = -2.0\text{ V}$
- (3) $V_{GS} = -2.5\text{ V}$
- (4) $V_{GS} = -2.75\text{ V}$
- (5) $V_{GS} = -4.5\text{ V}$

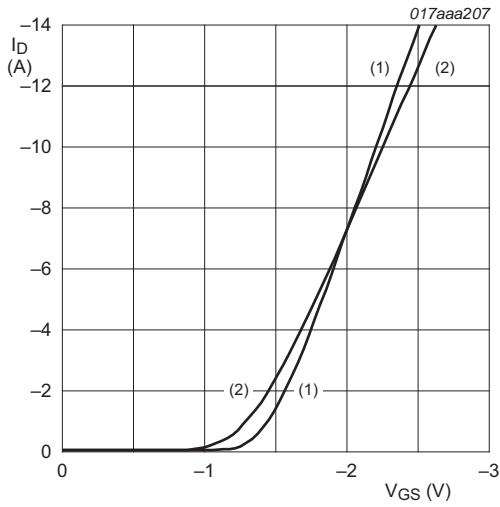
Fig 8. Drain-source on-state resistance as a function of drain current; typical values



$I_D = -2.4\text{ A}$

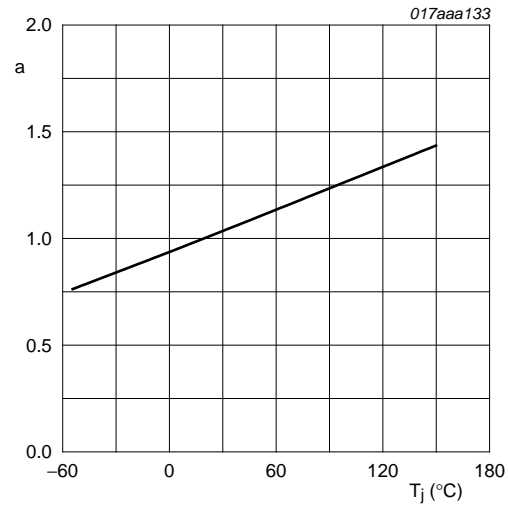
- (1) $T_j = 125\text{ }^\circ\text{C}$
- (2) $T_j = 25\text{ }^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



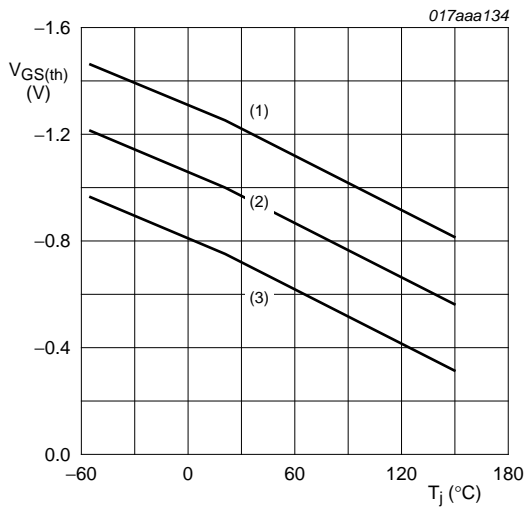
$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ °C}$
 (2) $T_j = 150\text{ °C}$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



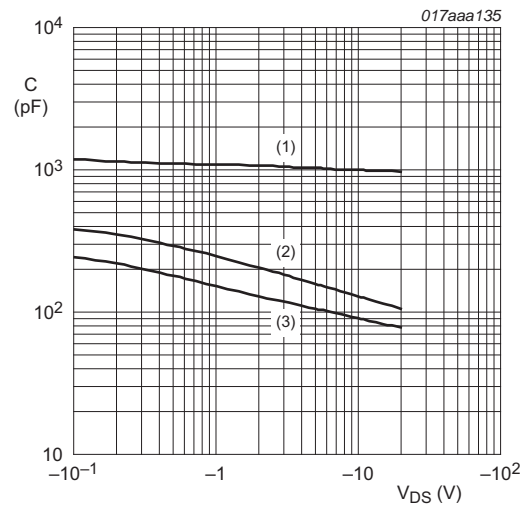
$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^\circ\text{C}}}$$

Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



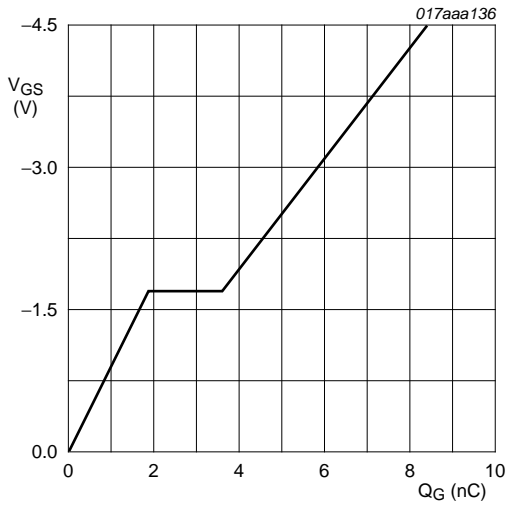
$I_D = -0.25\text{ mA}; V_{DS} = V_{GS}$
 (1) maximum values
 (2) typical values
 (3) minimum values

Fig 12. Gate-source threshold voltage as a function of junction temperature



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$
 (1) C_{iss}
 (2) C_{oss}
 (3) C_{rss}

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -2.4 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig 14. Gate-source voltage as a function of gate charge; typical values

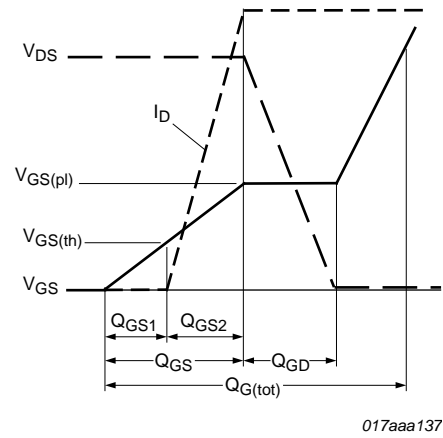
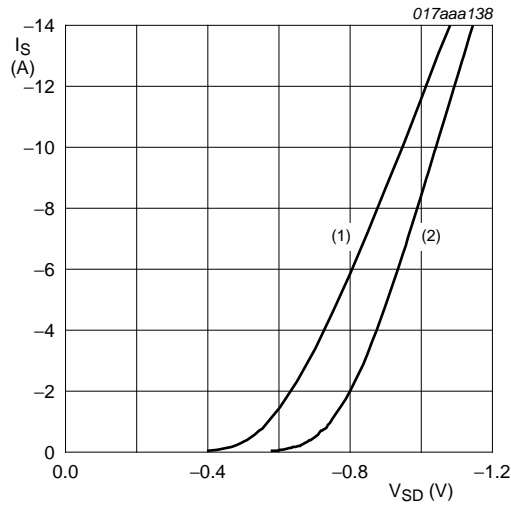


Fig 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$
 (1) $T_j = 150 \text{ }^\circ\text{C}$
 (2) $T_j = 25 \text{ }^\circ\text{C}$

Fig 16. Source current as a function of source-drain voltage; typical values

8. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

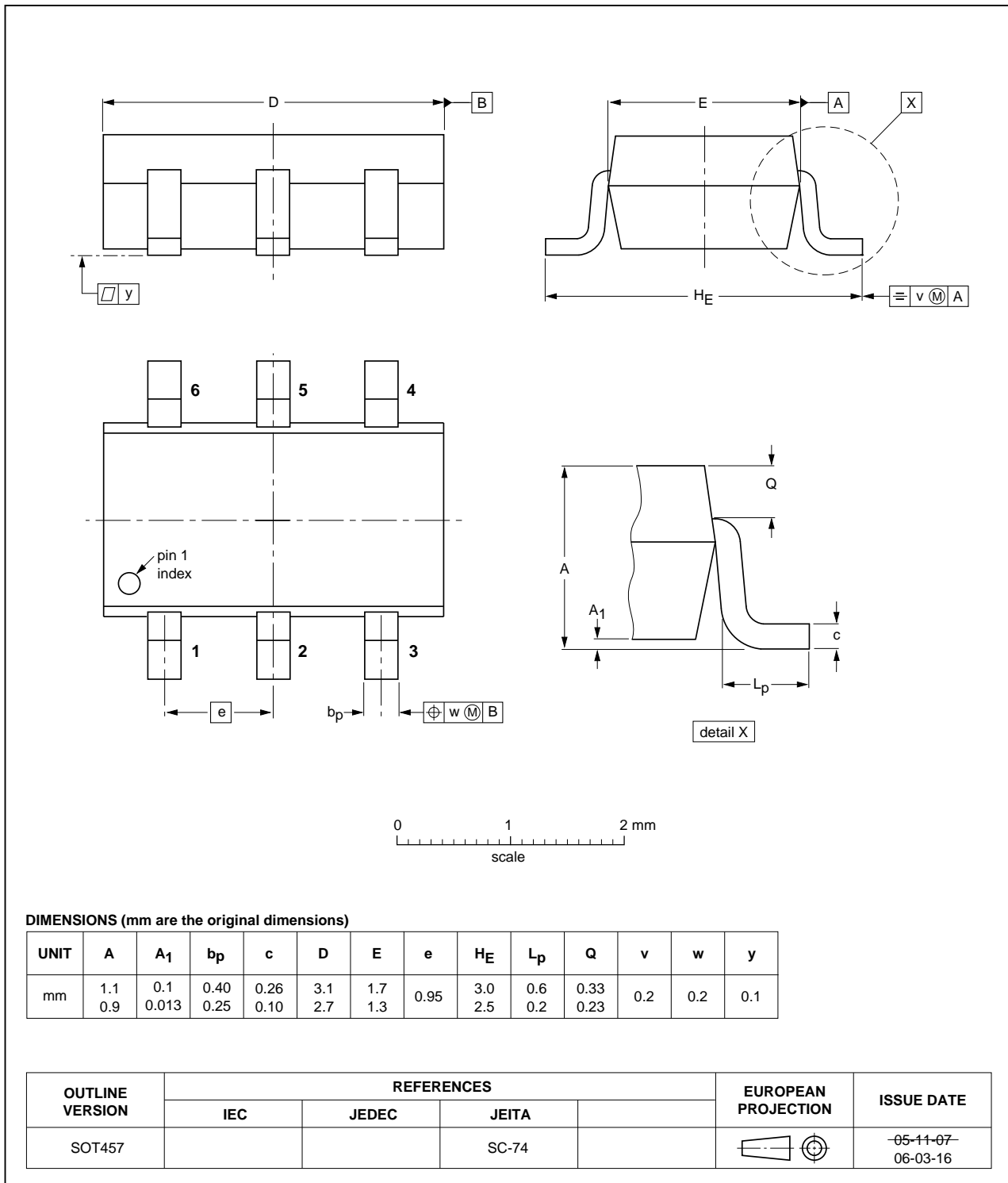
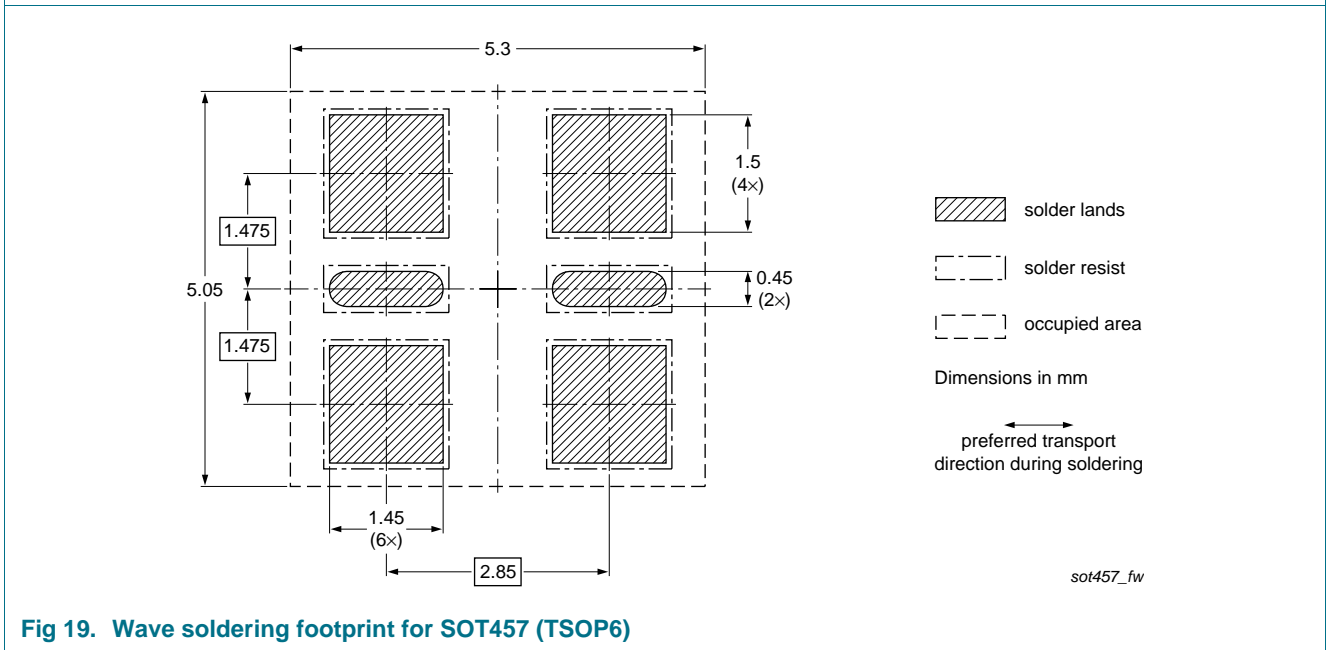
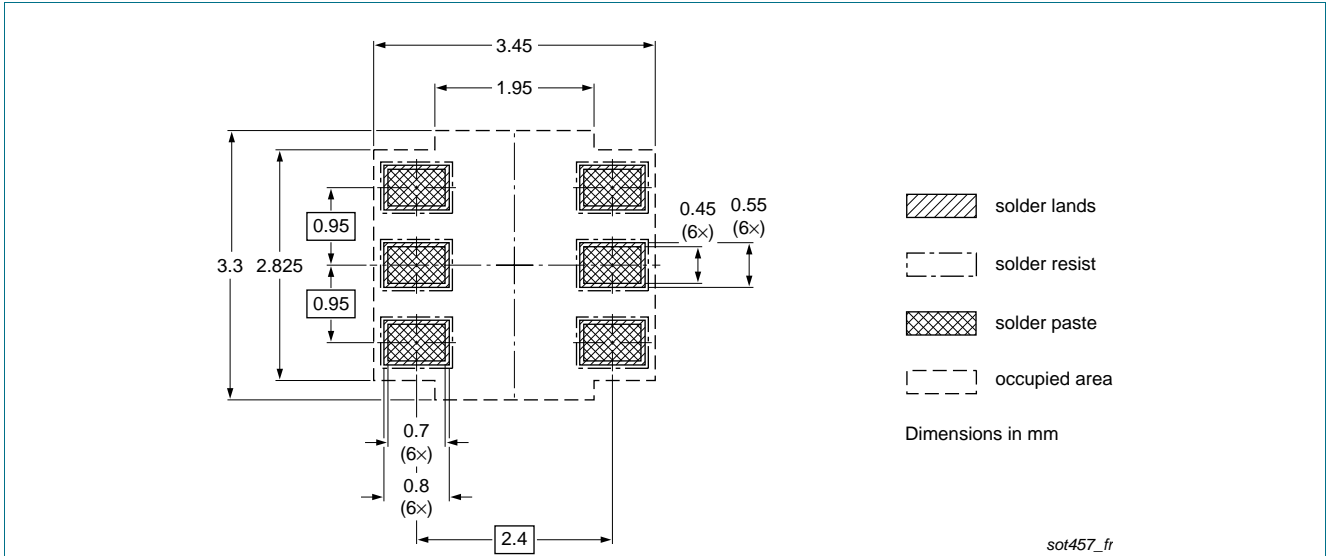


Fig 17. Package outline SOT457 (TSOP6)

9. Soldering



10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN48XP v.1	20110421	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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