PUMD6H-Q

50 V, 100 mA NPN/PNP Resistor-Equipped double Transistor; R1 = 4.7 kΩ, R2 = open

6 May 2021 Product data sheet

1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in a very small SOT363 (TSSOP6) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH7H-Q

PNP/PNP complement: PUMB3H-Q

2. Features and benefits

- 100 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- High-temperature applications up to 175 °C
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital applications
- Cost saving alternative for BC847 / BC857 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1	T_{amb} = 25 °C	[1]	3.3	4.7	6.1	kΩ

[1] See section "Test information" for resistor calculation and test conditions

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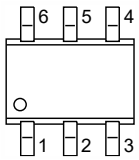
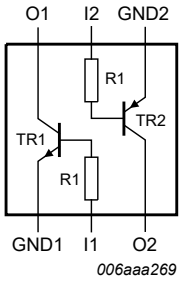
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 TSSOP6 (SOT363)	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD6H-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD6H-Q	7G%

[1] % = placeholder for manufacturing site code

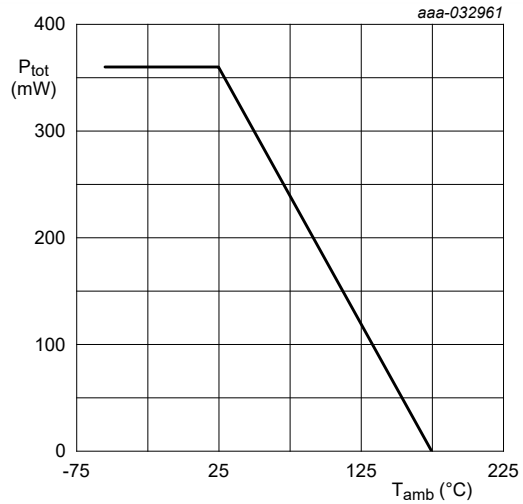
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	7	V
V_I	input voltage			-7	30	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	240	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	360	mW
T_j	junction temperature			-	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

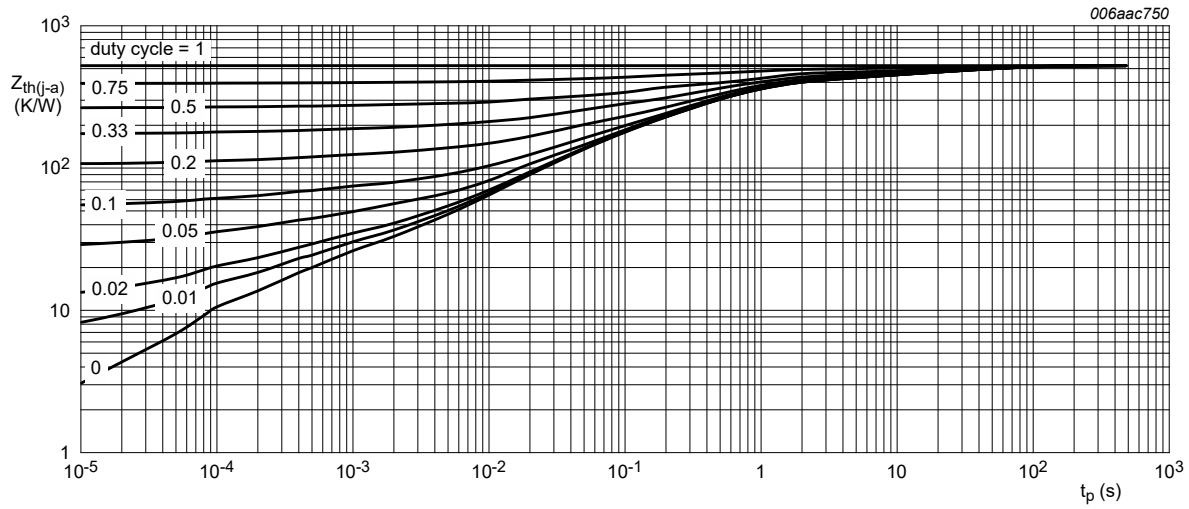
Fig. 1. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	230	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

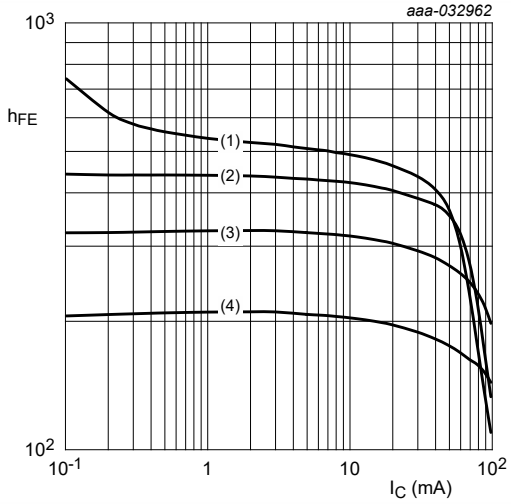
Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

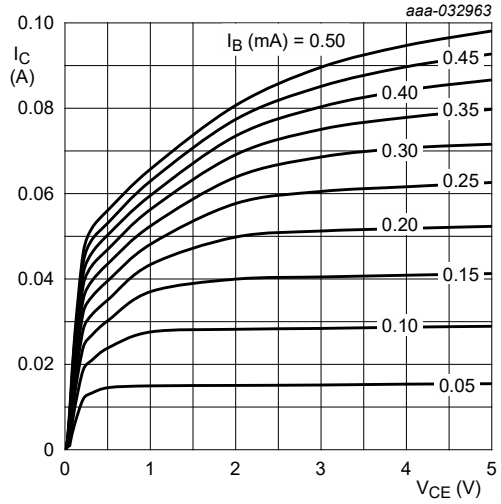
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A; T_{amb} = 25 °C		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A; T_{amb} = 25 °C		50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A; T_{amb} = 25 °C		-	-	100	nA
		V_{CE} = 30 V; I_B = 0 A; T_{amb} = 150 °C		-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 7 V; I_C = 0 mA; T_{amb} = 25 °C		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 1 mA; T_{amb} = 25 °C		200	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA; T_{amb} = 25 °C		-	-	100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA; T_{amb} = 25 °C		-	585	500	mV
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 10 mA; T_{amb} = 25 °C		1.3	0.88	-	V
R1	bias resistor 1	T_{amb} = 25 °C	[1]	3.3	4.7	6.1	kΩ
TR1 (NPN)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz
TR2 (PNP)							
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	3	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions
[2] Characteristics of built-in transistor



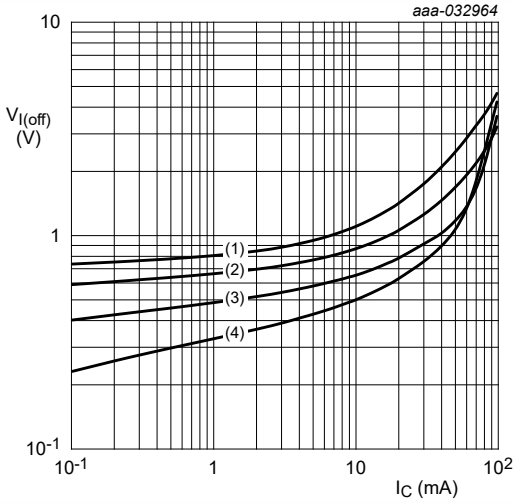
V_{CE} = 5 V
(1) T_{amb} = 175 °C
(2) T_{amb} = 150 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values



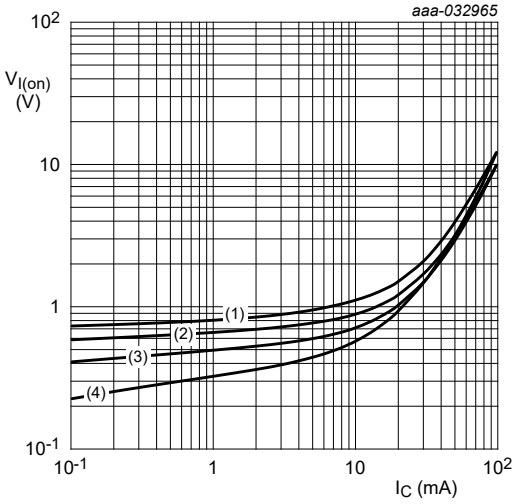
T_{amb} = 25 °C

Fig. 4. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



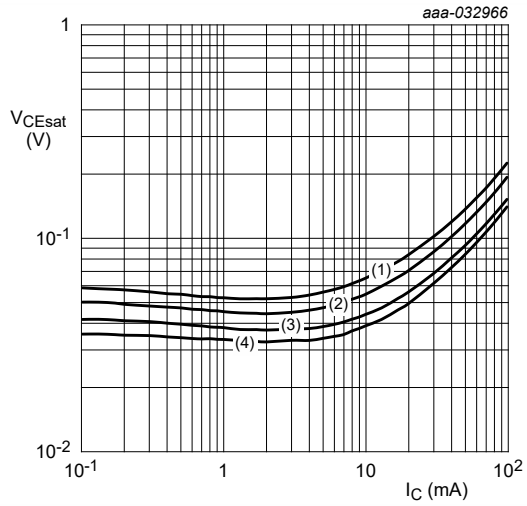
V_{CE} = 5 V
(1) T_{amb} = - 40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
(4) T_{amb} = 175 °C

Fig. 5. TR1 (NPN): Off-state input voltage as a function of collector current; typical values



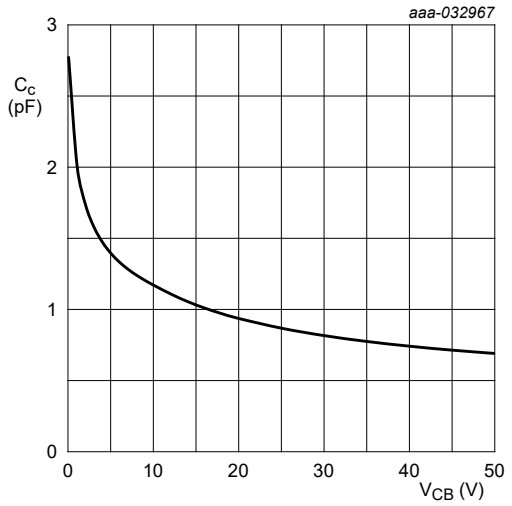
V_{CE} = 0.3 V
(1) T_{amb} = - 40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
(4) T_{amb} = 175 °C

Fig. 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



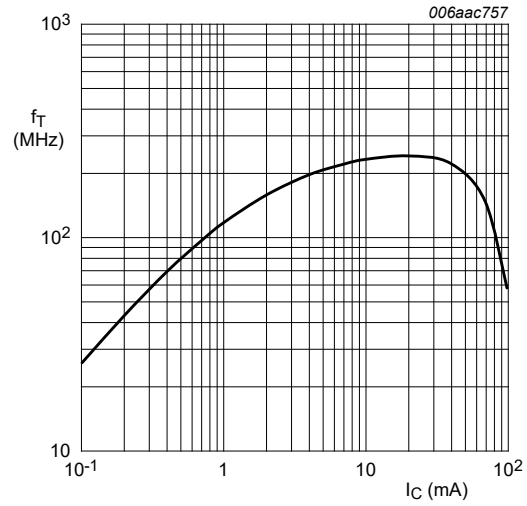
I_C/I_B = 20
(1) T_{amb} = 175 °C
(2) T_{amb} = 100 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 7. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



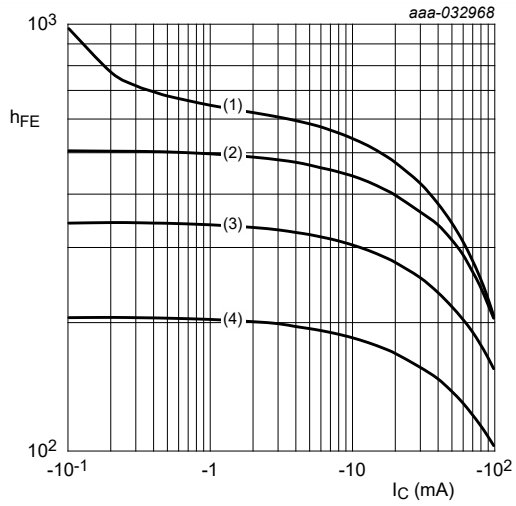
f = 1 MHz
T_{amb} = 25 °C

Fig. 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



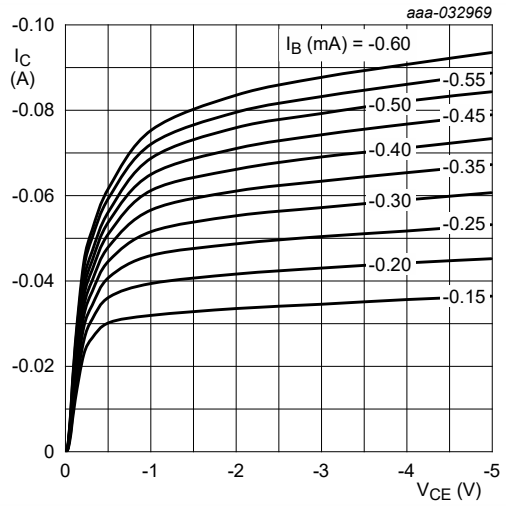
f = 100 MHz
T_{amb} = 25 °C
V_{CE} = 5 V

Fig. 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



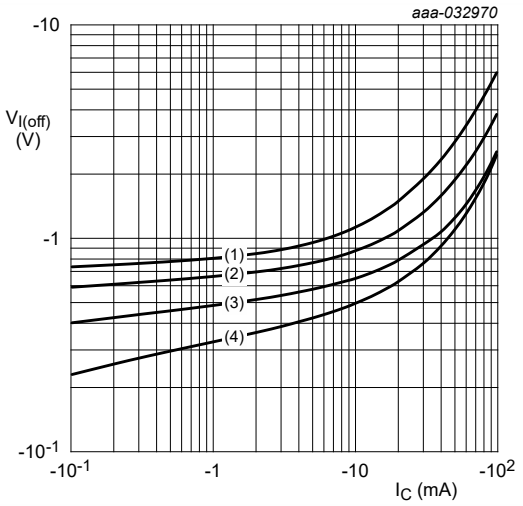
V_{CE} = -5 V
(1) T_{amb} = 175 °C
(2) T_{amb} = 100 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 10. TR2 (PNP): DC current gain as a function of collector current; typical values



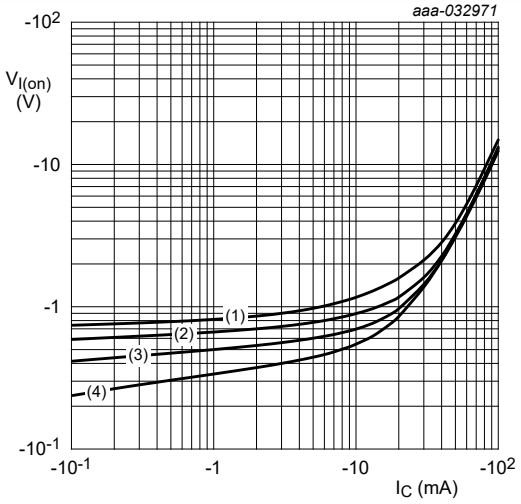
T_{amb} = 25 °C

Fig. 11. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



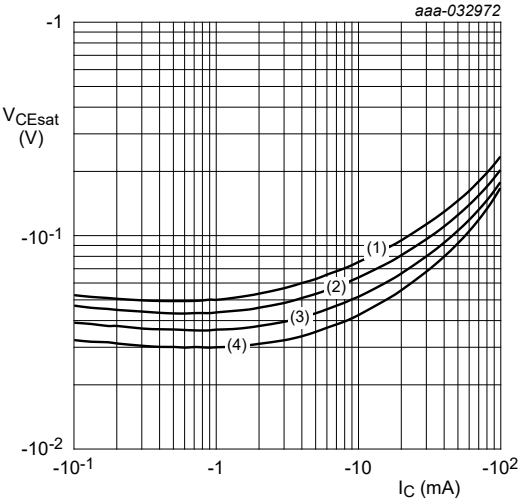
V_{CE} = -5 V
(1) T_{amb} = - 40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
(4) T_{amb} = 175 °C

Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



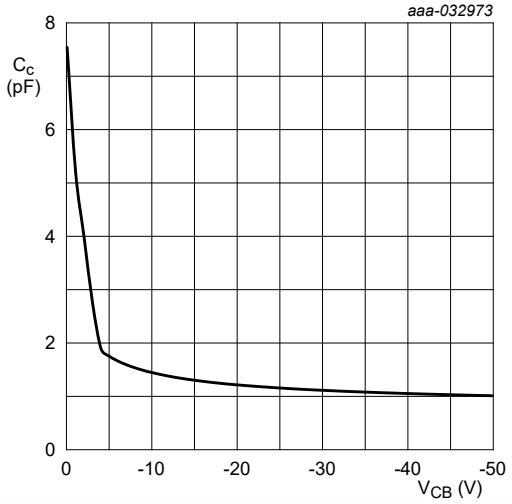
V_{CE} = -0.3 V
(1) T_{amb} = - 40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
(4) T_{amb} = 175 °C

Fig. 13. TR2 (PNP): On-state input voltage as a function of collector current; typical values



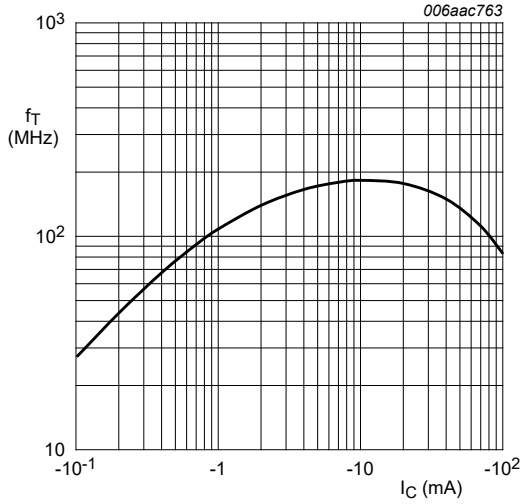
I_C/I_B = 20
(1) T_{amb} = 175 °C
(2) T_{amb} = 100 °C
(3) T_{amb} = 25 °C
(4) T_{amb} = -40 °C

Fig. 14. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



f = 1 MHz
T_{amb} = 25 °C

Fig. 15. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



f = 100 MHz
T_{amb} = 25 °C
V_{CE} = -5 V

Fig. 16. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

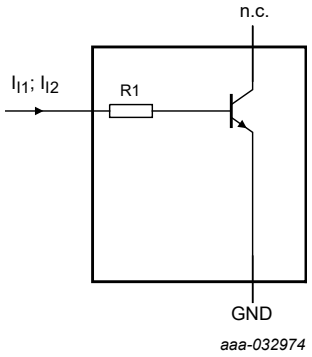


Fig. 17. TR1 (NPN): Resistor test circuit

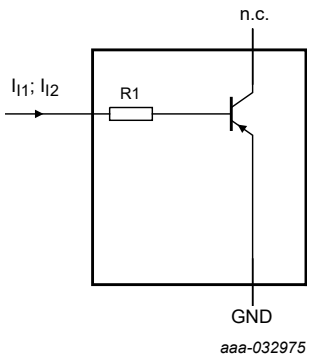


Fig. 18. TR2 (PNP): Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions	
			I_{I1}	I_{I2}
Per transistor, for the PNP transistor with negative polarity				
PUMD6H-Q	4.7	open	600 µA	700 µA

12. Package outline

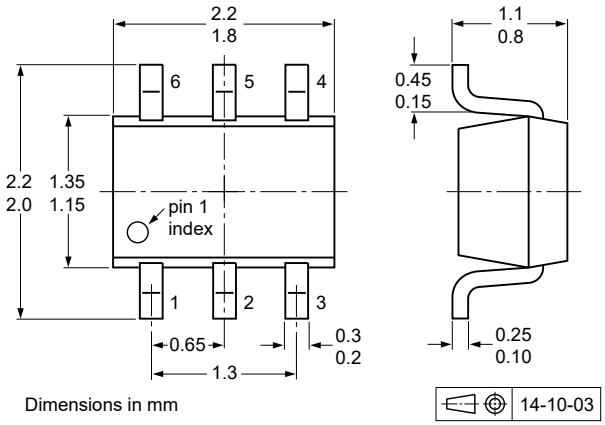


Fig. 19. Package outline TSSOP6 (SOT363)

13. Soldering

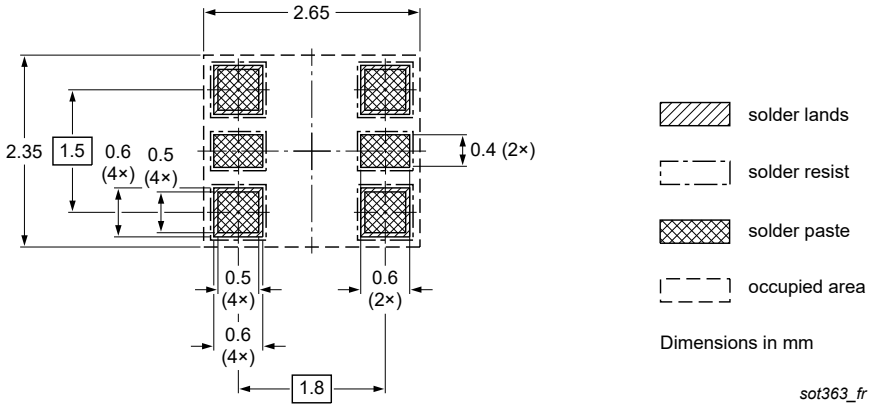


Fig. 20. Reflow soldering footprint for TSSOP6 (SOT363)

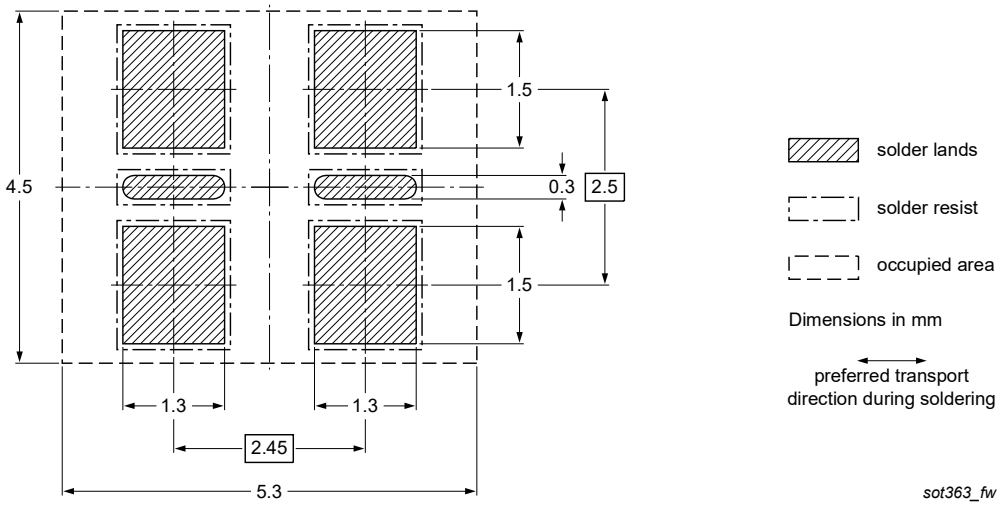


Fig. 21. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD6H-Q v.1	20210506	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 6 May 2021

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