



# PSMP033-60YE

60 V, P-channel Trench MOSFET

13 January 2021

Product data sheet

## 1. General description

P-channel enhancement mode MOSFET in an LFLPAK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology

## 3. Applications

- Reverse battery protection
- Power management
- High-side load switch
- Motor drive

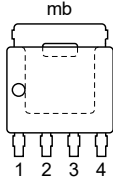
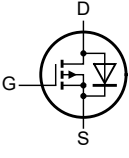
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-60	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	-30	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	110	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -7\text{ A}; T_j = 25\text{ °C}$	-	26	33	mΩ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LFPAK56; Power-SO8 (SOT669)</b></p>	 <p>017aaa094</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMP033-60YE	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMP033-60YE	03360YE

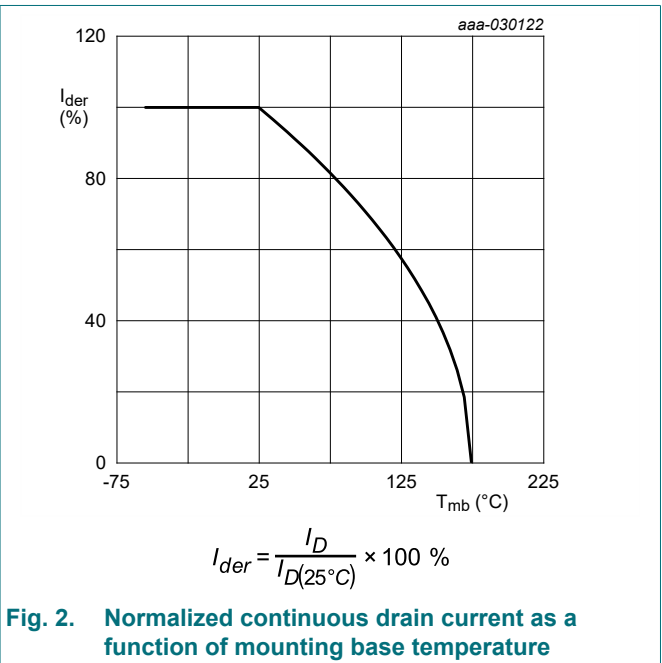
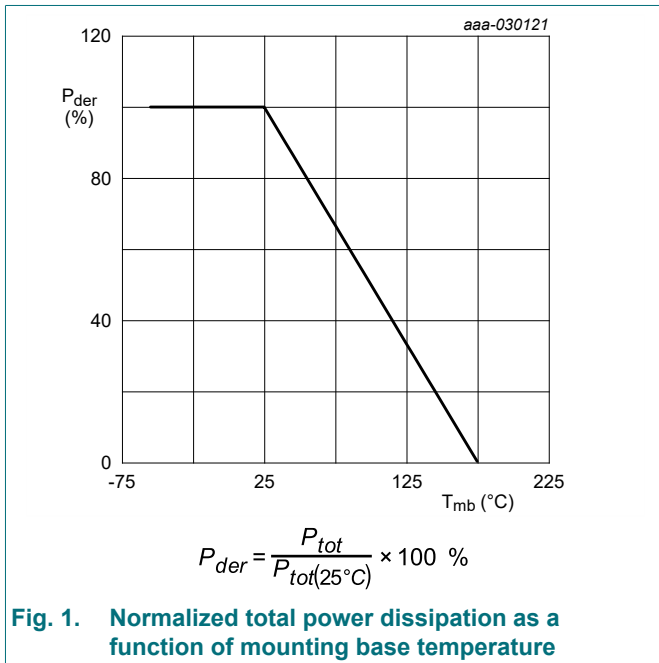
## 8. Limiting values

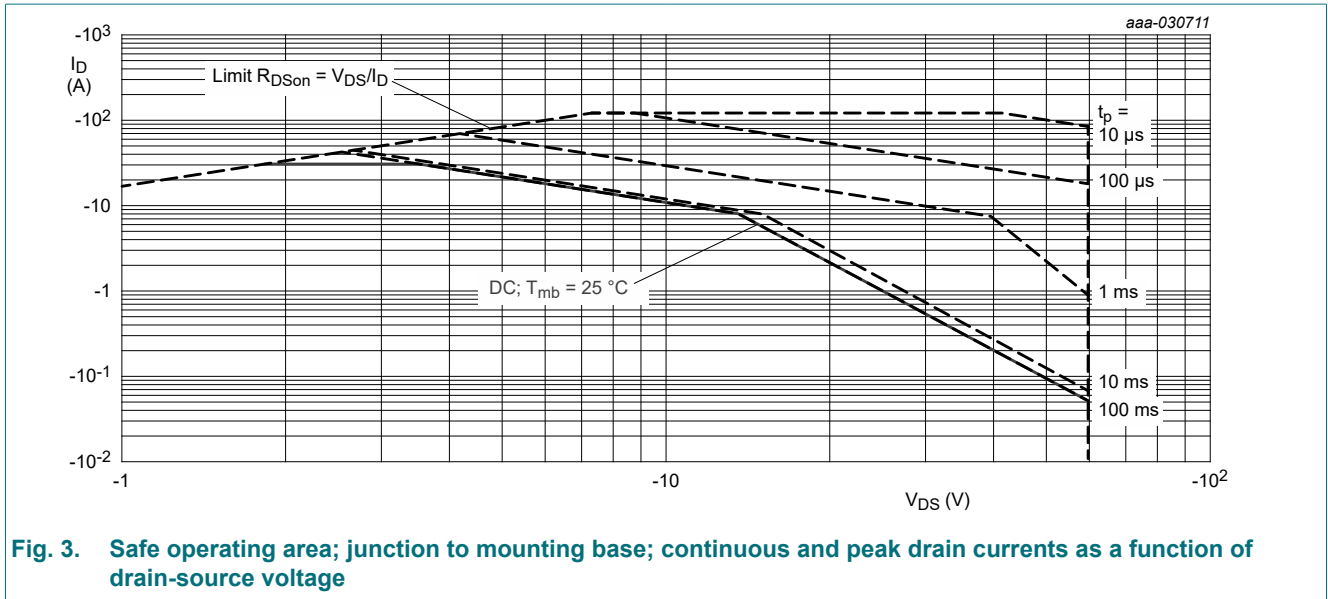
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	-60	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -10 V; T <sub>mb</sub> = 25 °C	-	-30	A
		V <sub>GS</sub> = -10 V; T <sub>mb</sub> = 100 °C	-	-21	A
I <sub>DM</sub>	peak drain current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	-120	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C	-	110	W
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>amb</sub>	ambient temperature		-55	175	°C
T <sub>stg</sub>	storage temperature		-65	175	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	-30	A
I <sub>SM</sub>	peak source current	single pulse; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	-120	A
<b>ESD maximum rating</b>					
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[1]	1000	V
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = -2.8 A; DUT in avalanche (unclamped)	-	85	mJ

[1] Measured between all pins.



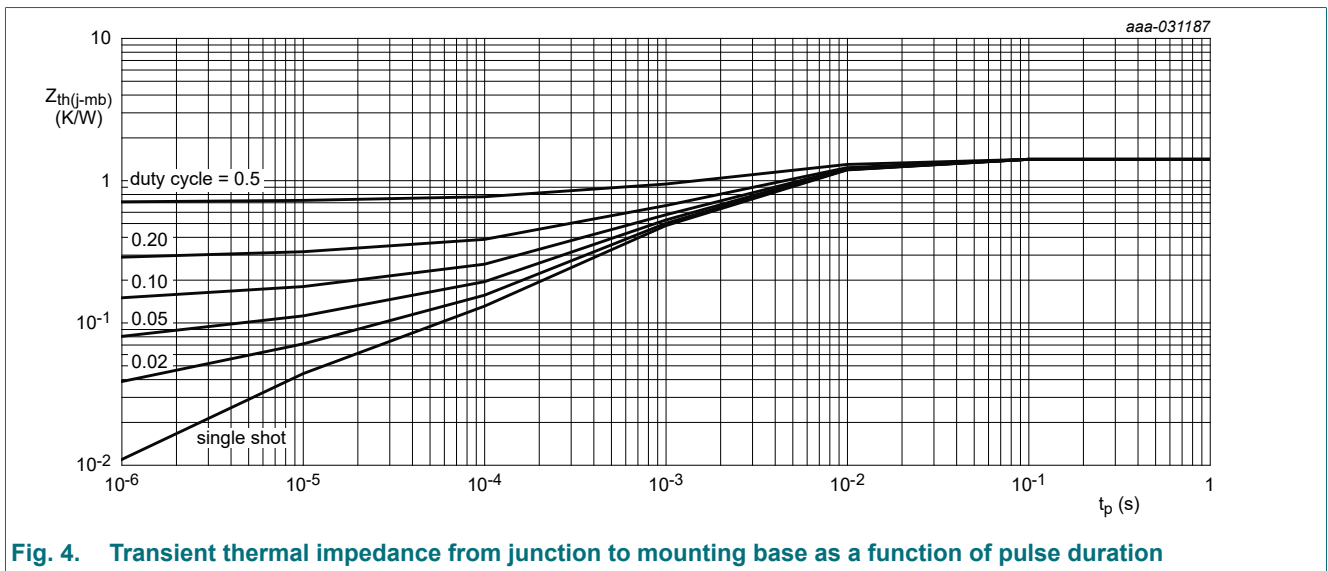


### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	83	91	K/W
			[2]	-	46	51	K/W
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base		-	1.1	1.4	K/W	

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



## 10. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-60	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 ^\circ C$	-1.5	-2	-3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -60 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -60 V$ ; $V_{GS} = 0 V$ ; $T_j = 125 ^\circ C$	-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-	-100	nA
		$V_{GS} = 20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 V$ ; $I_D = -7 A$ ; $T_j = 25 ^\circ C$	-	26	33	m $\Omega$
		$V_{GS} = -10 V$ ; $I_D = -7 A$ ; $T_j = 175 ^\circ C$	-	55	69	m $\Omega$
		$V_{GS} = -4.5 V$ ; $I_D = -6.7 A$ ; $T_j = 25 ^\circ C$	-	30	36	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V$ ; $I_D = -4.8 A$ ; $T_j = 25 ^\circ C$	-	99	-	S
$R_G$	gate resistance	$f = 1 MHz$	-	6.1	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -30 V$ ; $I_D = -7 A$ ; $V_{GS} = -10 V$ ; $T_j = 25 ^\circ C$	-	46	69	nC
$Q_{GS}$	gate-source charge		-	7.3	-	nC
$Q_{GD}$	gate-drain charge		-	9.4	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -30 V$ ; $f = 1 MHz$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-	2590	-	pF
$C_{oss}$	output capacitance		-	202	-	pF
$C_{rss}$	reverse transfer capacitance		-	118	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -30 V$ ; $I_D = -7 A$ ; $V_{GS} = -10 V$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 ^\circ C$	-	9	-	ns
$t_r$	rise time		-	16	-	ns
$t_{d(off)}$	turn-off delay time		-	81	-	ns
$t_f$	fall time		-	310	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -30 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-	-0.7	-1.2	V
$t_{rr}$	reverse recovery time	$I_S = -30 A$ ; $di_S/dt = 100 A/\mu s$ ;	-	32	-	ns
$Q_r$	recovered charge	$V_{GS} = -10 V$ ; $V_{DS} = -30 V$ ; $T_j = 25 ^\circ C$	-	18	-	nC

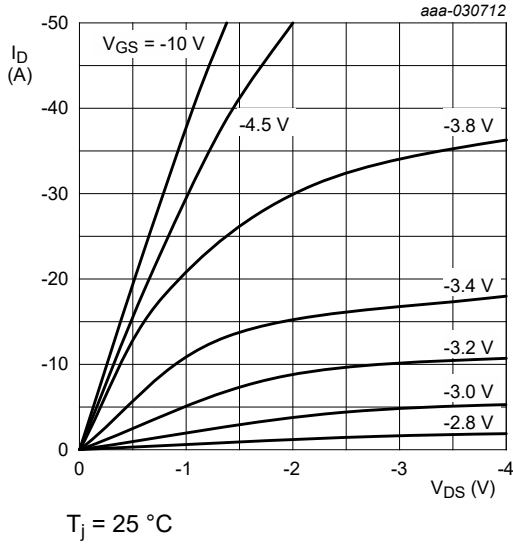


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

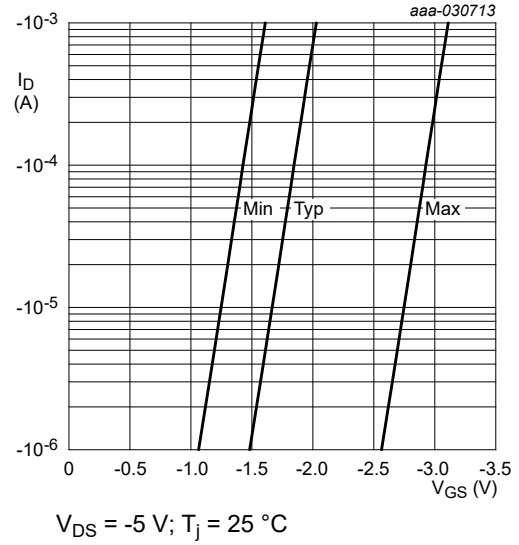


Fig. 6. Sub-threshold drain current as a function of gate-source voltage

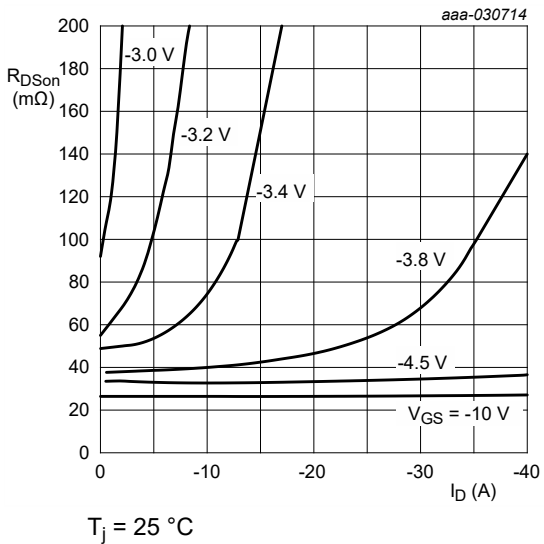


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

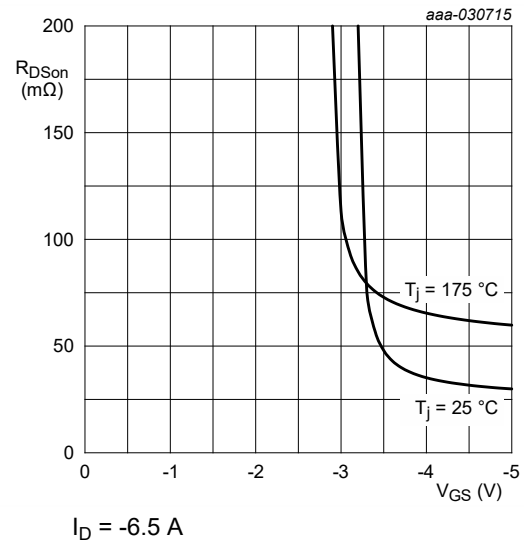


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

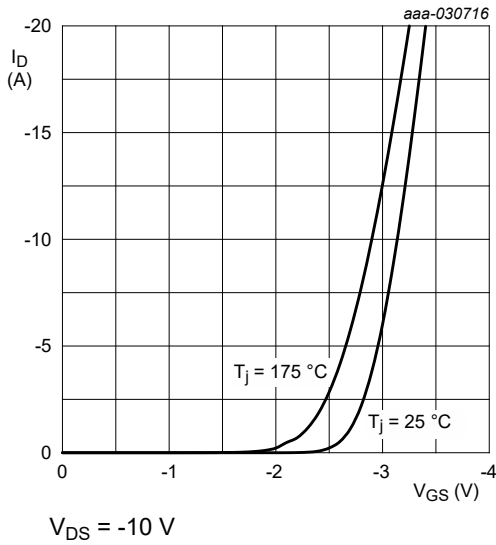


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

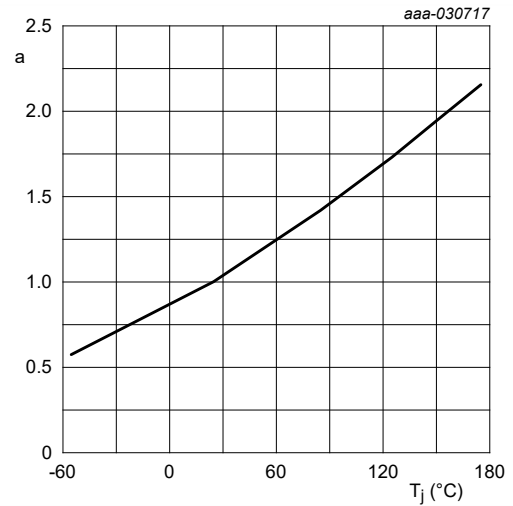


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

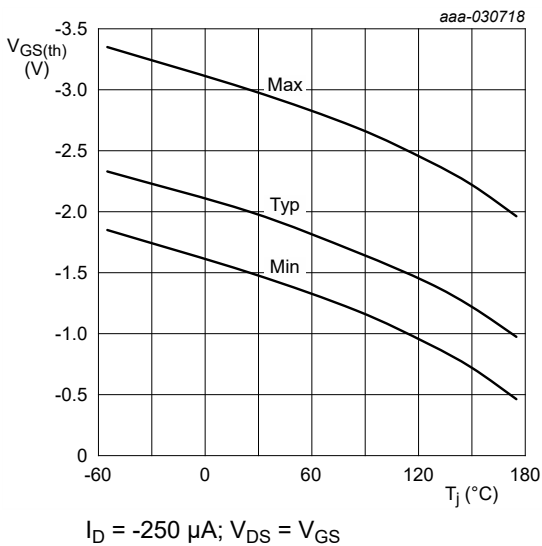


Fig. 11. Gate-source threshold voltage as a function of junction temperature

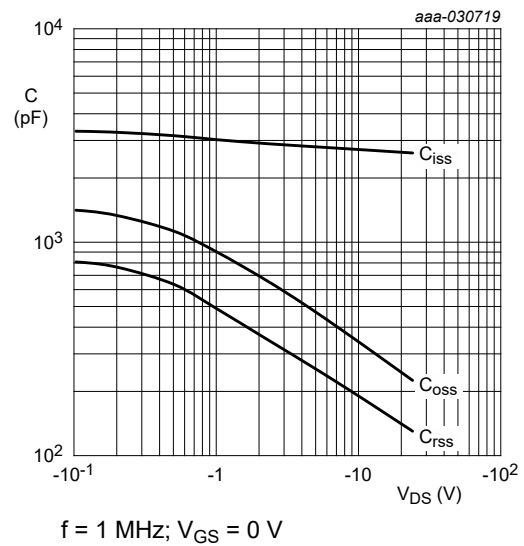
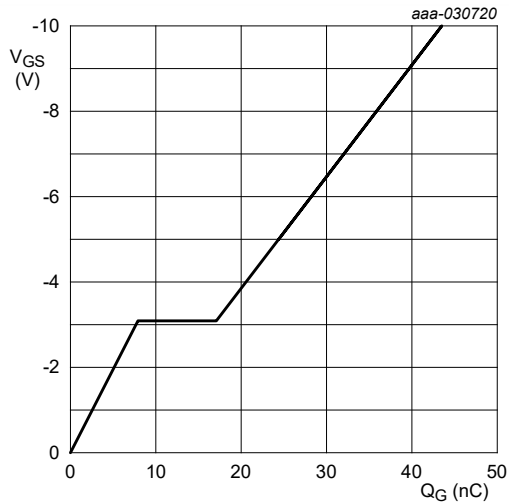


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -30\text{ V}$ ;  $I_D = -10.8\text{ A}$ ;  $T_j = 25\text{ }^\circ\text{C}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

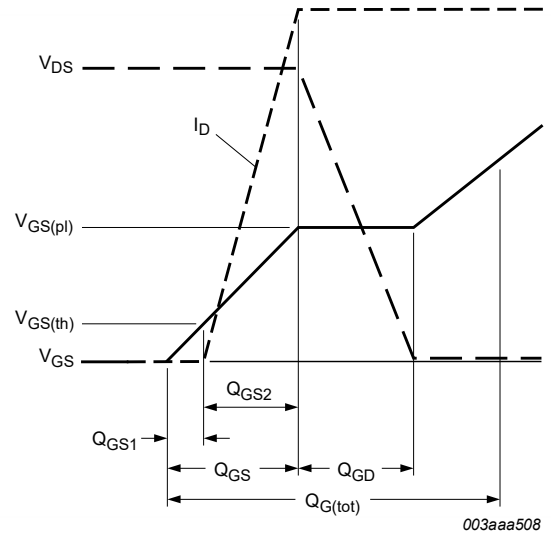
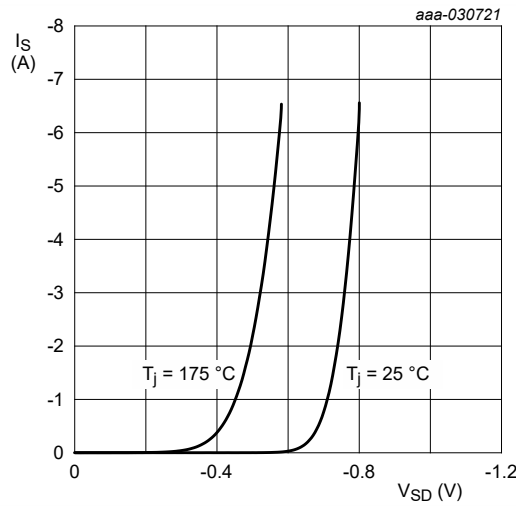


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 15. Source current as a function of source-drain voltage; typical values



## 11. Test information

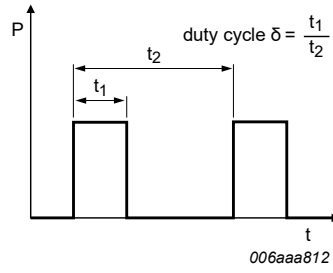


Fig. 16. Duty cycle definition

12. Package outline

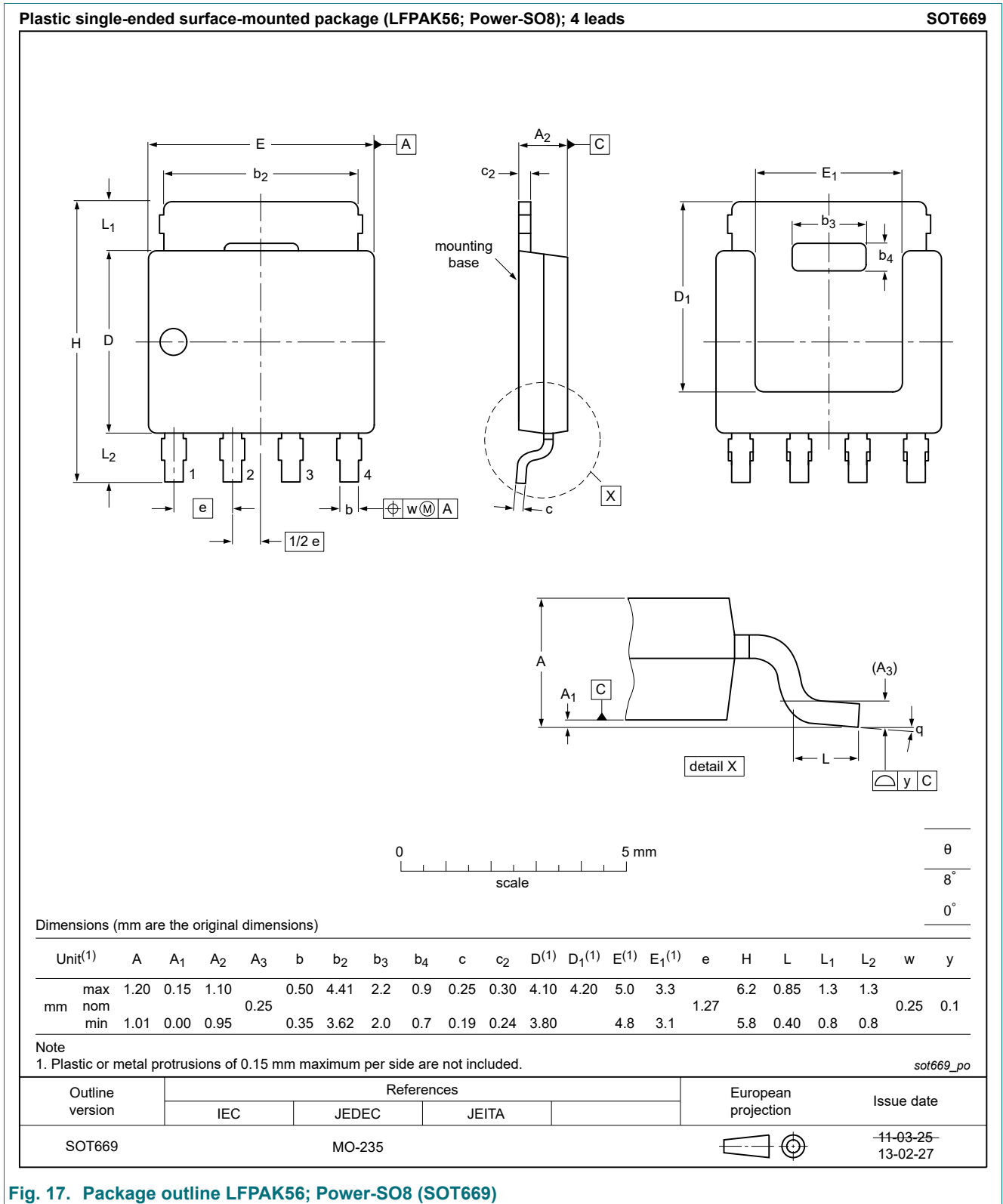


Fig. 17. Package outline LFAK56; Power-SO8 (SOT669)

### 13. Soldering

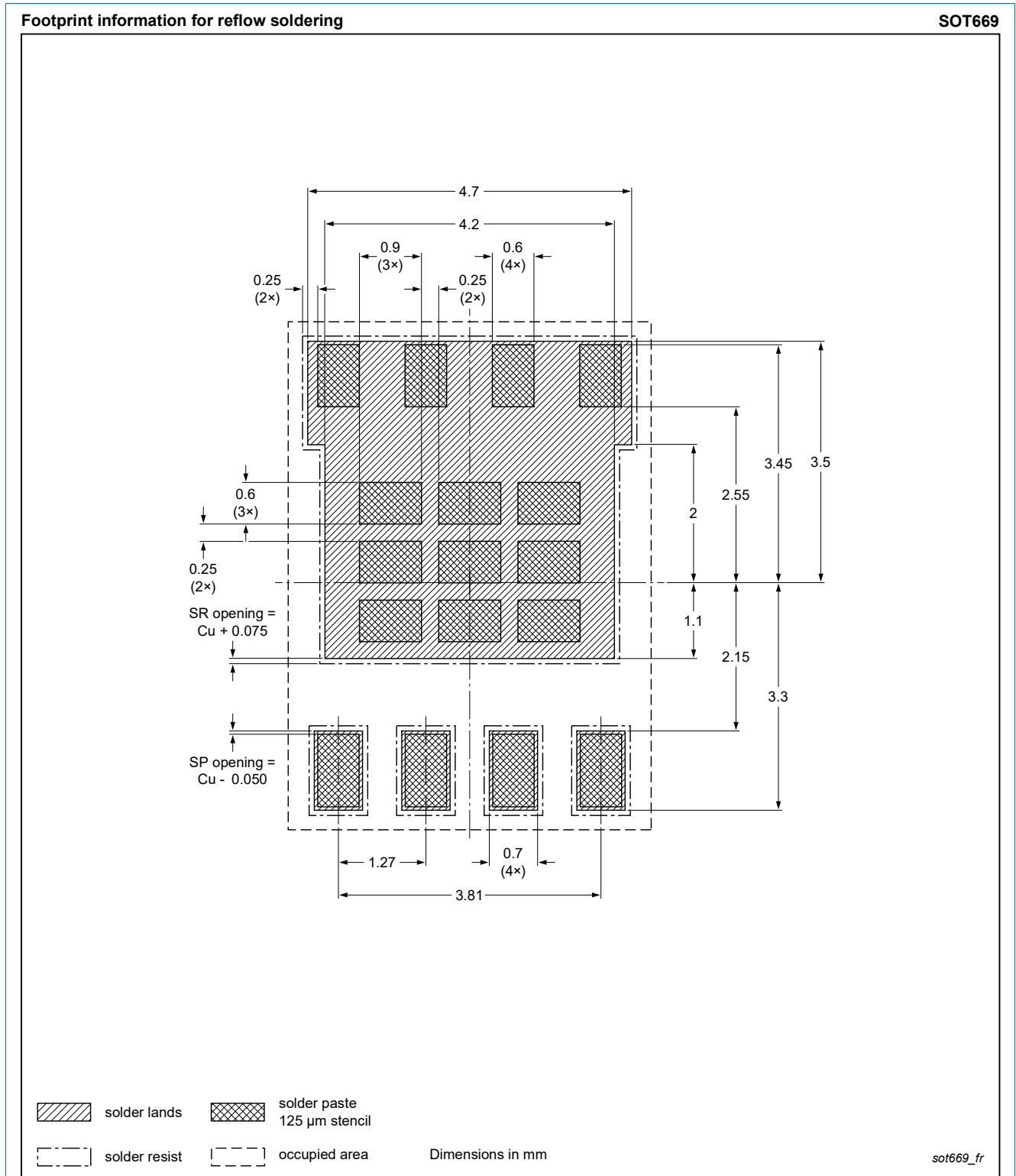
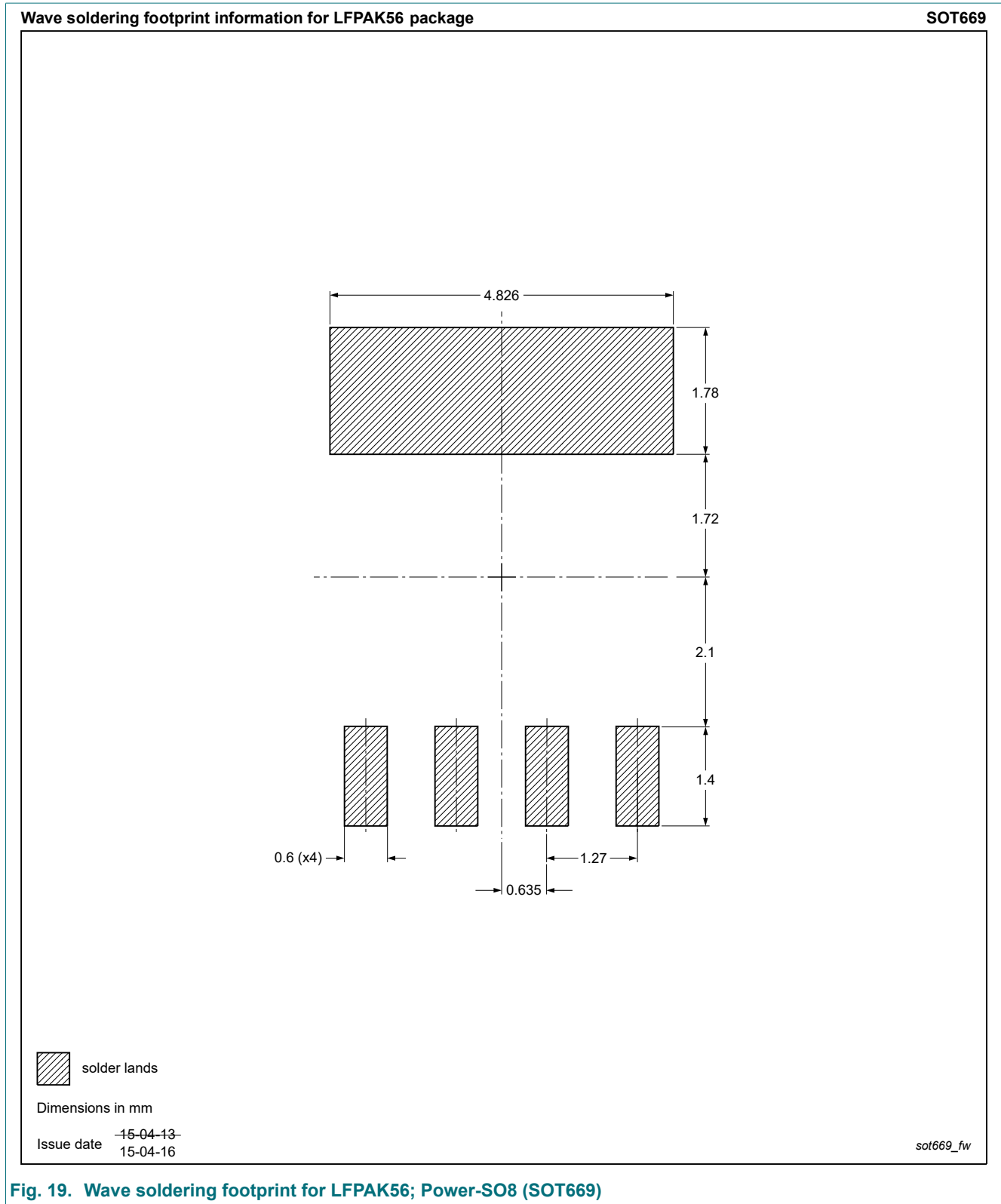


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)



### 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PSMP033-60YE v.1	20210113	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## Contents

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1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Test information.....	9
12. Package outline.....	10
13. Soldering.....	11
14. Revision history.....	13
15. Legal information.....	14

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