



PUMD48

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

1 October 2022

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

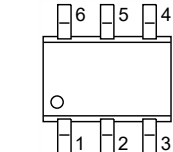
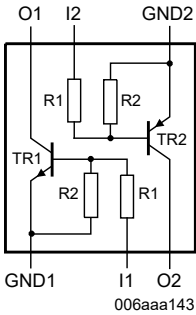
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
I _O	output current			-	-	100	mA
Transistor TR1 (NPN)							
R1	bias resistor 1 (input)		[1]	33	47	61	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
Transistor TR2 (PNP)							
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	

[1] See section "Test information" for resistor calculation and test conditions.

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 TSSOP6 (SOT363)	 006aaa143
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD48	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD48	4%8

[1] % = placeholder for manufacturing site code

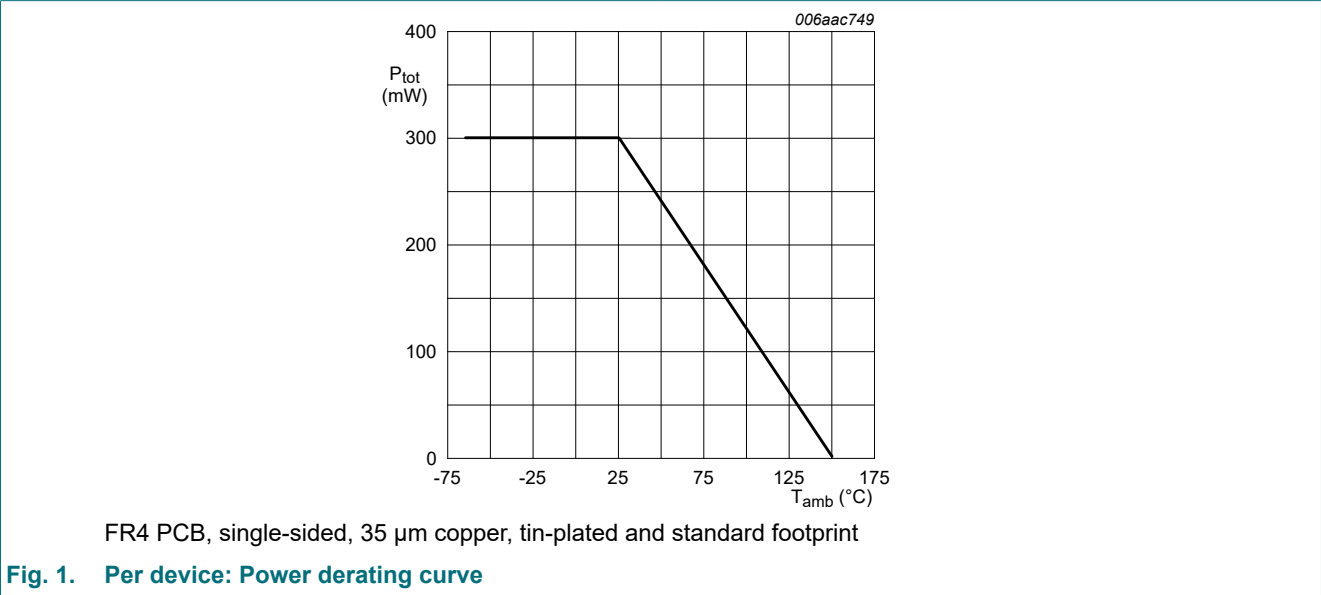
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R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector TR1 (NPN)		-	10	V
		open collector TR2 (PNP)		-	-5	V
V _I	input voltage	positive (input voltage TR1)		-	40	V
		negative (input voltage TR1)		-	-10	V
		positive (input voltage TR2)		-	5	V
		negative (input voltage TR2)		-	-12	V
I _O	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



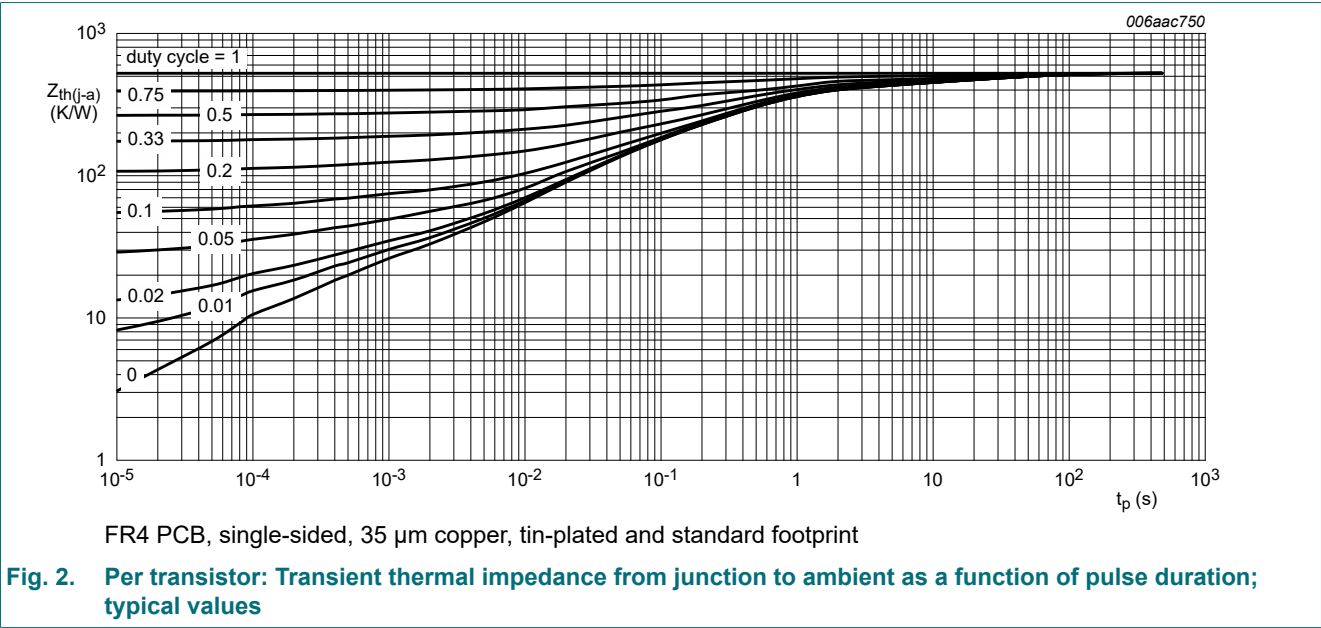
50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

10. Characteristics

Table 7. Characteristics

$T_{amb} = 25\text{ °C}$, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
V _{(BR)CBO}	collector-base breakdown voltage	I _C = 100 μA; I _E = 0 A		50	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	I _C = 2 mA; I _B = 0 A		50	-	-	V
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A		-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A		-	-	1	μA
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μA
Transistor TR1 (NPN)							
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A		-	-	90	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA		80	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA		-	-	100	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA		-	1.2	0.8	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 2 mA		3	1.6	-	V
R1	bias resistor 1 (input)		[1]	33	47	61	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz		-	-	2.5	pF
f _T	transition frequency	V _{CE} = 5 V; I _C = 10 mA; f = 100 MHz	[2]	-	230	-	MHz
Transistor TR2 (PNP)							
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A		-	-	-180	μA
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -10 mA		100	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -5 mA; I _B = -0.25 mA		-	-	-100	mV
V _{I(off)}	off-state input voltage	V _{CE} = -5 V; I _C = -100 μA		-	-0.6	-0.5	V
V _{I(on)}	on-state input voltage	V _{CE} = -0.3 V; I _C = -5 mA		-1.1	-0.75	-	V
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz		-	-	3	pF
f _T	transition frequency	V _{CE} = -5 V; I _C = -10 mA; f = 100 MHz	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

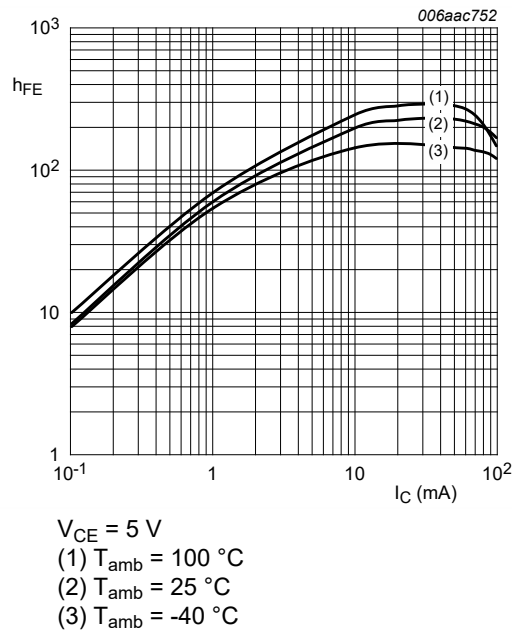


Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values

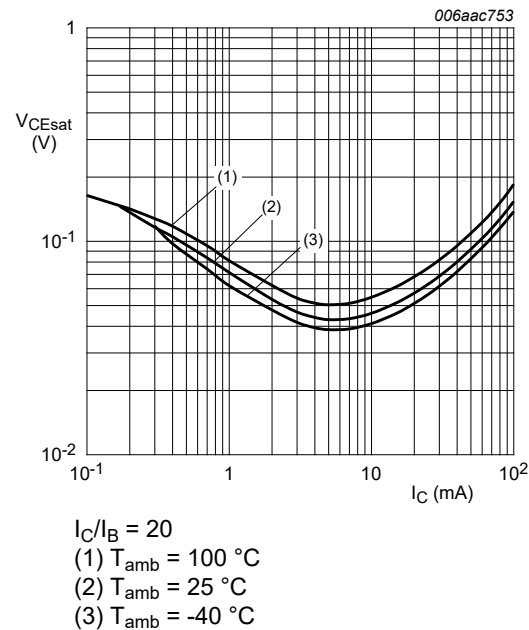


Fig. 4. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

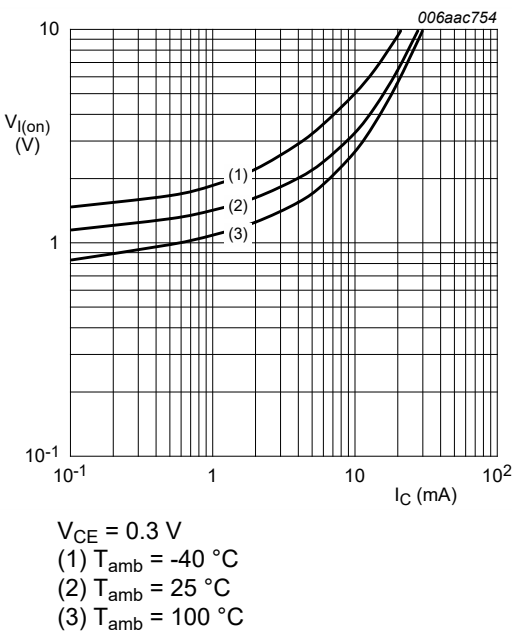


Fig. 5. TR1 (NPN): On-state input voltage as a function of collector current; typical values

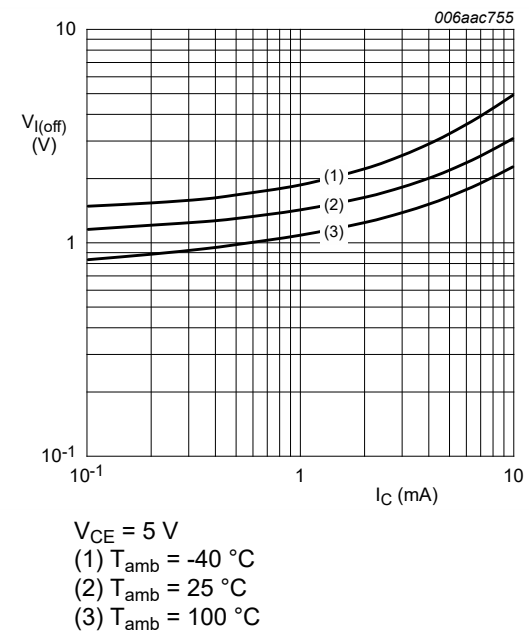


Fig. 6. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

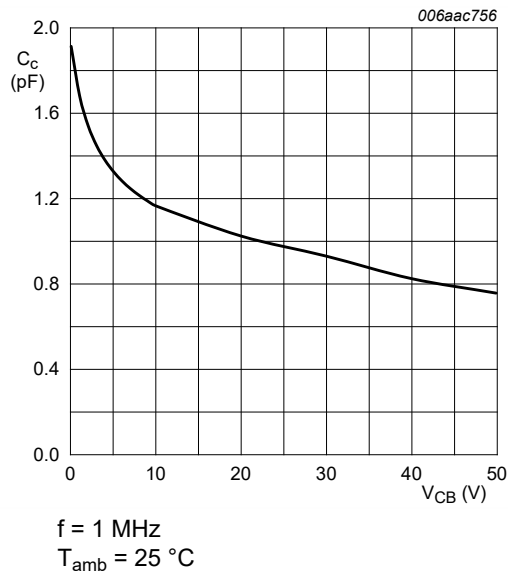


Fig. 7. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values

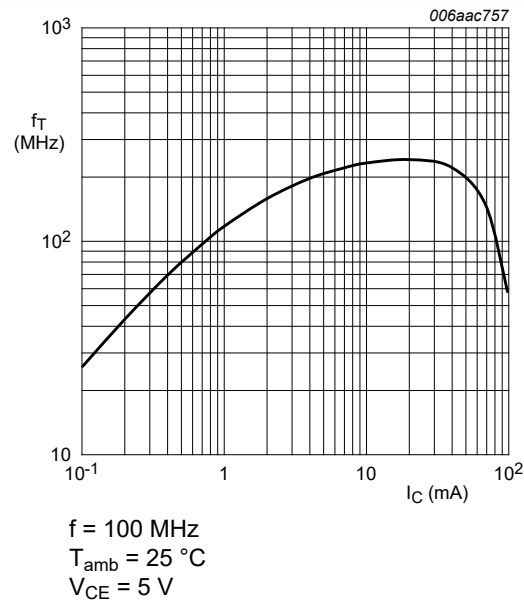


Fig. 8. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor

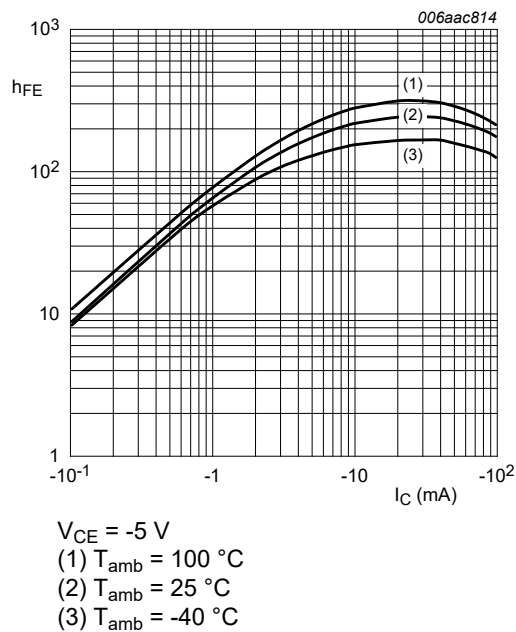


Fig. 9. TR2 (PNP): DC current gain as a function of collector current; typical values

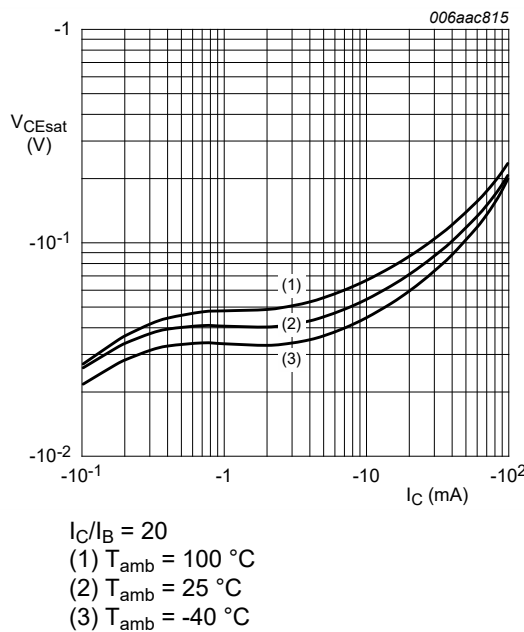


Fig. 10. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

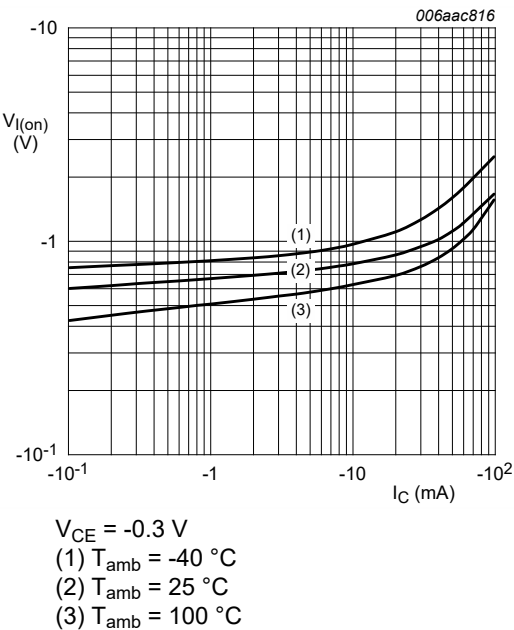


Fig. 11. TR2 (PNP): On-state input voltage as a function of collector current; typical values

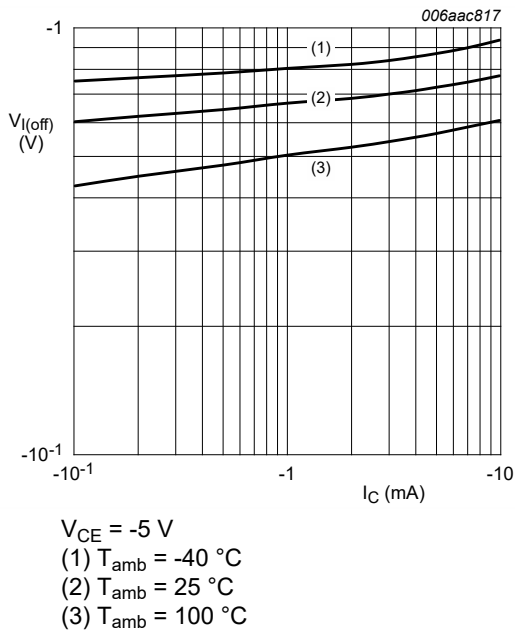


Fig. 12. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

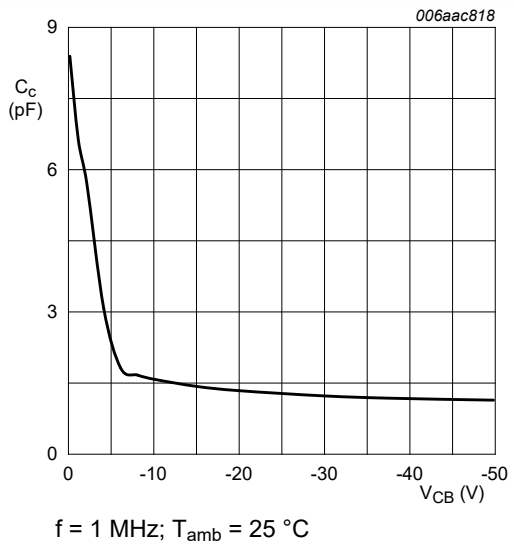


Fig. 13. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

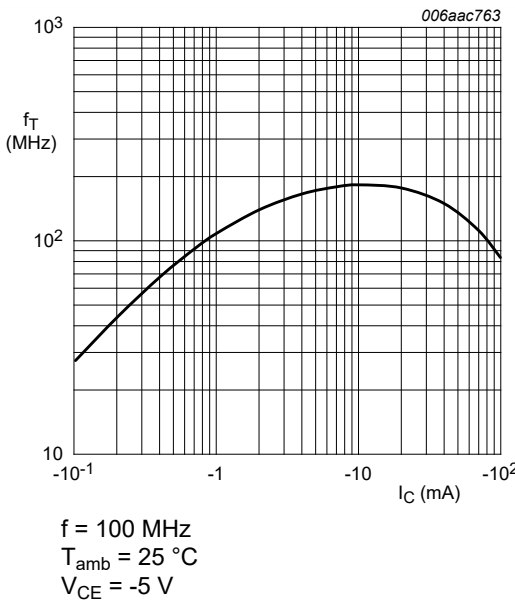


Fig. 14. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

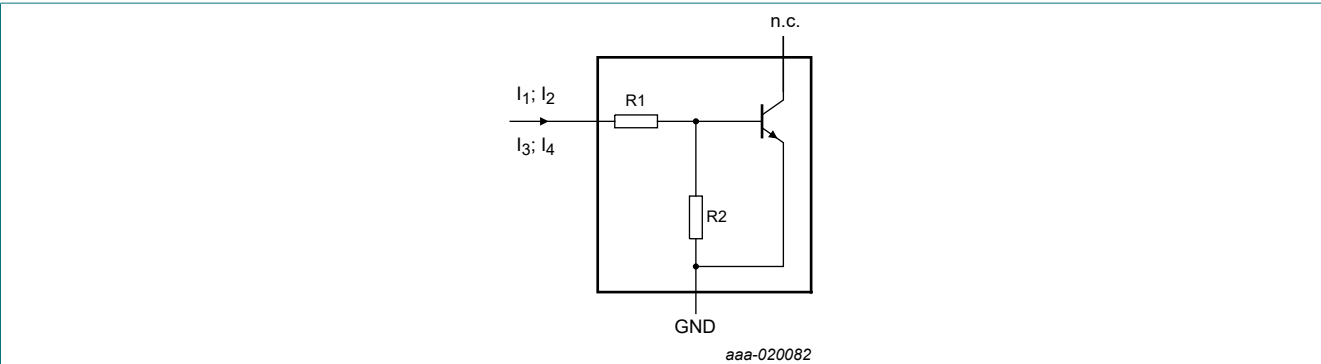


Fig. 15. NPN transistor: Resistor test circuit

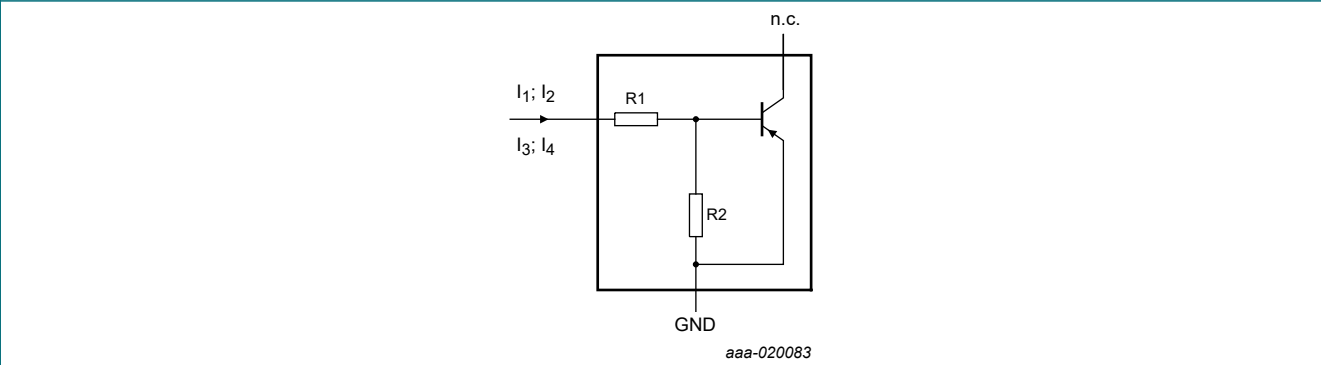


Fig. 16. PNP transistor: Resistor test circuit

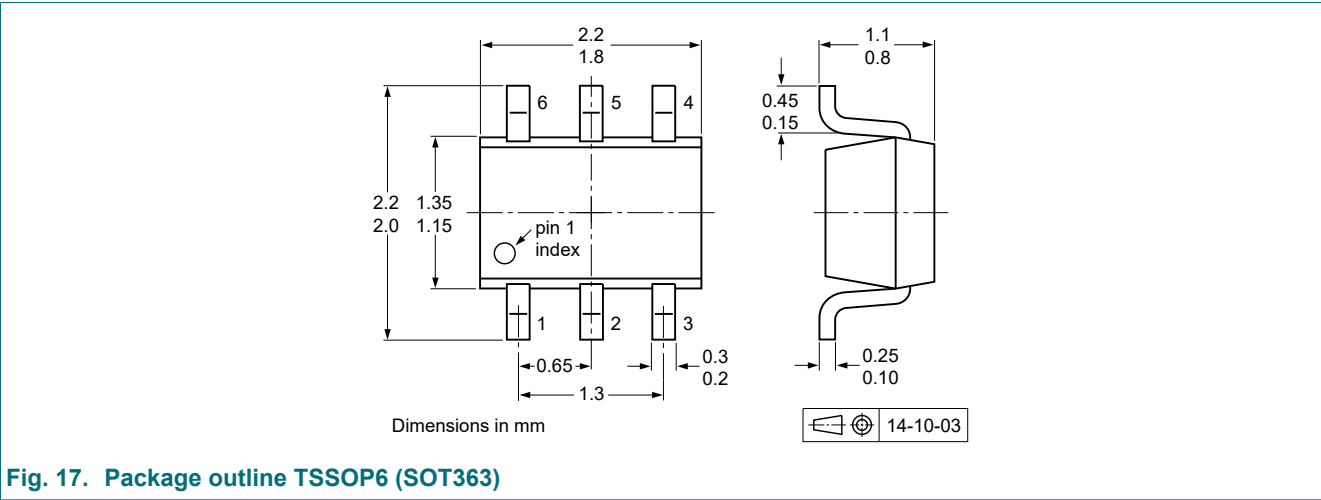
Resistor test conditions

Table 8. Resistor test conditions

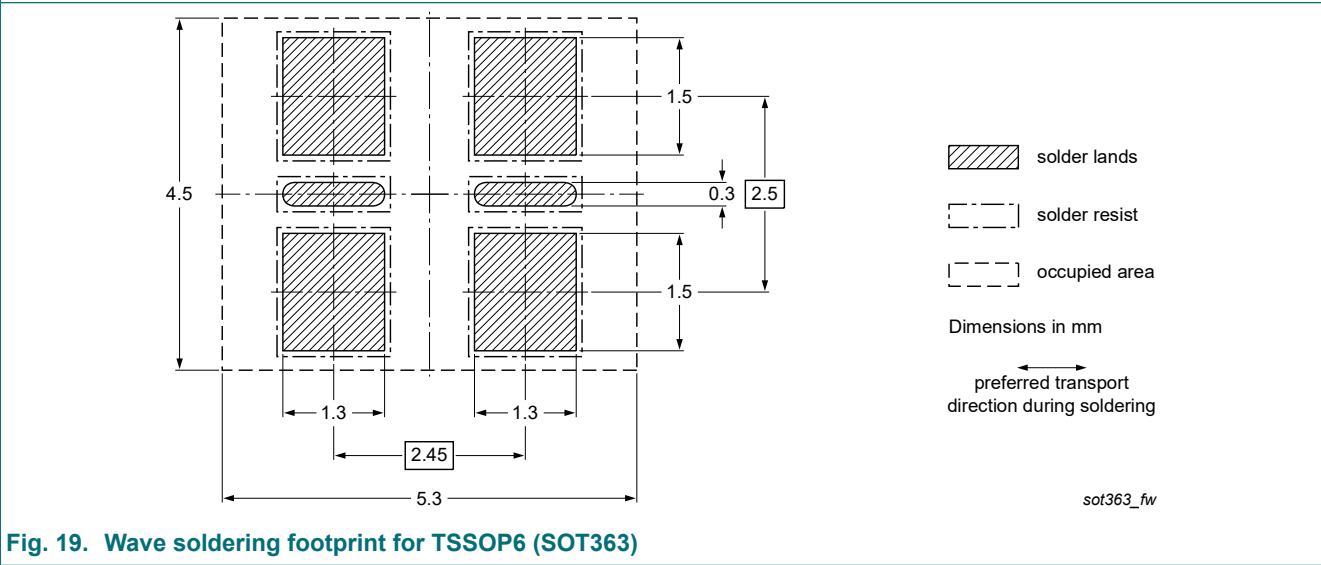
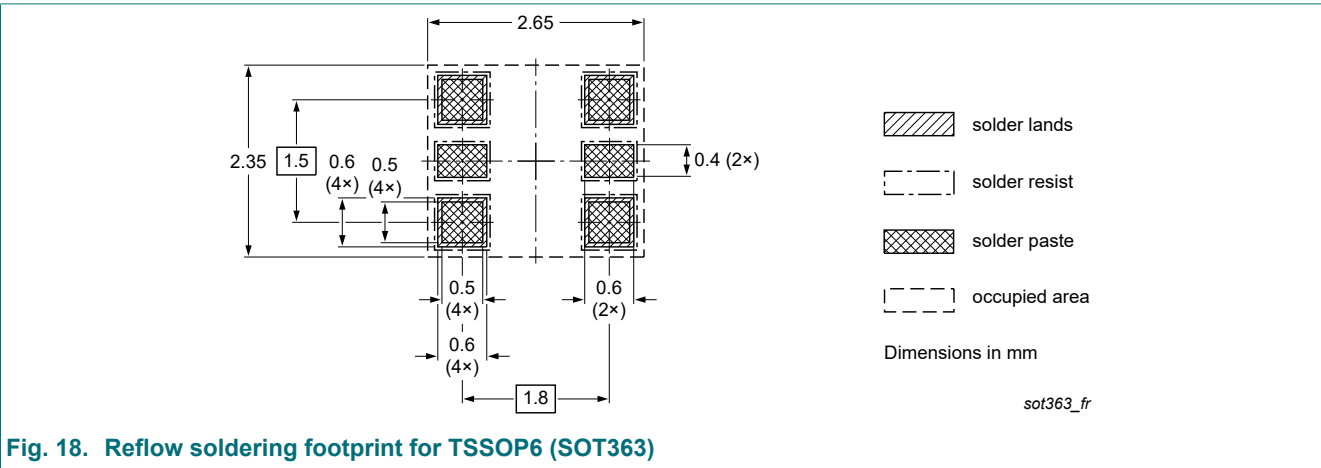
PUMD48	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
TR1 (NPN)	47	47	55 μA	105 μA	-55 μA	-105 μA
TR2 (PNP)	2.2	47	-90 μA	-140 μA	55 μA	105 μA

50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

12. Package outline



13. Soldering



50 V, 100 mA NPN/PNP resistor-equipped double transistor;
R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD48 v.7	20221001	Product data sheet	-	PEMD48_PUMD48 v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s). Packing information is removed. 			
PEMD48_PUMD48 v.6	20120124	Product data sheet	-	PEMD48_PUMD48 v.5
PEMD48_PUMD48 v.5	20100413	Product data sheet	-	PEMD48_PUMD48 v.4
PEMD48_PUMD48 v.4	20040624	Product specification	-	PEMD48_PUMD48 v.3
PEMD48_PUMD48 v.3	20040602	Product specification	-	PUMD48 v.2 PEMD48 v.2
PUMD48 v.2	20010201	Product specification	-	PUMD48 v.1
PUMD48 v.1	19990422	Product specification	-	-
PEMD48 v.2	20011107	Product specification	-	PEMD48 v.1
PEMD48 v.1	20010924	Preliminary specification	-	-

50 V, 100 mA NPN/PNP resistor-equipped double transistor;

R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

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15. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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