PSMN1R5-30YLC

N-channel 30 V 1.55mΩ logic level MOSFET in LFPAK using NextPower technology

3 June 2021 **Product data sheet**

1. General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low Rdson and low parasitic inductance

3. Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

4. Quick reference data

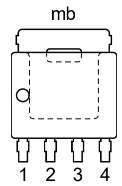
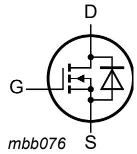
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	30	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	200	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	179	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.65	2.05	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.3	1.55	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15		-	8.6	-	nC
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	65	-	nC

[1] 200A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R5-30YLC	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R5-30YLC	1C530L

8. Limiting values

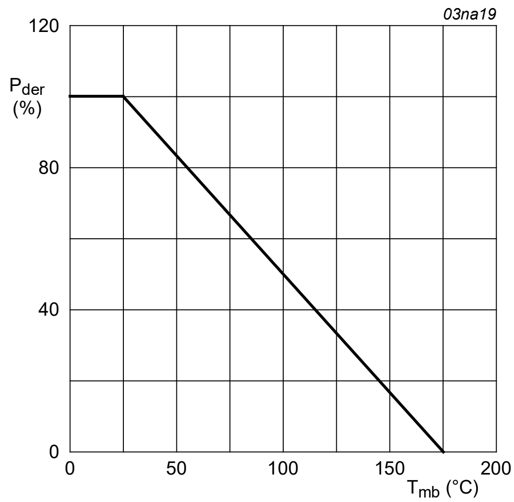
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	179	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	200	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	179	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1016	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	machine model according to JEDEC JESD22-A115		1000	-	V
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	163	A

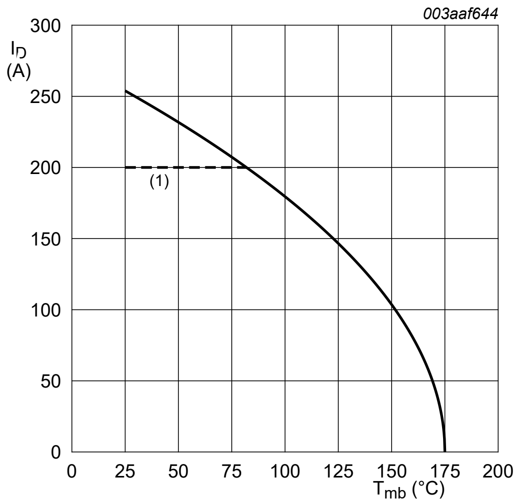
Symbol	Parameter	Conditions		Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \le$ 10 µs; T_{mb} = 25 °C		-	1016	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	147	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 30 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[2]	-	158	A

[1] 200A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test.



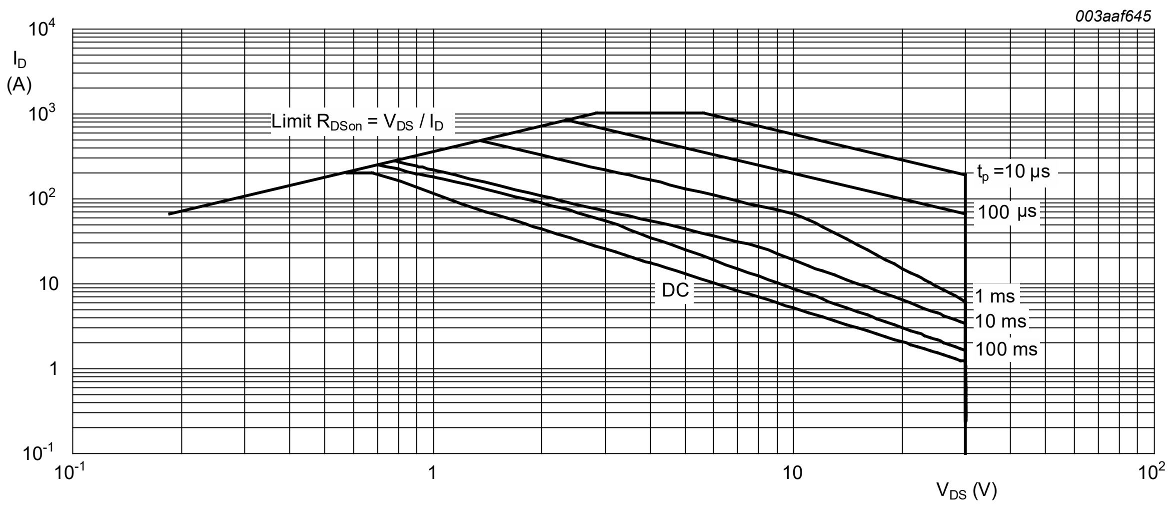
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



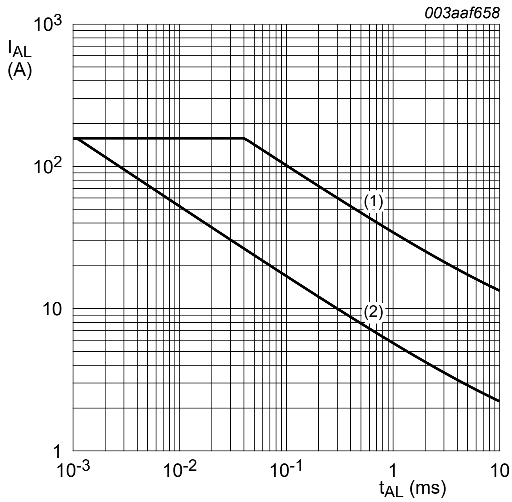
$V_{GS} \ge$ 10V
(1) 200A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25°C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\,(init)}$ = 25°C; (2) $T_{j\,(init)}$ = 150°C;

Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.71	0.84	K/W

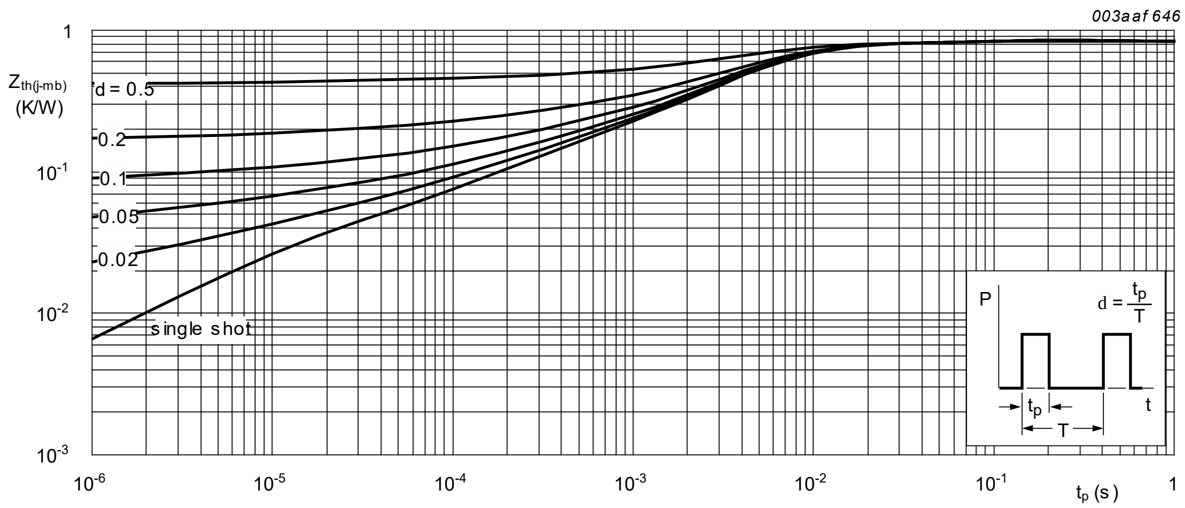


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

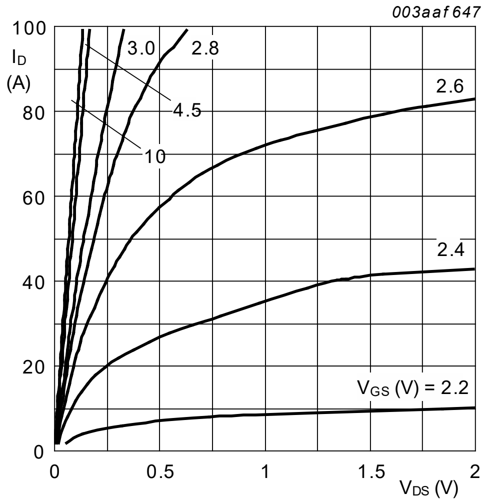
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		27	-	-	V

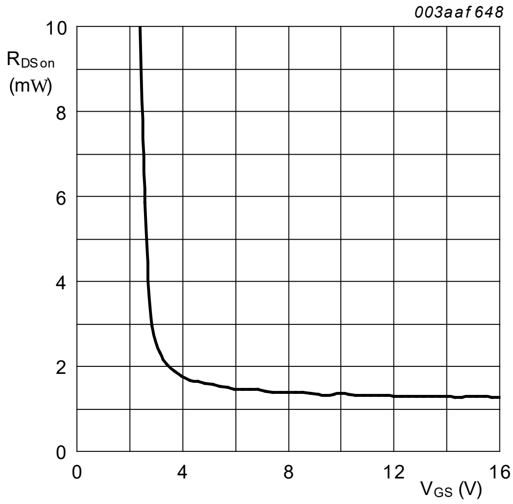
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11	1.05	1.51	1.95	V
		I_D = 10 mA; V_{DS}=V_{GS}; T_j = 150 °C	0.5	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C	-	-	2.25	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12	-	1.65	2.05	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; Fig. 12; Fig. 13	-	-	3.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12	-	1.3	1.55	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; Fig. 12; Fig. 13	-	-	2.6	mΩ
R_G	gate resistance	f = 1 MHz	-	1.05	2.1	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V; Fig. 14; Fig. 15	-	65	-	nC
		I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15	-	30	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V	-	53	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V; Fig. 14; Fig. 15	-	9.7	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.1	-	nC
Q_{GD}	gate-drain charge		-	8.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 15 V; Fig. 14; Fig. 15	-	2.53	-	V
C_{iss}	input capacitance	V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16	-	4044	-	pF
C_{oss}	output capacitance		-	860	-	pF
C_{rss}	reverse transfer capacitance		-	287	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω	-	33	-	ns
t_r	rise time		-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	62	-	ns
t_f	fall time		-	38	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_j = 25 °C	-	23	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17	-	0.8	1.1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V	-	41	-	ns
Q_r	recovered charge		-	43	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_a	reverse recovery rise time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 15 V; Fig. 18		-	24	-	ns
t_b	reverse recovery fall time			-	17	-	ns



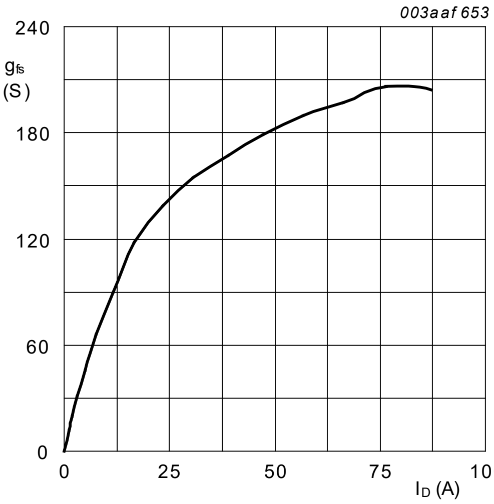
$T_j = 25°C$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



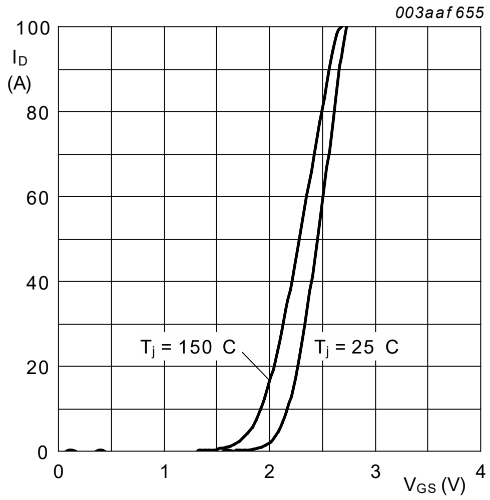
T_j = 25°C; I_D = 25A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



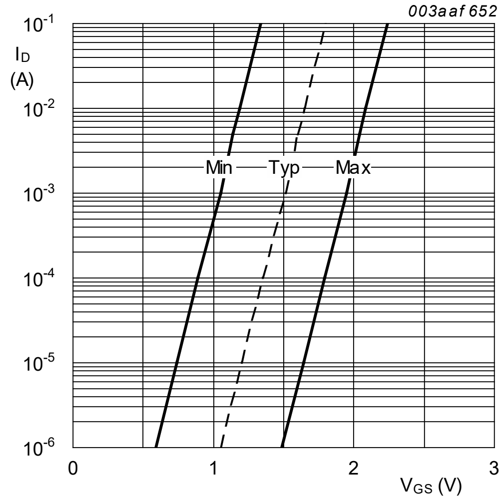
T_j = 25°C; V_{DS} = 10V

Fig. 8. Forward transconductance as a function of drain current; typical values



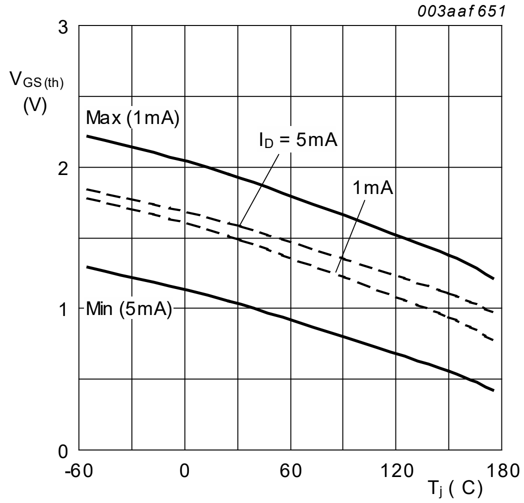
$V_{DS} = 10V$

Fig. 9. Transfer characteristics; drain-source current as a function of gate-source voltage; typical values



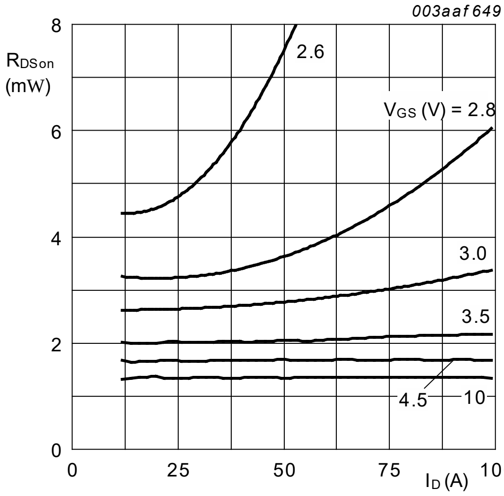
T_j = 25°C; V_{DS} = 5V

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



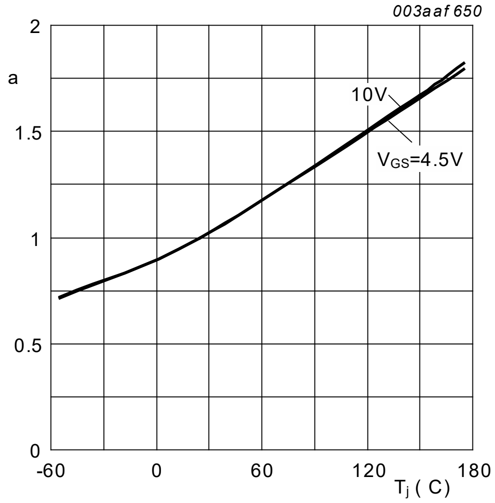
$V_{DS} = V_{GS}$

Fig. 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25°C$

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

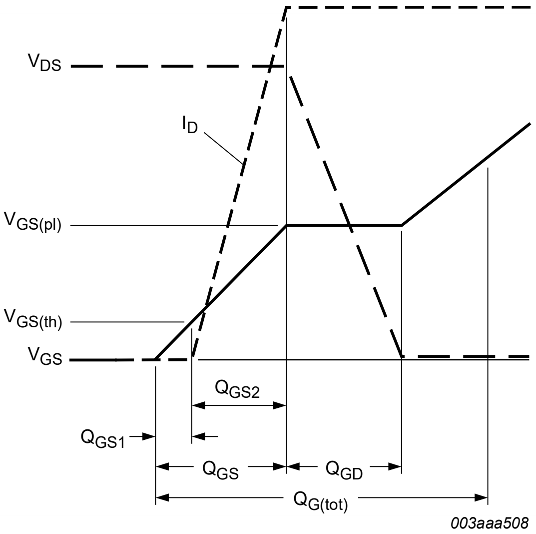
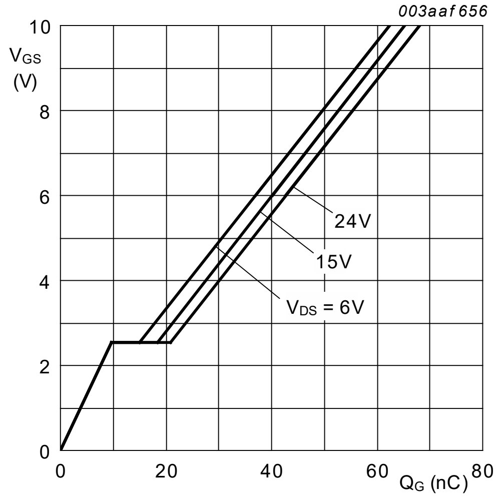
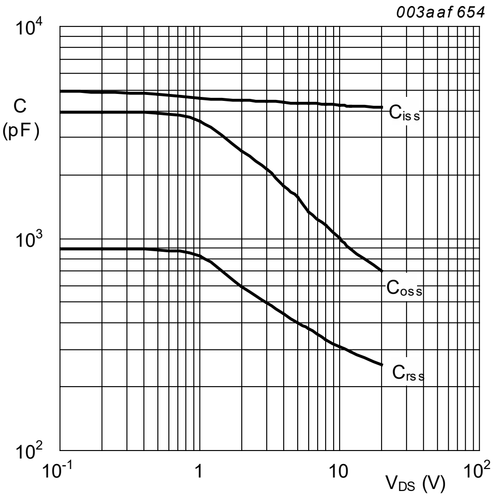


Fig. 14. Gate charge waveform definitions



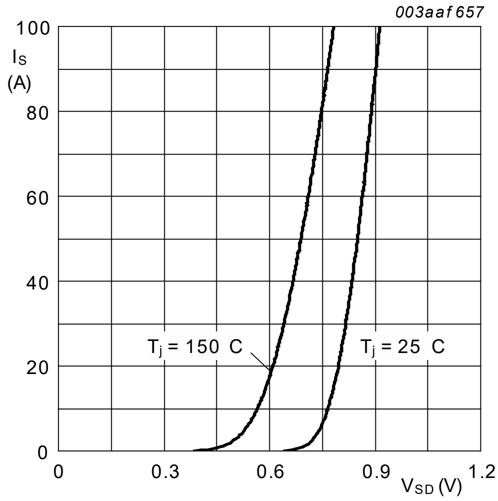
$T_j = 25°C; I_D = 25A$

Fig. 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig. 17. Source current as a function of source-drain voltage; typical values

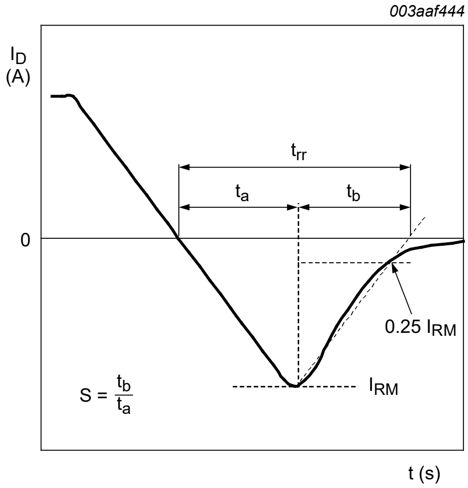
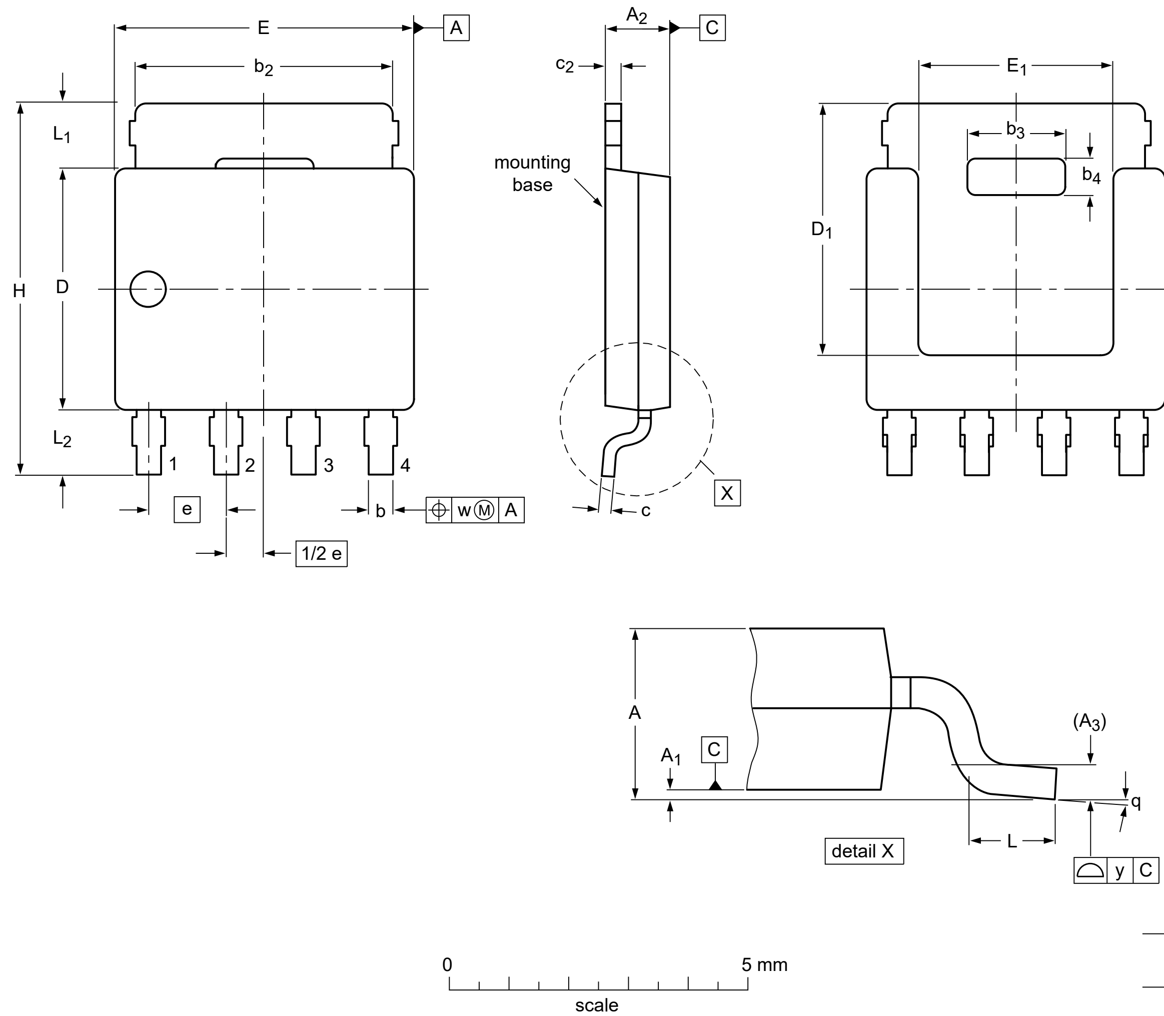


Fig. 18. Reverse recovery waveform definitions

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A1	A2	A3	b	b2	b3	b4	c	c2	D(1)	D1(1)	E(1)	E1(1)	e	H	L	L1	L2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 19. Package outline LFPAK56; Power-SO8 (SOT669)

12. Soldering

Footprint information for reflow soldering **SOT669**

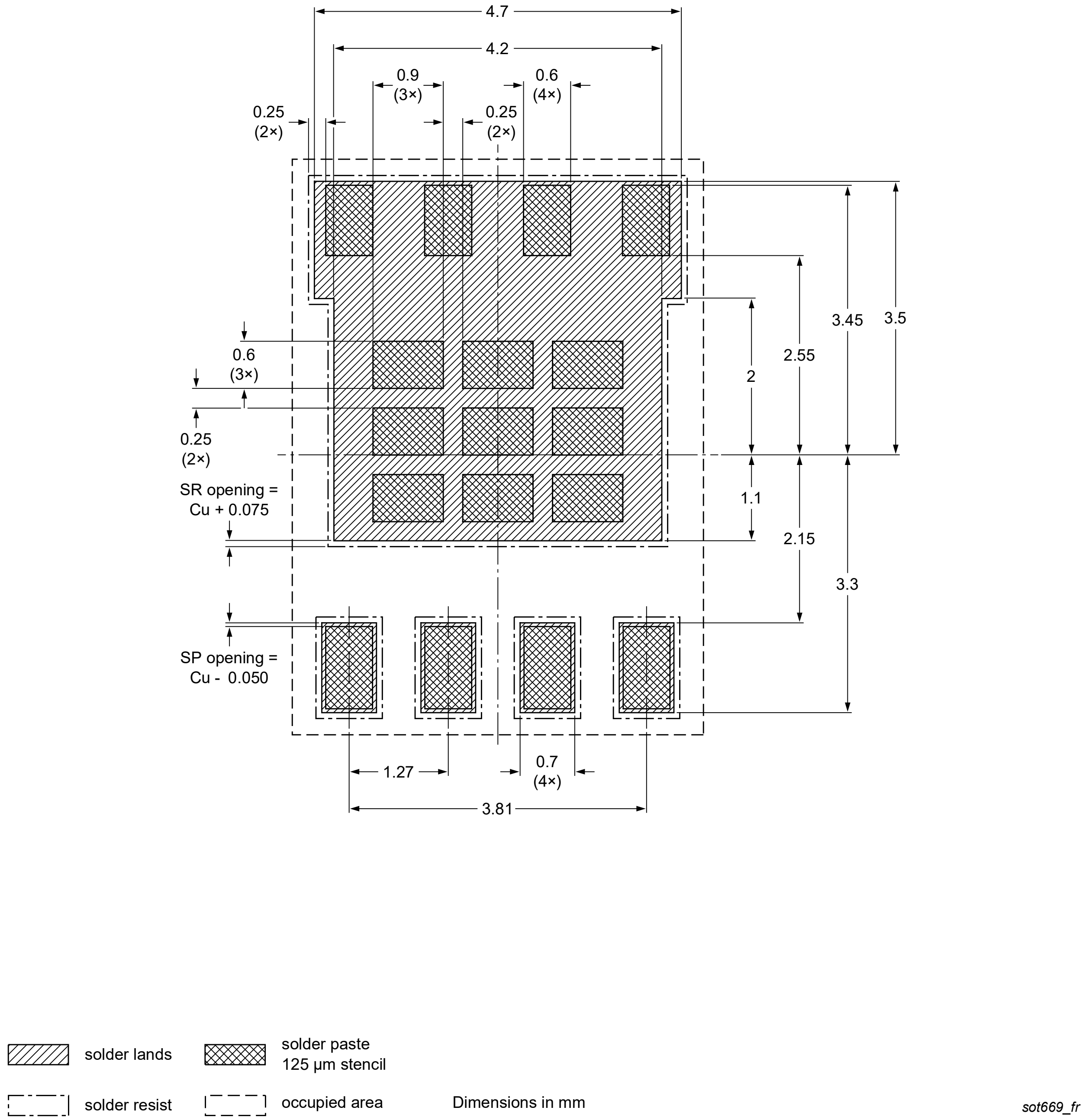
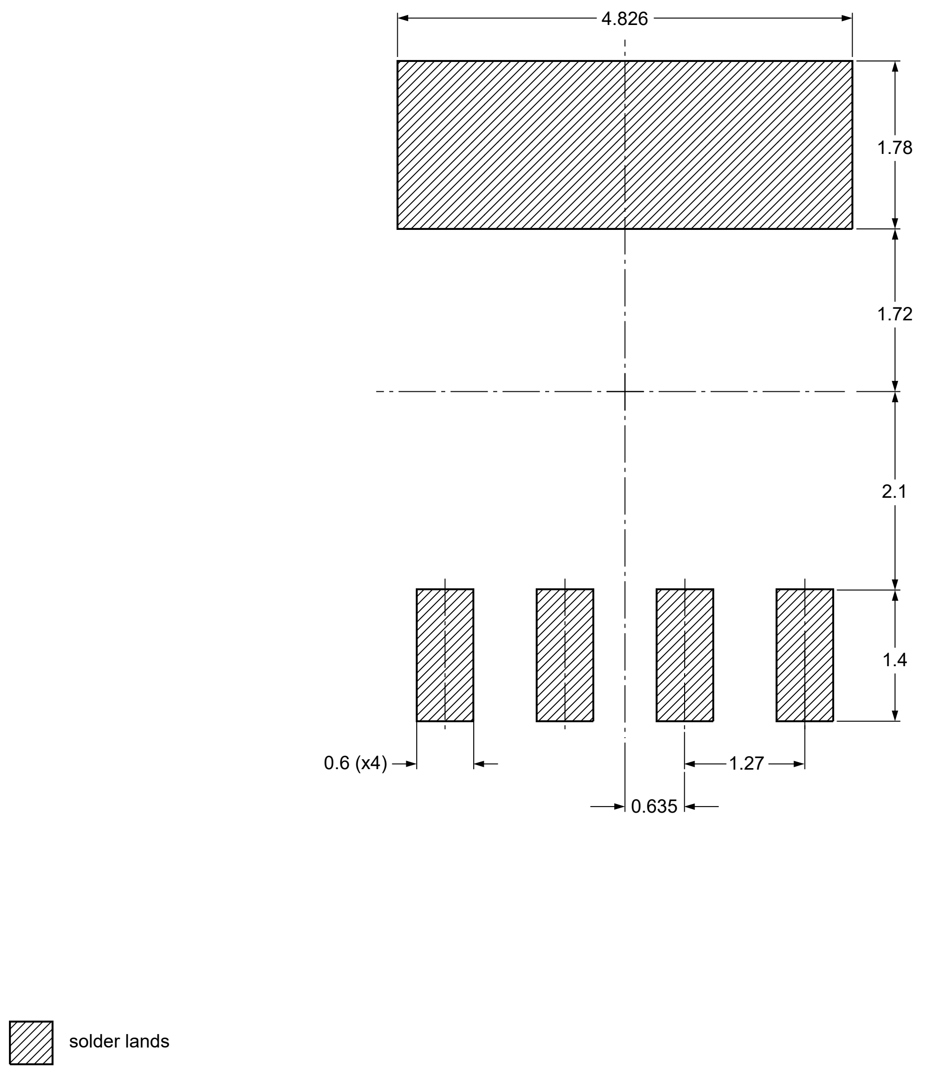


Fig. 20. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**



Dimensions in mm

Issue date ~~15-04-13~~ 15-04-16

sot669_fw

Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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