



PDTD114EU

50 V, 500 mA NPN resistor-equipped transistor

5 March 2024

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTB114EU

2. Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- $\pm 10\%$ resistor ratio tolerance
- High temperature applications up to 175 °C
- AEC-Q101 qualified

3. Applications

- Controlling IC inputs
- Cost-saving alternative to BC817 series in digital applications
- Switching loads

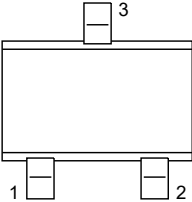
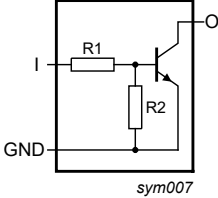
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CE0}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	500	mA
R1	bias resistor 1 (input)		7	10	13	k Ω
R2/R1	bias resistor ratio		0.9	1	1.1	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SC-70 (SOT323)	 sym007
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTD114EU	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTD114EU	ZV%

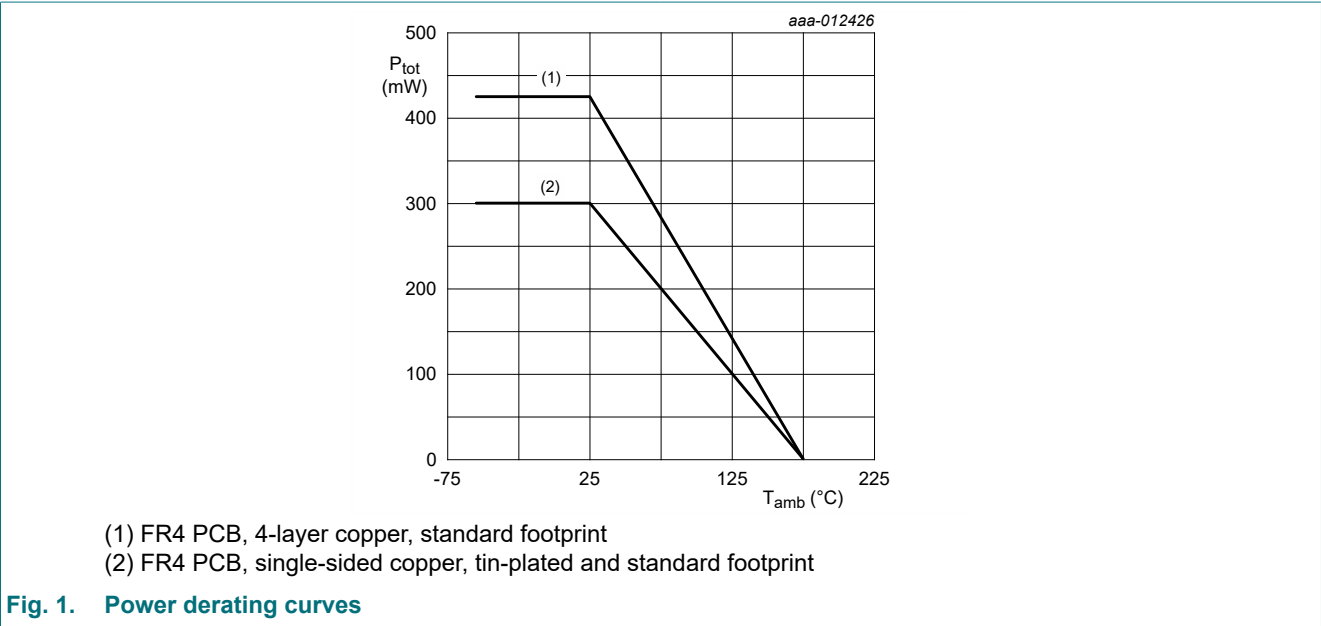
[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage			-10	50	V
I _O	output current			-	500	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
			[2]	-	425	mW
T _j	junction temperature			-	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-55	175	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

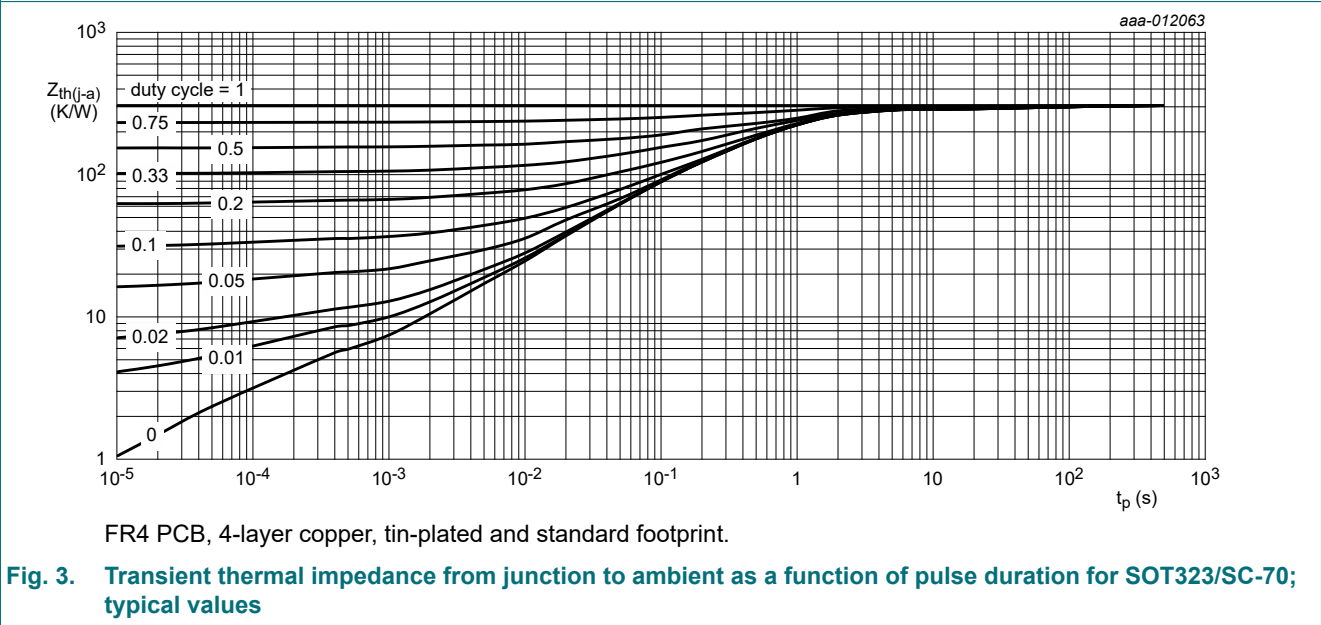
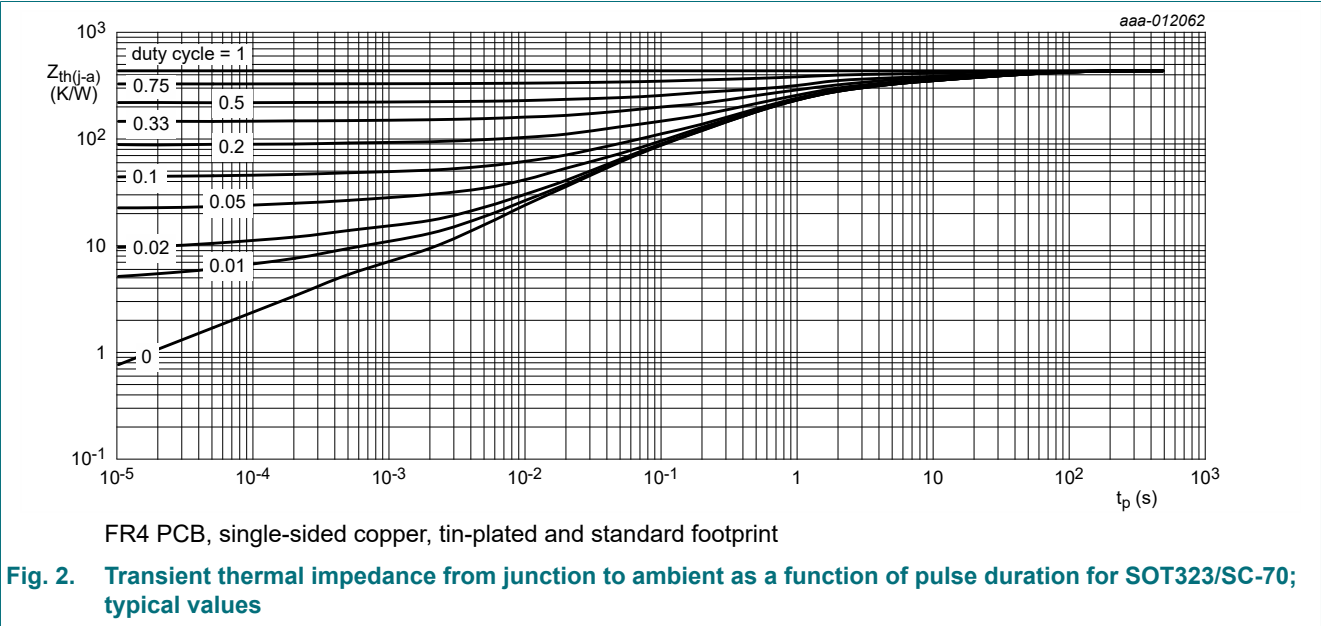


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W
			[2]	-	-	353	K/W

- [1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

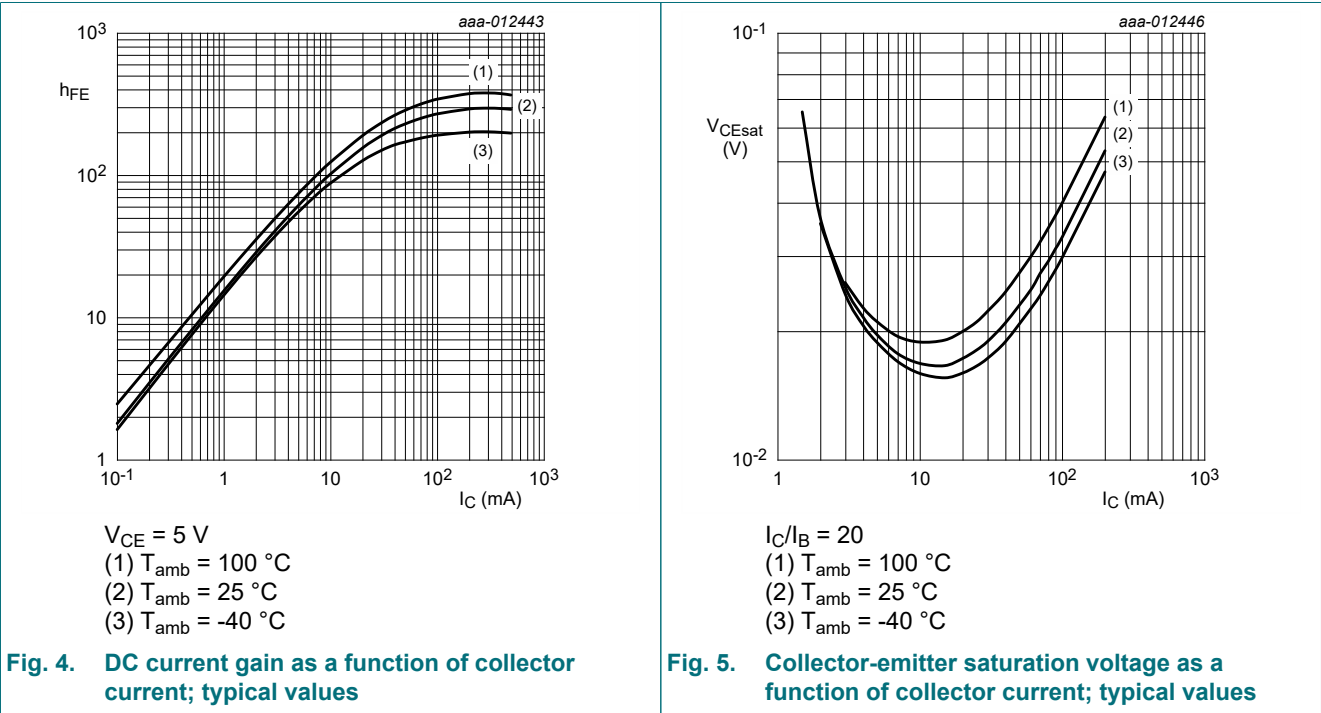


10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = 40 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
		V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 50 V; I _B = 0 A; T _{amb} = 25 °C	-	-	0.5	µA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	0.4	mA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 50 mA; T _{amb} = 25 °C	70	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 50 mA; I _B = 2.5 mA; T _{amb} = 25 °C	-	-	100	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 µA; T _{amb} = 25 °C	0.6	1	1.5	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 20 mA; T _{amb} = 25 °C	1	1.9	3	V
R1	bias resistor 1 (input)		7	10	13	kΩ
R2/R1	bias resistor ratio		0.9	1	1.1	
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	7	-	pF
f _T	transition frequency	V _{CE} = 5 V; I _C = 50 mA; f = 100 MHz; T _{amb} = 25 °C	[1]	225	-	MHz

[1] Characteristics of built-in transistor.



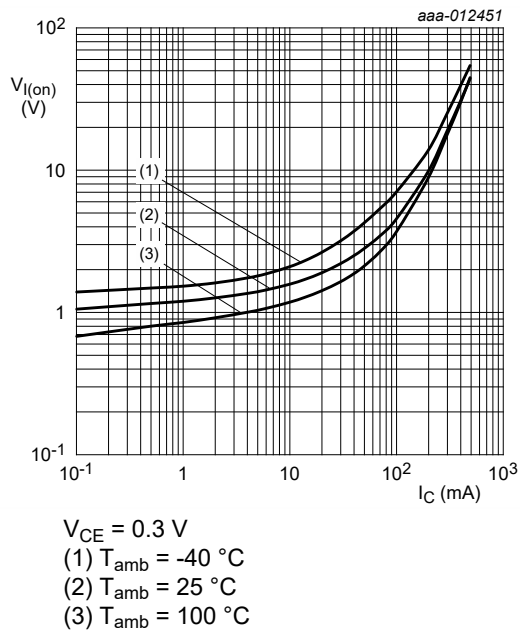


Fig. 6. On-state input voltage as a function of collector current; typical values

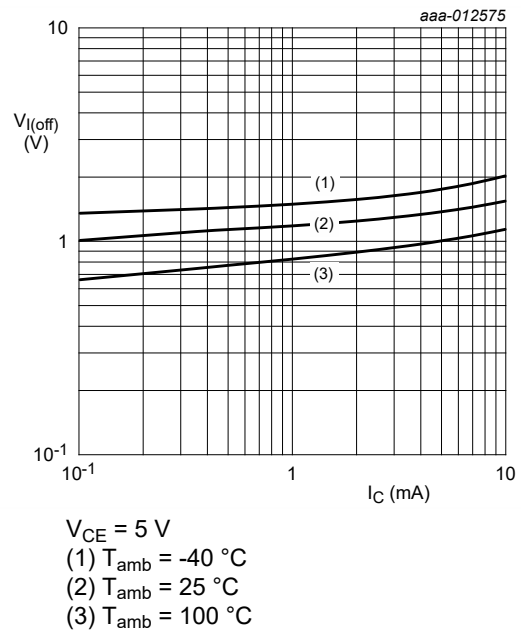


Fig. 7. Off-state input voltage as a function of collector current; typical values

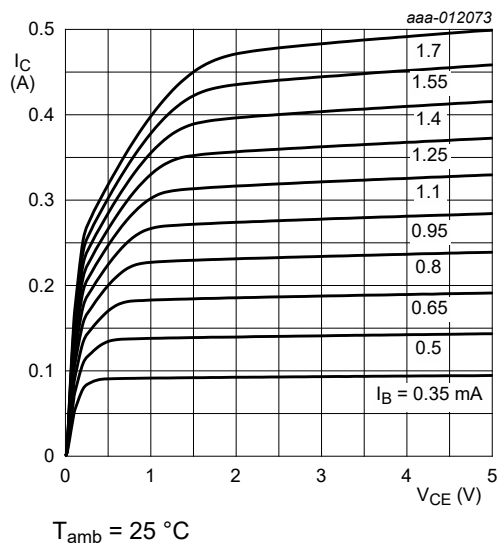


Fig. 8. Collector current as a function of collector-emitter voltage; typical values

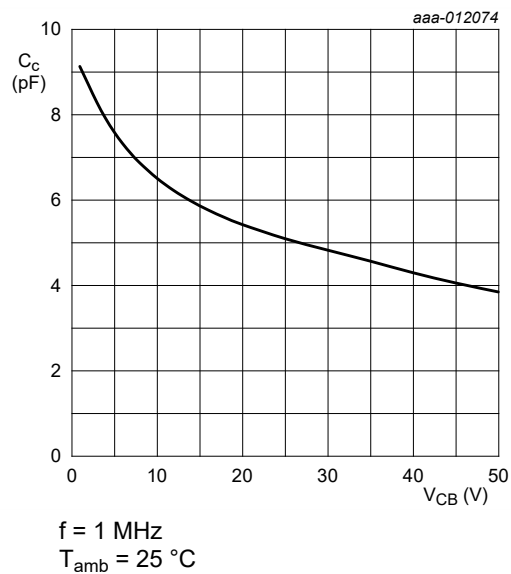
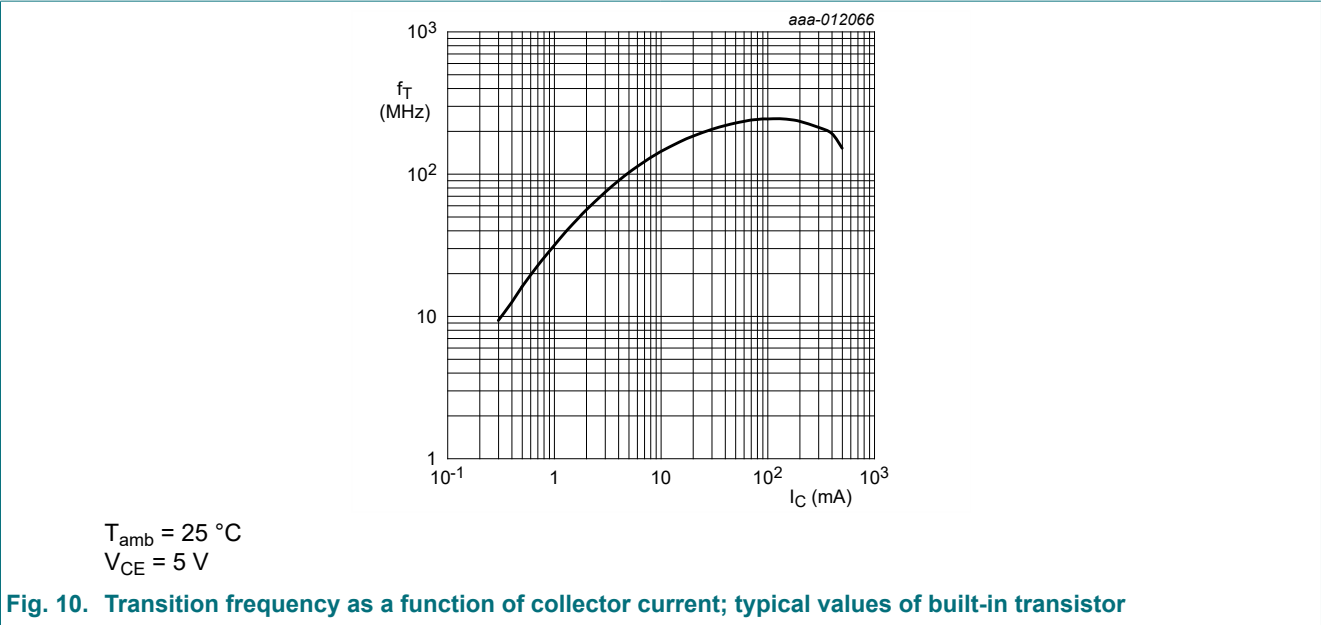


Fig. 9. Collector capacitance as a function of collector-base voltage; typical values

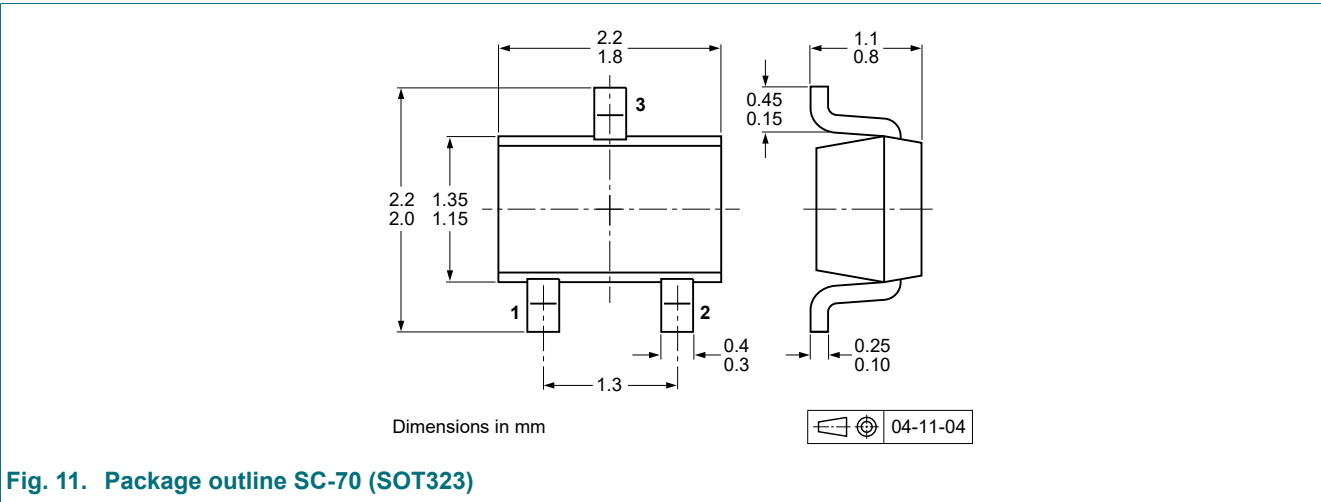


11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering

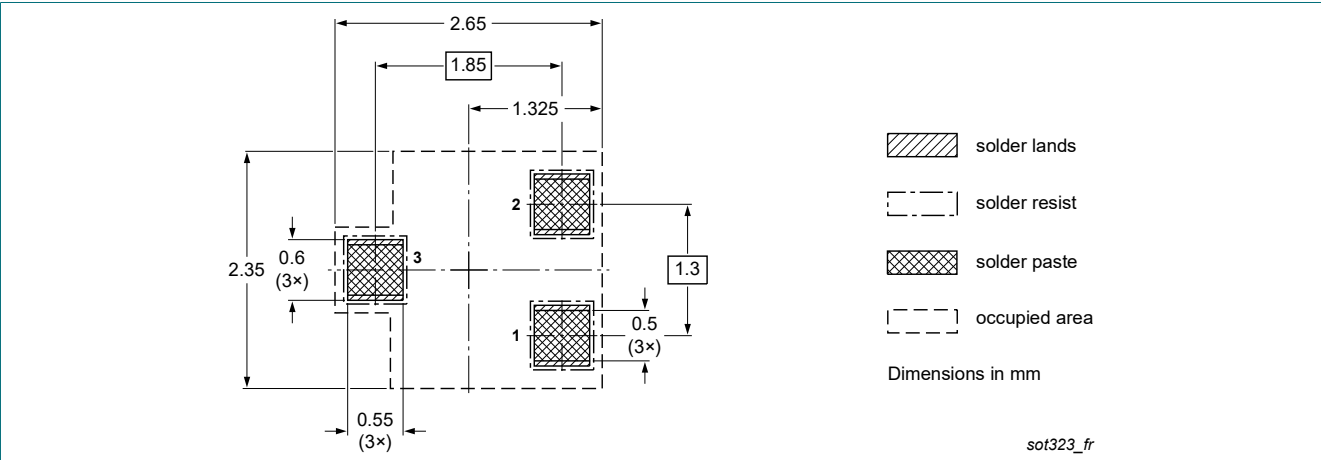


Fig. 12. Reflow soldering footprint for SC-70 (SOT323)

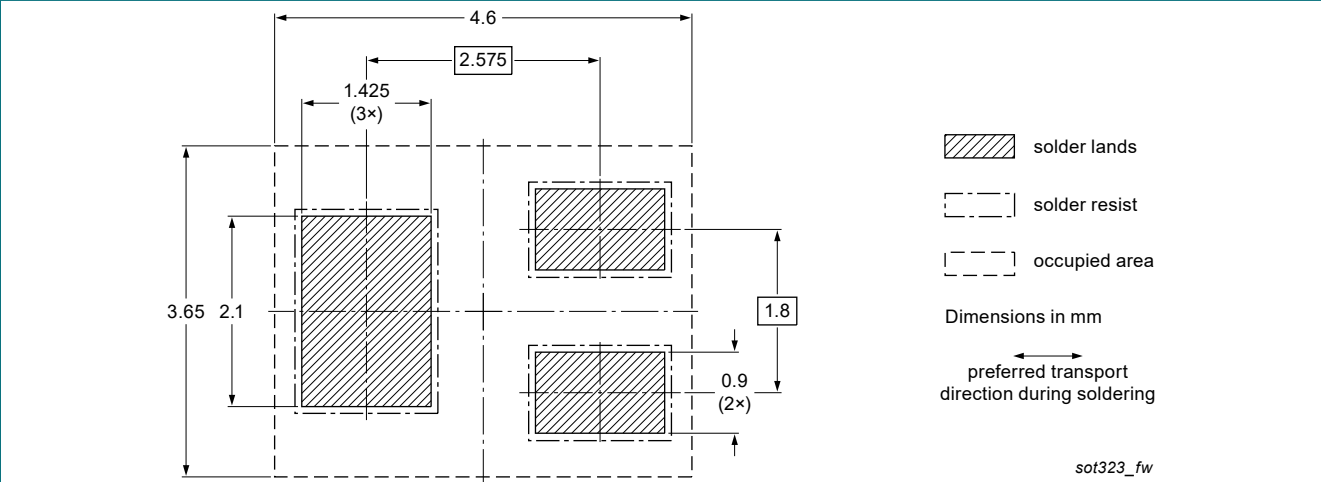


Fig. 13. Wave soldering footprint for SC-70 (SOT323)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTD114EU v.2	20240305	Product data sheet	-	PDTD1XXXU_SER v.1
Modifications:	• Family data sheet reduced to single type data sheet.			
PDTD1XXXU_SER v.1	20140513	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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