



PBSS4112PAN

120 V, 1 A NPN/NPN low V_{CEsat} (BISS) transistor

29 November 2012

Product data sheet

1. Product profile

1.1 General description

NPN/NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package. NPN/PNP complement: PBSS4112PANP. PNP/PNP complement: PBSS5112PAP.

1.2 Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- High energy efficiency due to less heat generation
- AEC-Q101 qualified

1.3 Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

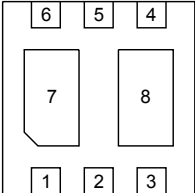
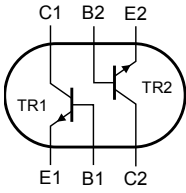
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	120	V
I_C	collector current		-	-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1.5	A
Per transistor						
R_{CEsat}	collector-emitter saturation resistance	$I_C = 500$ mA; $I_B = 50$ mA; pulsed; $t_p \leq 300$ μ s; $\delta \leq 0.02$; $T_{amb} = 25$ °C	-	-	240	m Ω

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 Transparent top view DFN2020-6 (SOT1118)	 sym140
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4112PAN	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

4. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4112PAN	2R

5. Limiting values

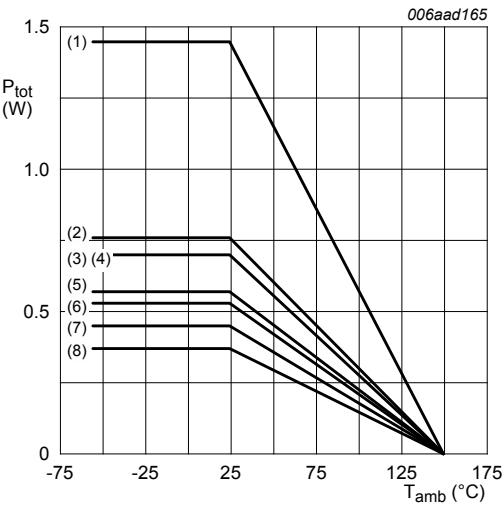
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor					
V _{CBO}	collector-base voltage	open emitter	-	120	V
V _{CEO}	collector-emitter voltage	open base	-	120	V
V _{EBO}	emitter-base voltage	open collector	-	7	V
I _C	collector current		-	1	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	1.5	A
I _B	base current		-	0.3	A

Symbol	Parameter	Conditions		Min	Max	Unit
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
 [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
 [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
 [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
 [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
 [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
 [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
 [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm²
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm²
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm²
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm²
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

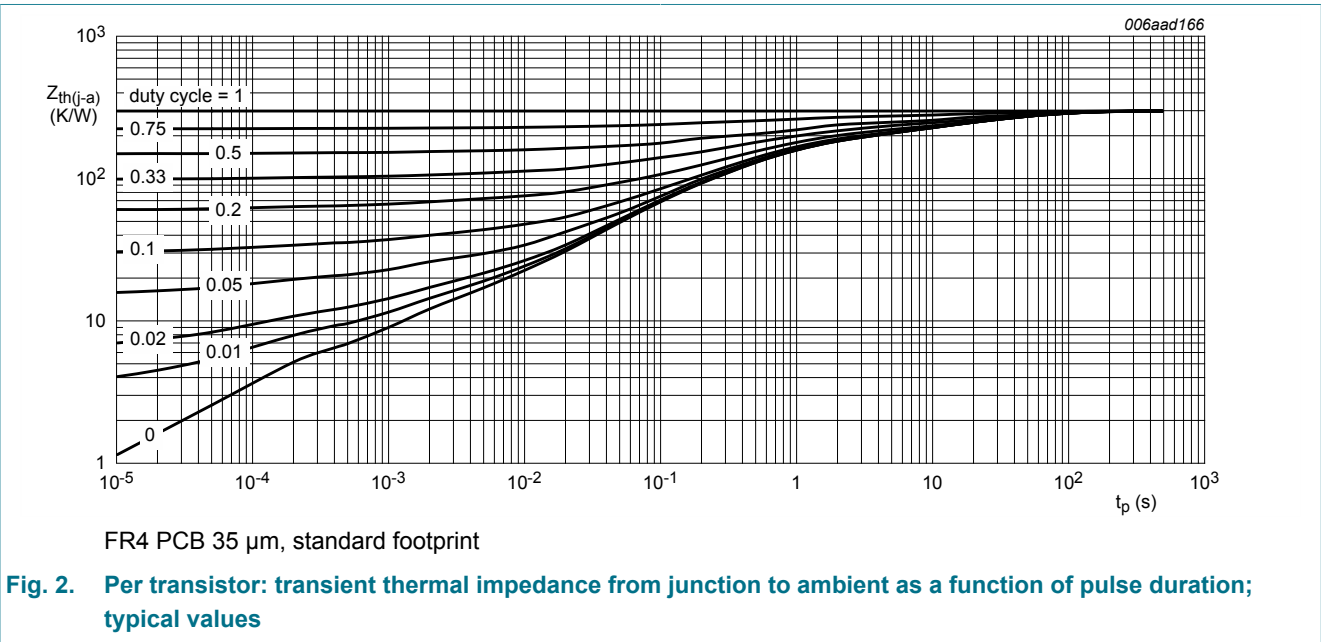
6. Thermal characteristics

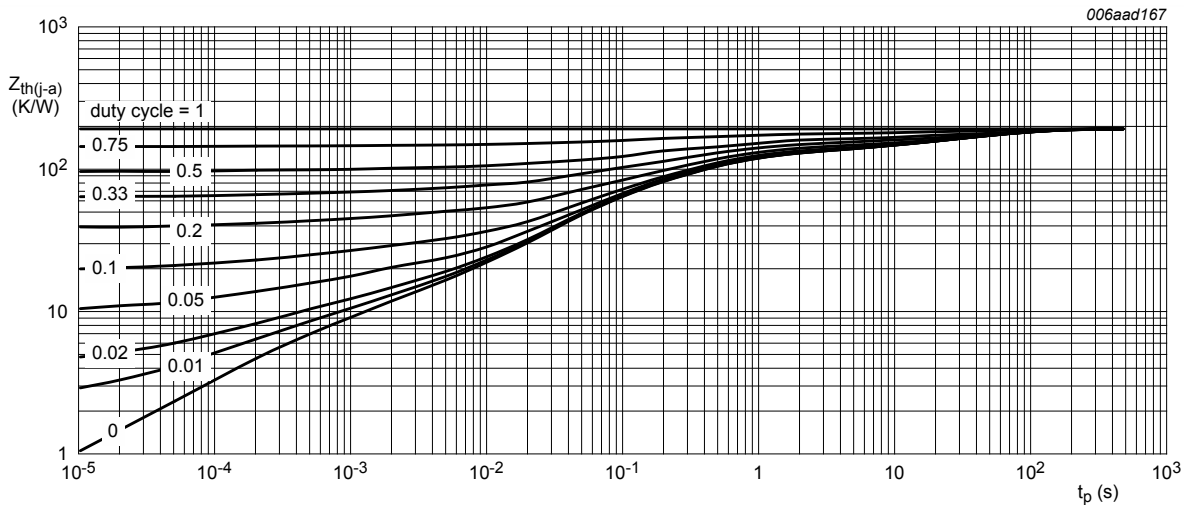
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	-	30	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

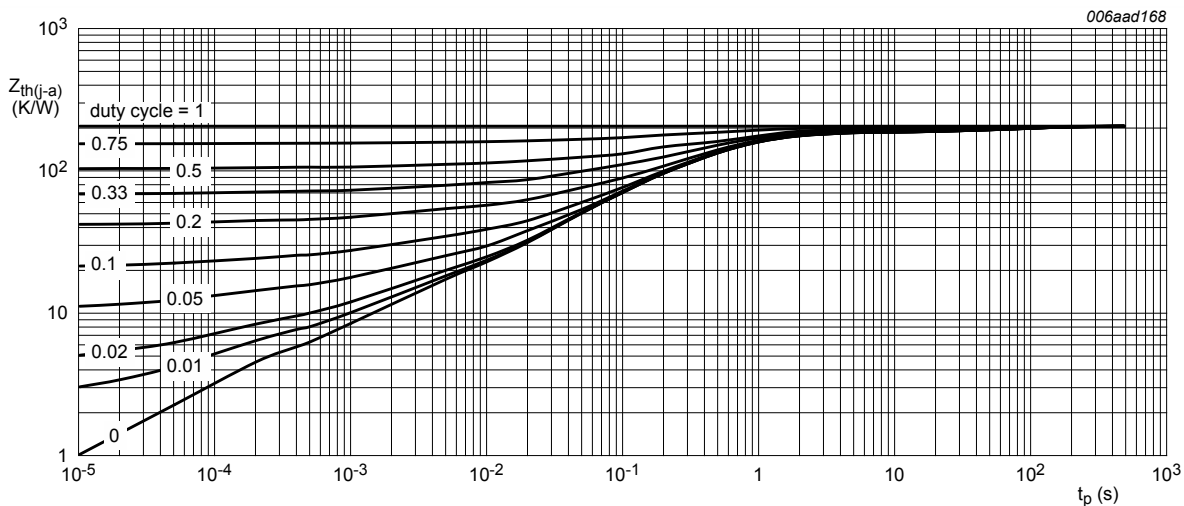
- [1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm².





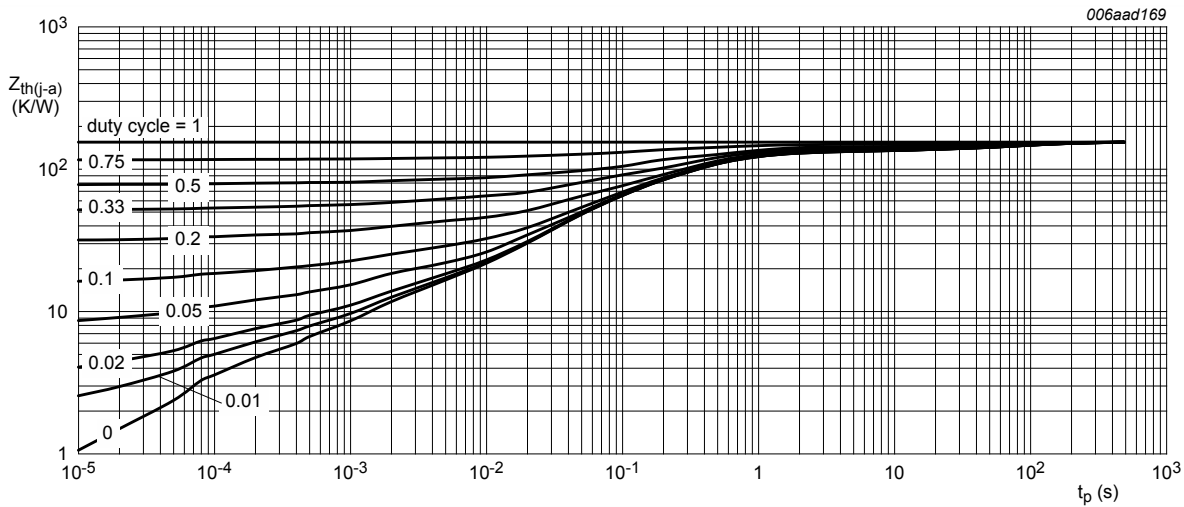
FR4 PCB 35 μ m, mounting pad for collector 1 cm²

Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



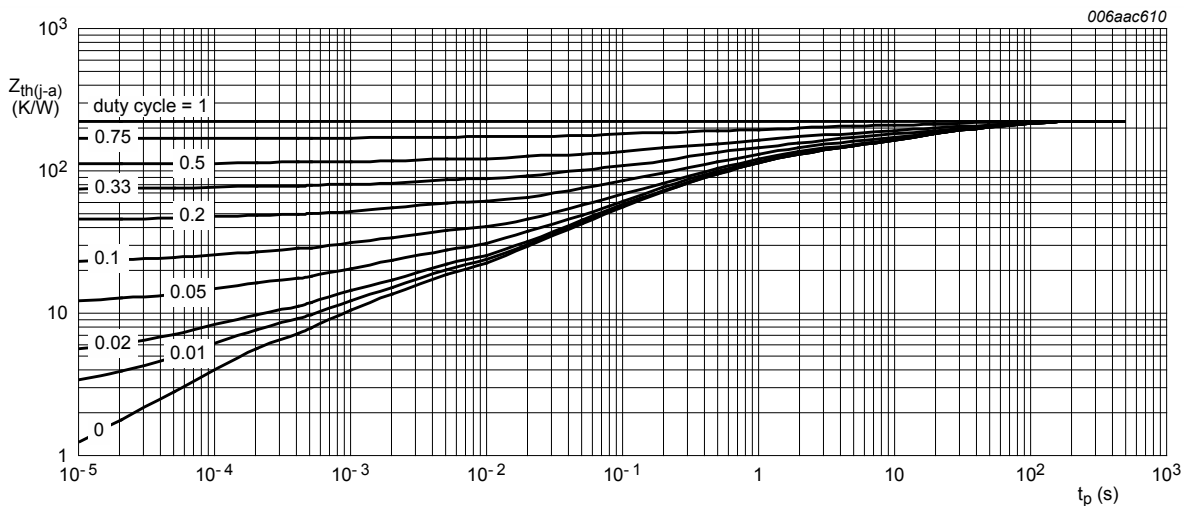
4-layer PCB 35 μ m, standard footprint

Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



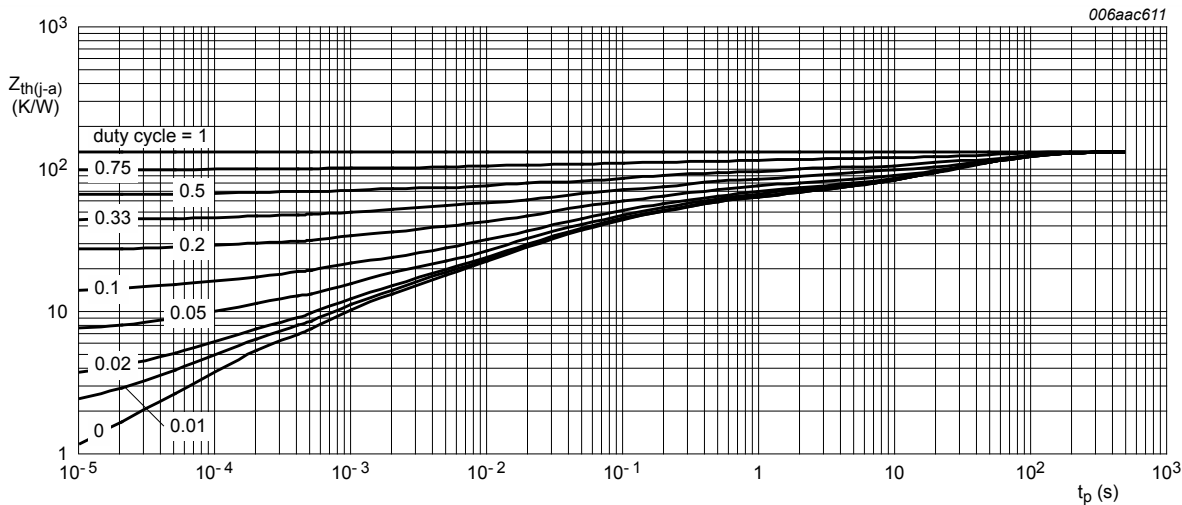
4-layer PCB 35 μm , mounting pad for collector 1 cm^2

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



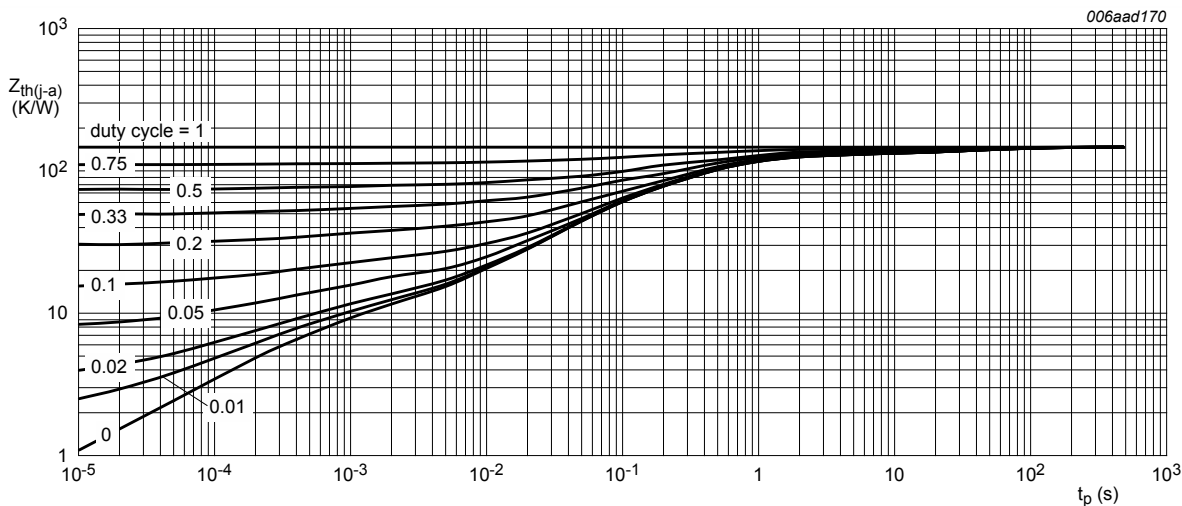
FR4 PCB 70 μm , standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB 70 μm , mounting pad for collector 1 cm^2

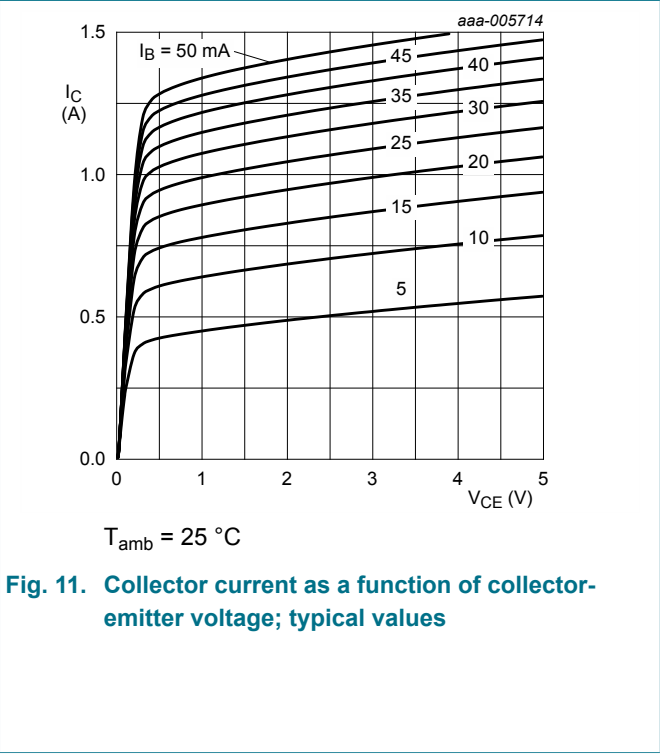
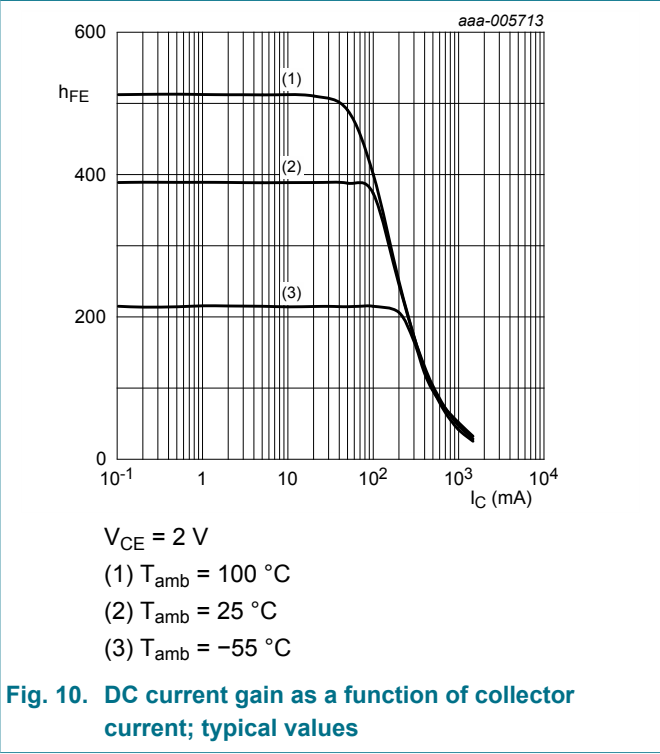
Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 μm , standard footprint

Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BEsat}	base-emitter saturation voltage	I _C = 500 mA; I _B = 50 mA; T _{amb} = 25 °C	-	-	1	V
		I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	1.1	V
		I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = 2 V; I _C = 0.5 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	0.9	V
t _d	delay time	V _{CC} = 10 V; I _C = 500 mA; I _{Bon} = 25 mA; I _{Boff} = -25 mA; T _{amb} = 25 °C	-	20	-	ns
t _r	rise time		-	440	-	ns
t _{on}	turn-on time		-	460	-	ns
t _s	storage time		-	615	-	ns
t _f	fall time		-	390	-	ns
t _{off}	turn-off time		-	1005	-	ns
f _T	transition frequency	V _{CE} = 10 V; I _C = 50 mA; f = 100 MHz; T _{amb} = 25 °C	60	120	-	MHz
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	4.5	7	pF



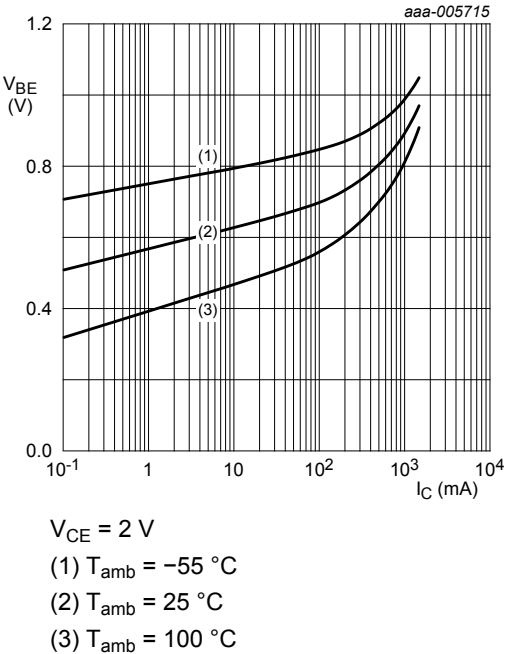


Fig. 12. Base-emitter voltage as a function of collector current; typical values

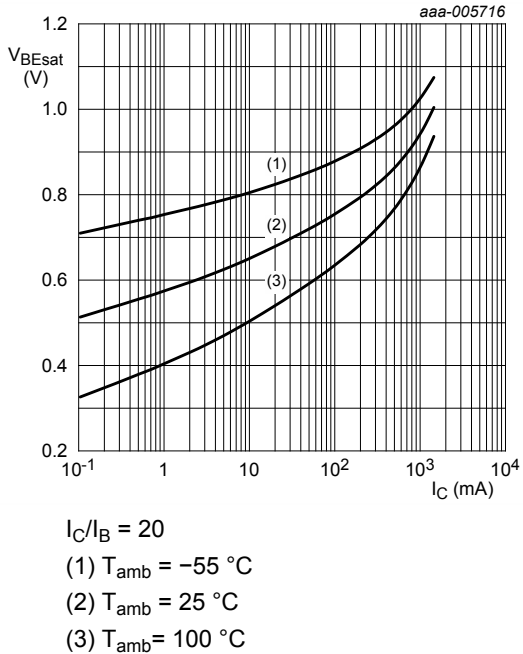


Fig. 13. Base-emitter saturation voltage as a function of collector current; typical values

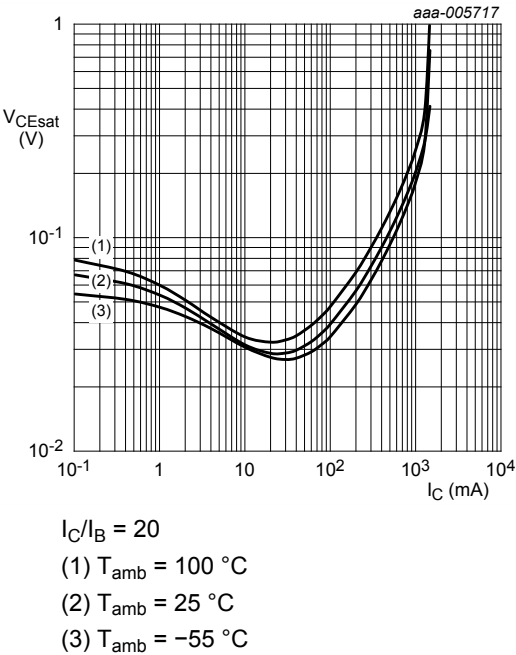


Fig. 14. Collector-emitter saturation voltage as a function of collector current; typical values

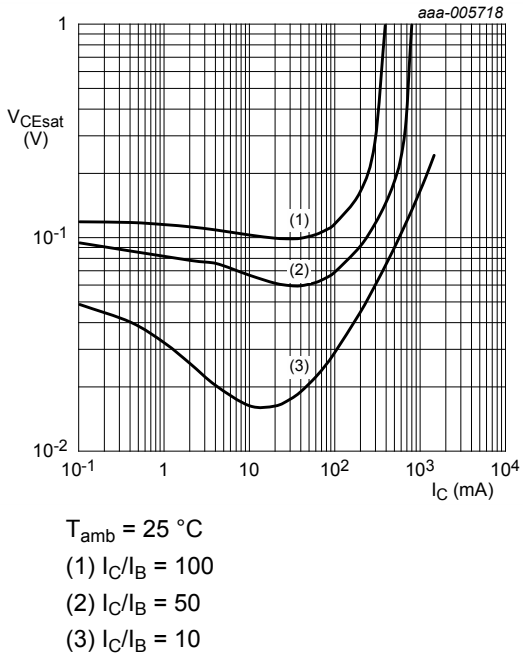
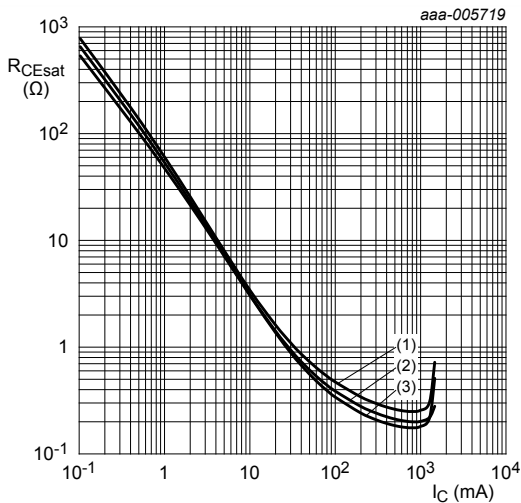
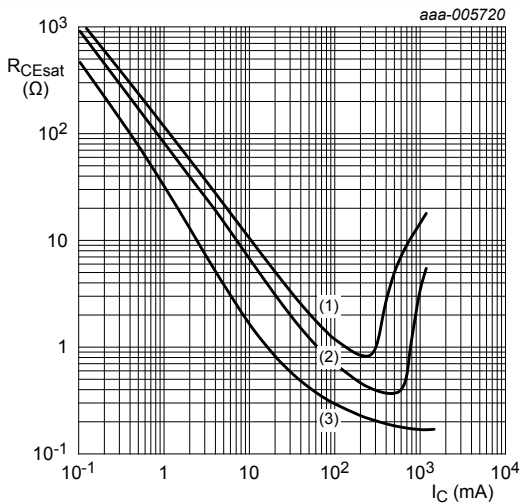


Fig. 15. Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
(1) $T_{amb} = 100^\circ C$
(2) $T_{amb} = 25^\circ C$
(3) $T_{amb} = -55^\circ C$

Fig. 16. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25^\circ C$
(1) $I_C/I_B = 100$
(2) $I_C/I_B = 50$
(3) $I_C/I_B = 10$

Fig. 17. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

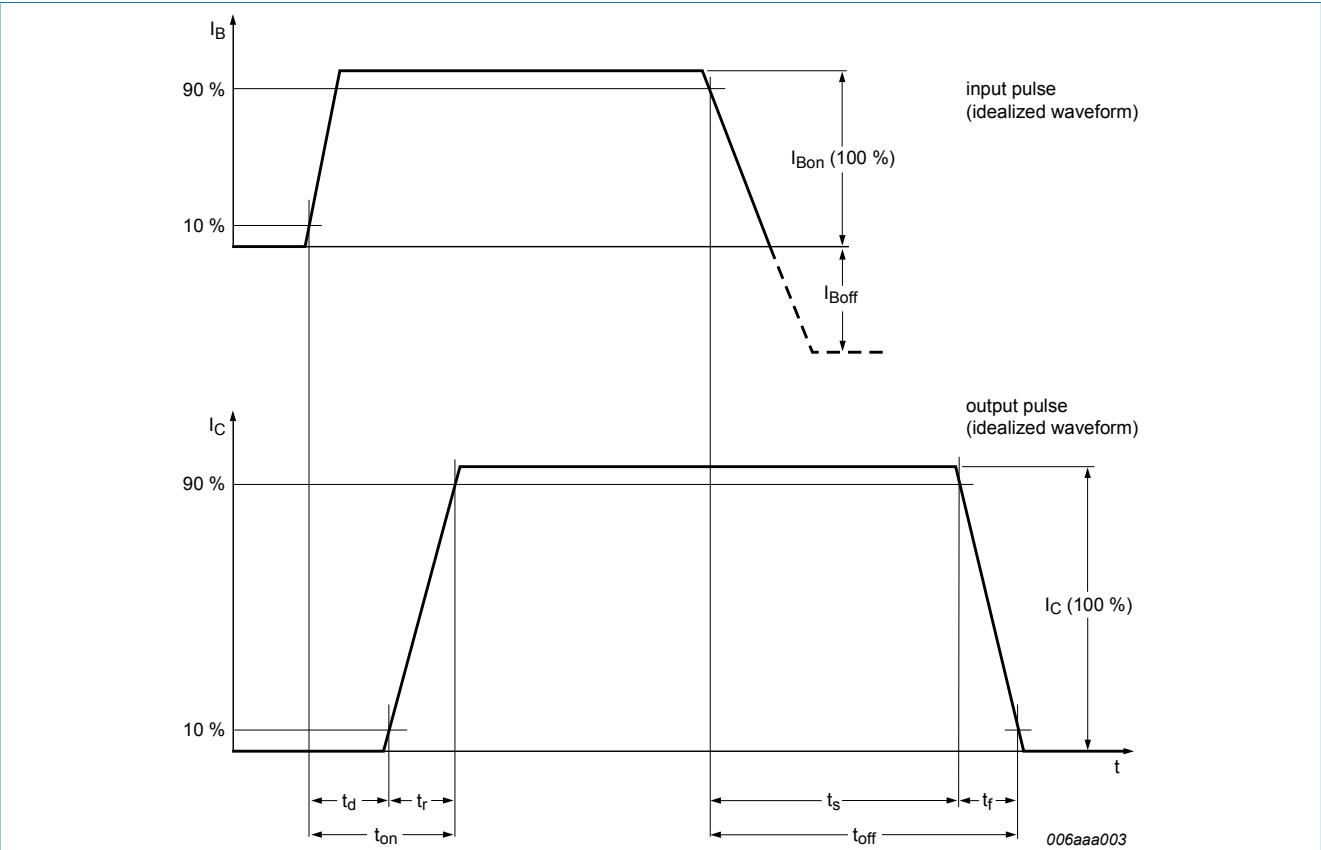


Fig. 18. BISS transistor switching time definition

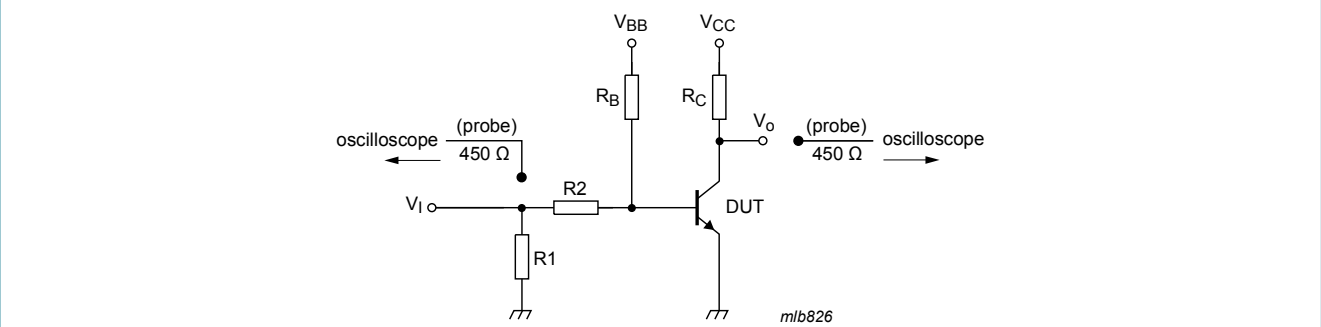
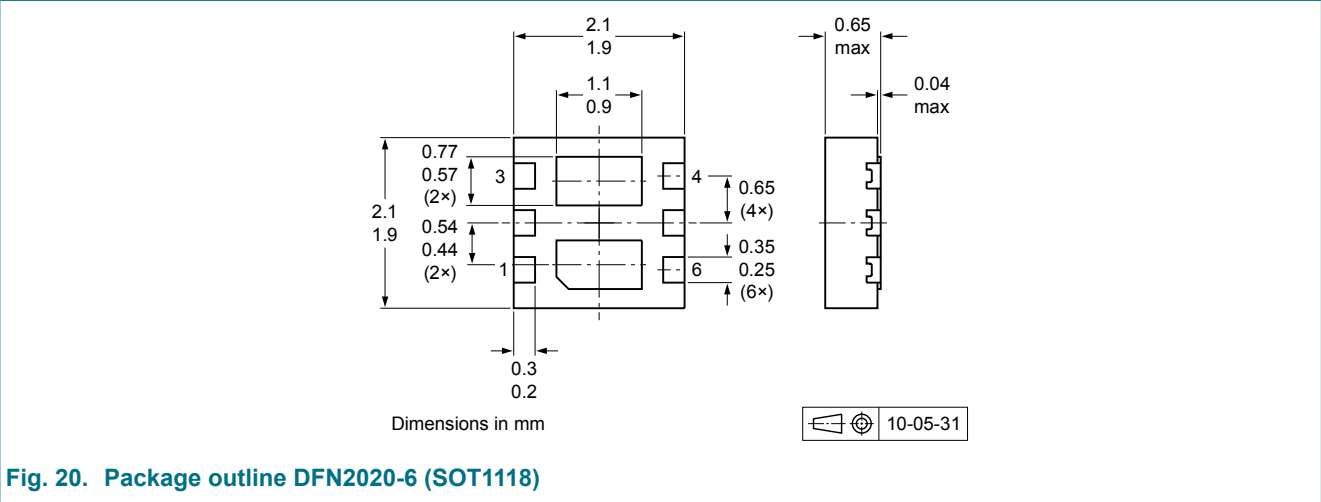


Fig. 19. Test circuit for switching times

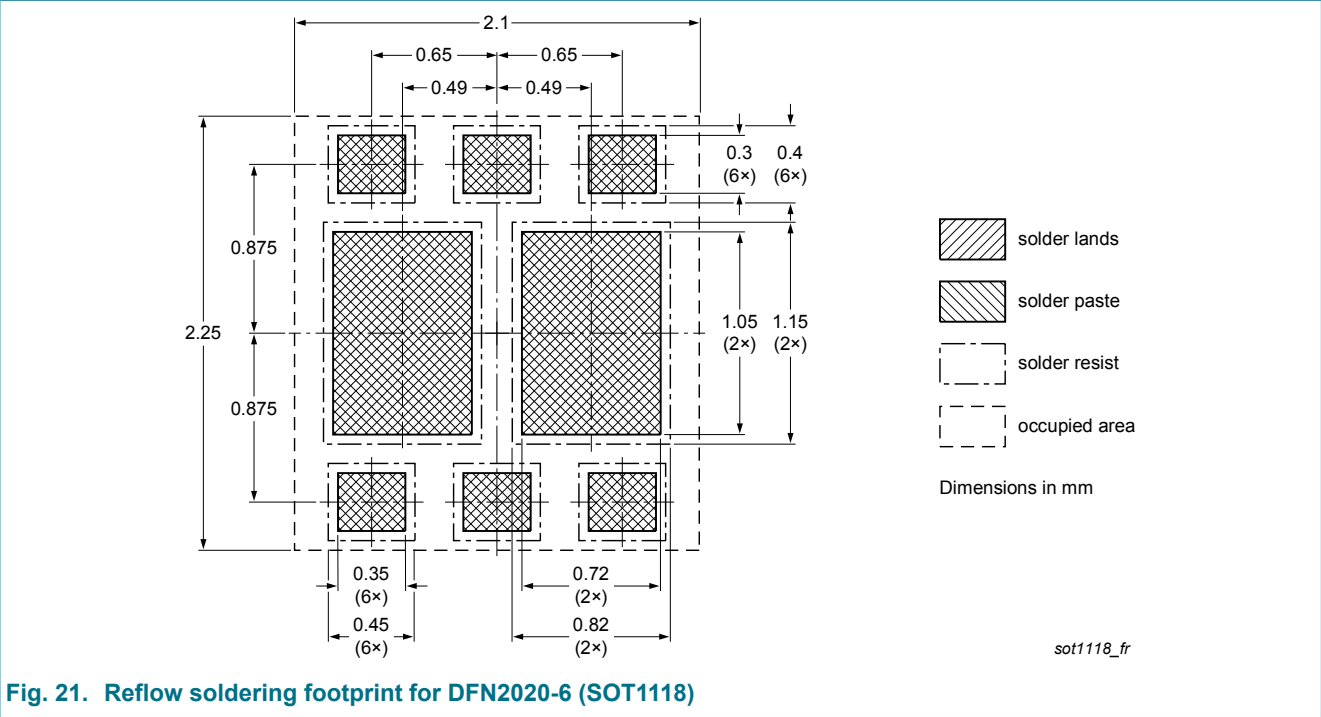
8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

9. Package outline



10. Soldering



11. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4112PAN v.N	20121129	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 29 November 2012

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