



# BUK7K18-40E

Dual N-channel 40 V, 19 mΩ standard level MOSFET

10 December 2013

Product data sheet

## 1. General description

Dual standard level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  of greater than 1 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

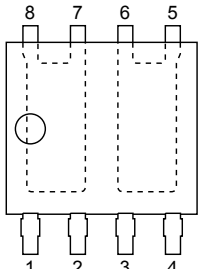
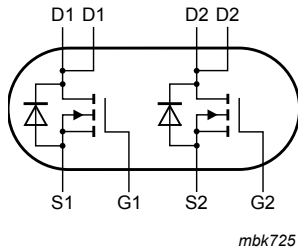
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	24.2	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	38	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	15.5	19	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	4.3	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K18-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K18-40E	71840E

## 8. Limiting values

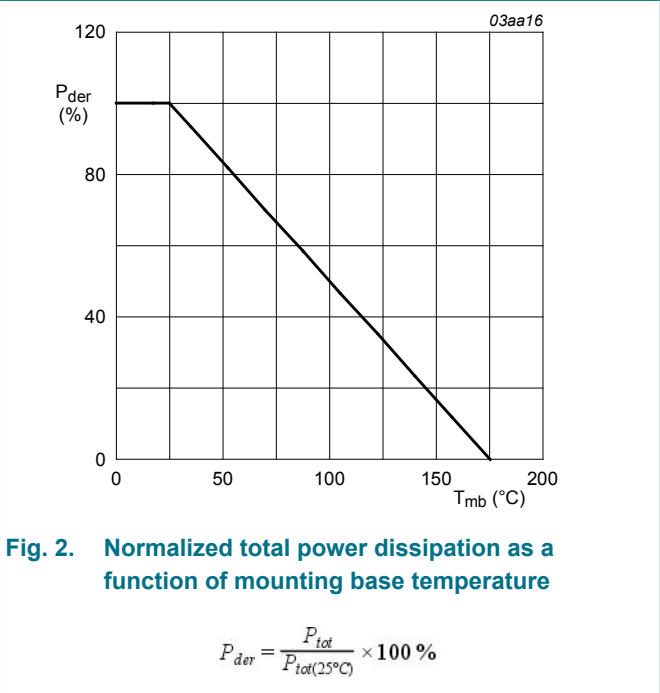
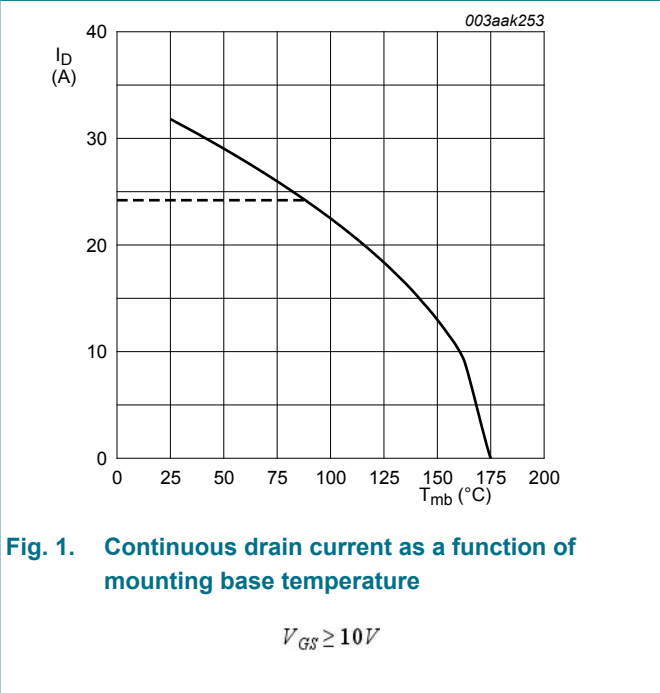
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-20	20	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; Fig. 1	-	24.2	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; Fig. 1	-	22	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	127	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 2	-	38	W

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	24.2	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	127	A
Avalanche Ruggedness FET1 and FET2						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 24.2 A; V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; Fig. 3	[1][2]	-	26.3	mJ

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



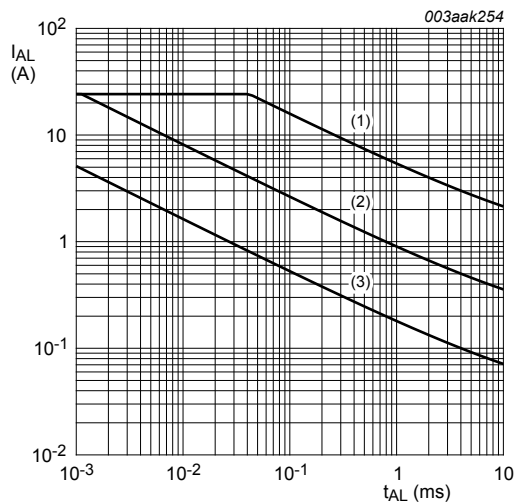


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 150^{\circ}C$ ; (3) Repetitive Avalanche

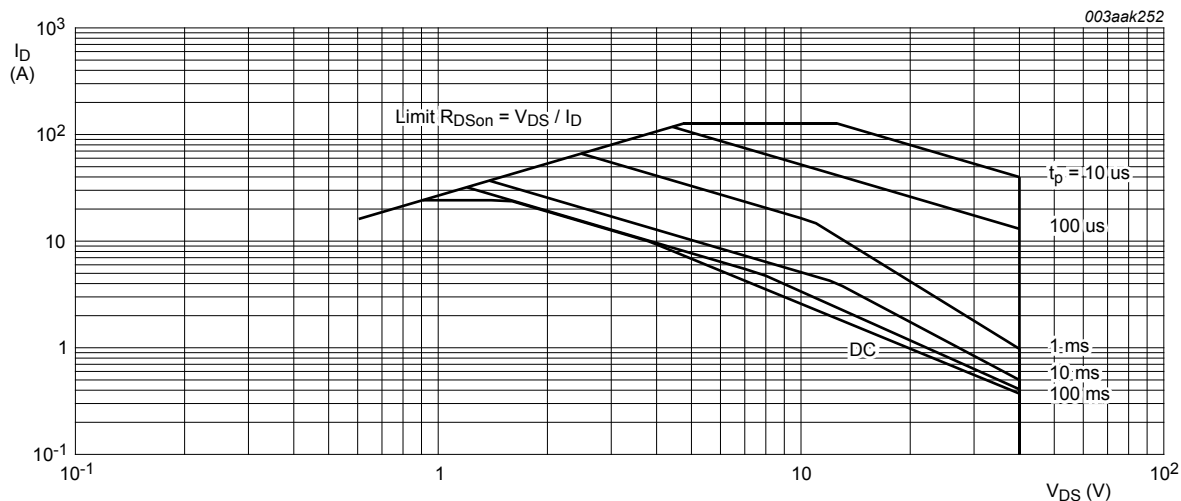


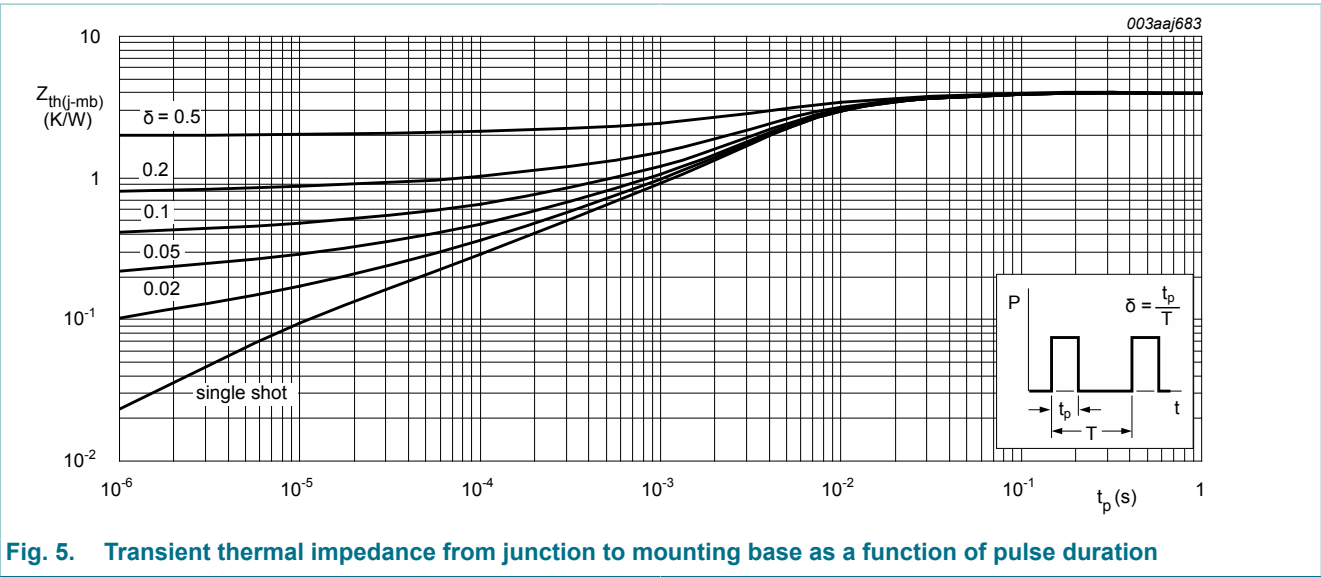
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	3.96	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C		36	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C		40	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		2.4	3	4	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 175 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		1	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = -55 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		-	-	4.5	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	0.02	1	μA
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 175 °C		-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	2	100	nA
		V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>		-	15.5	19	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>		-	30.5	37.4	mΩ
Dynamic characteristics FET1 and FET2							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	11.8	-	nC
Q <sub>GS</sub>	gate-source charge			-	3.6	-	nC
Q <sub>GD</sub>	gate-drain charge			-	4.3	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>		-	606	808	pF
C <sub>oss</sub>	output capacitance			-	134	161	pF
C <sub>rss</sub>	reverse transfer capacitance			-	87	119	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 32 V; R <sub>L</sub> = 3.3 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C; I <sub>D</sub> = 10 A		-	6.2	-	ns
t <sub>r</sub>	rise time			-	12.7	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	7.9	-	ns
t <sub>f</sub>	fall time			-	10	-	ns
Source-drain diode FET1 and FET2							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>		-	0.83	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C		-	16.8	-	ns
Q <sub>r</sub>	recovered charge			-	9.1	-	nC

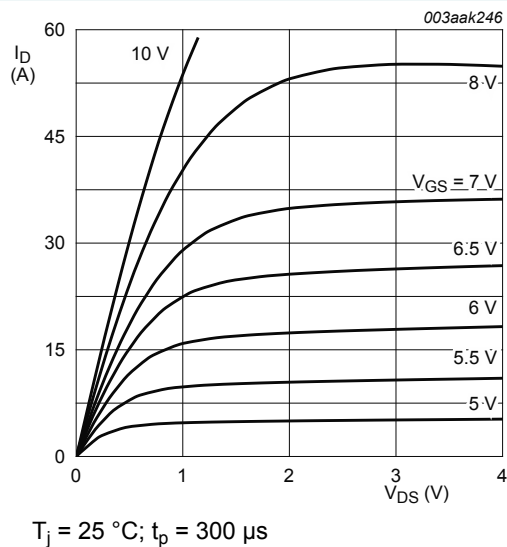


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

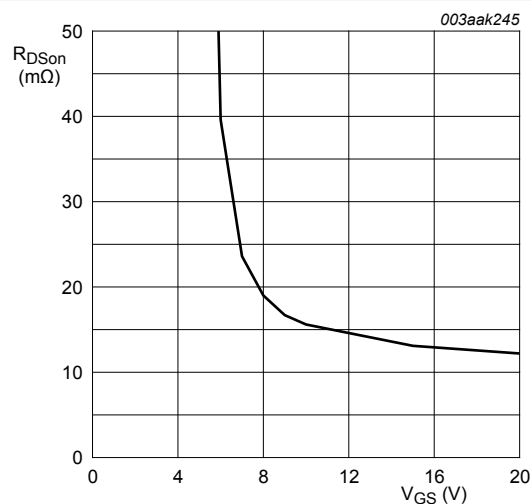


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

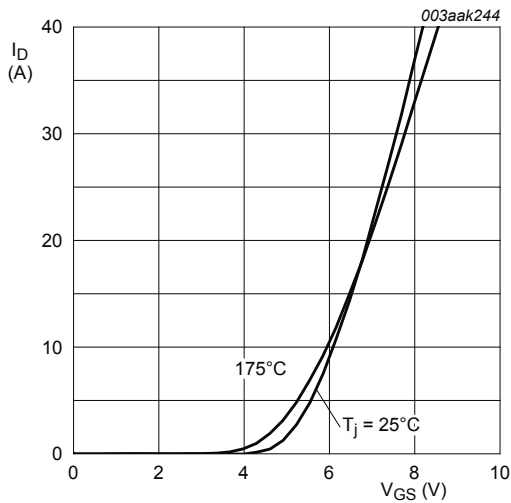


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

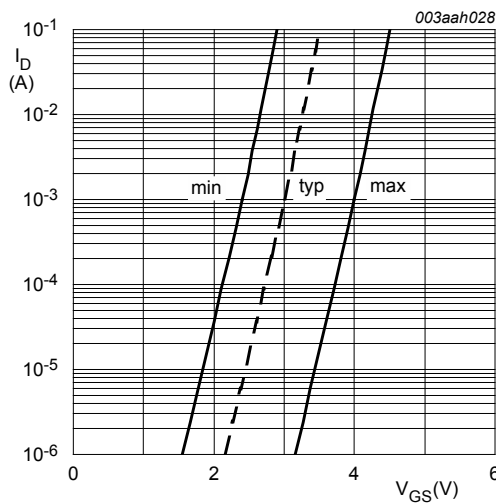


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ C; V_{DS} = 5V$

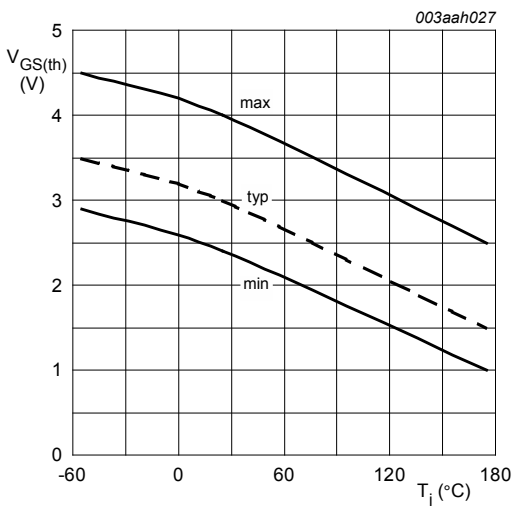


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

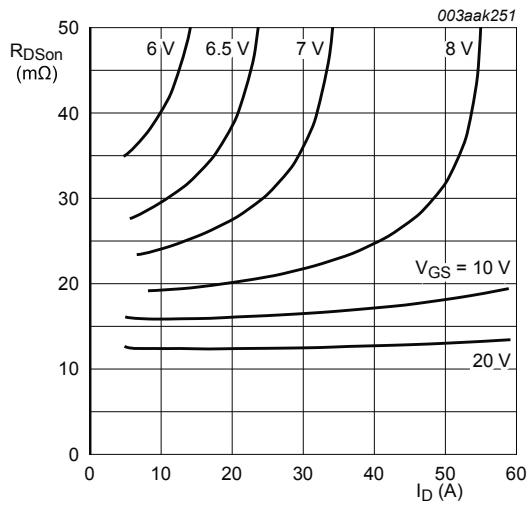


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ C; t_p = 300\text{ }\mu s$

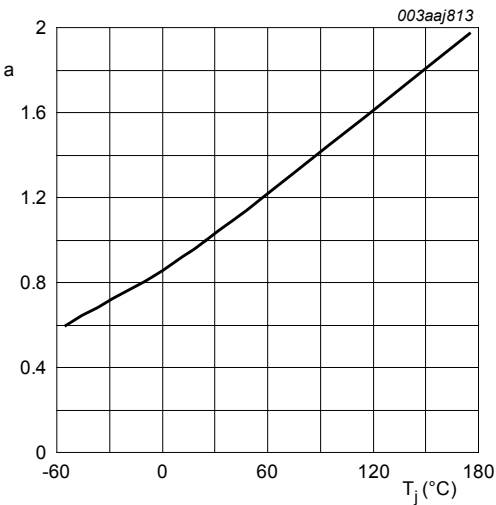


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

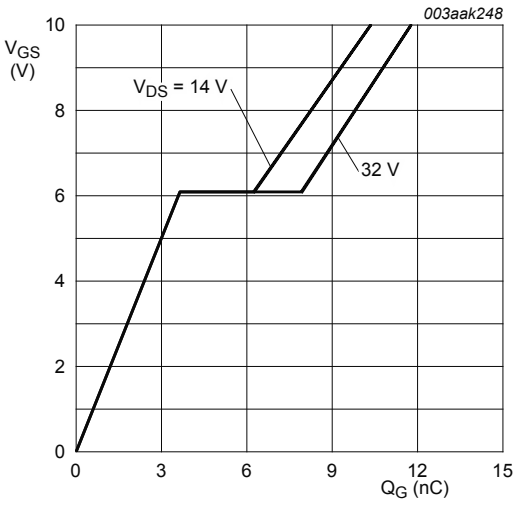


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$$

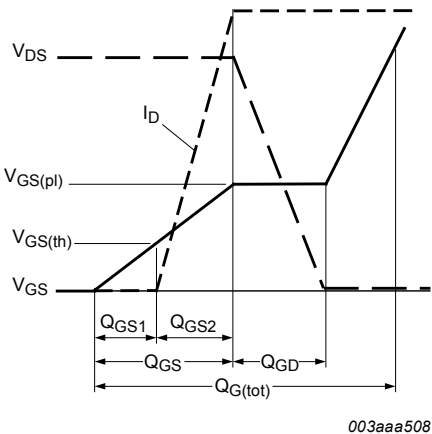


Fig. 14. Gate charge waveform definitions

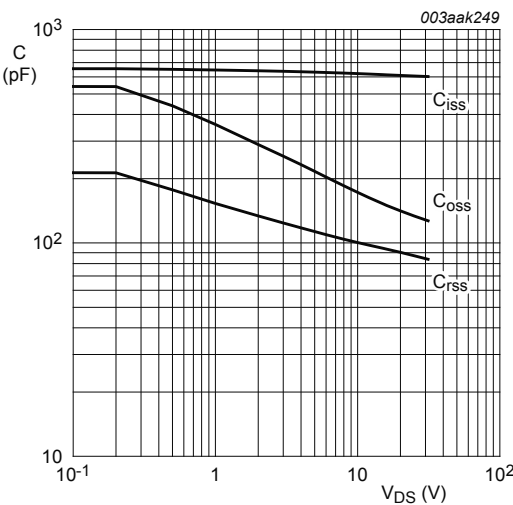


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$



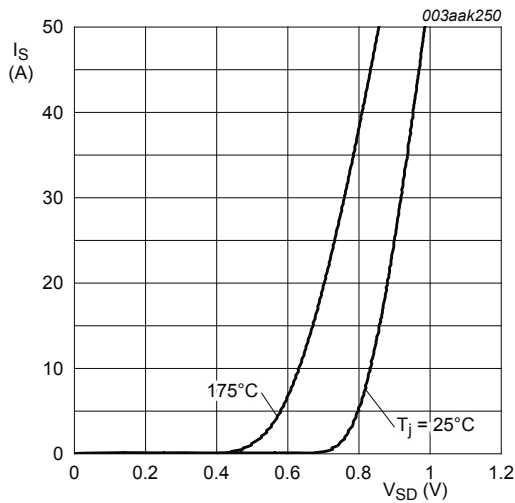


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline

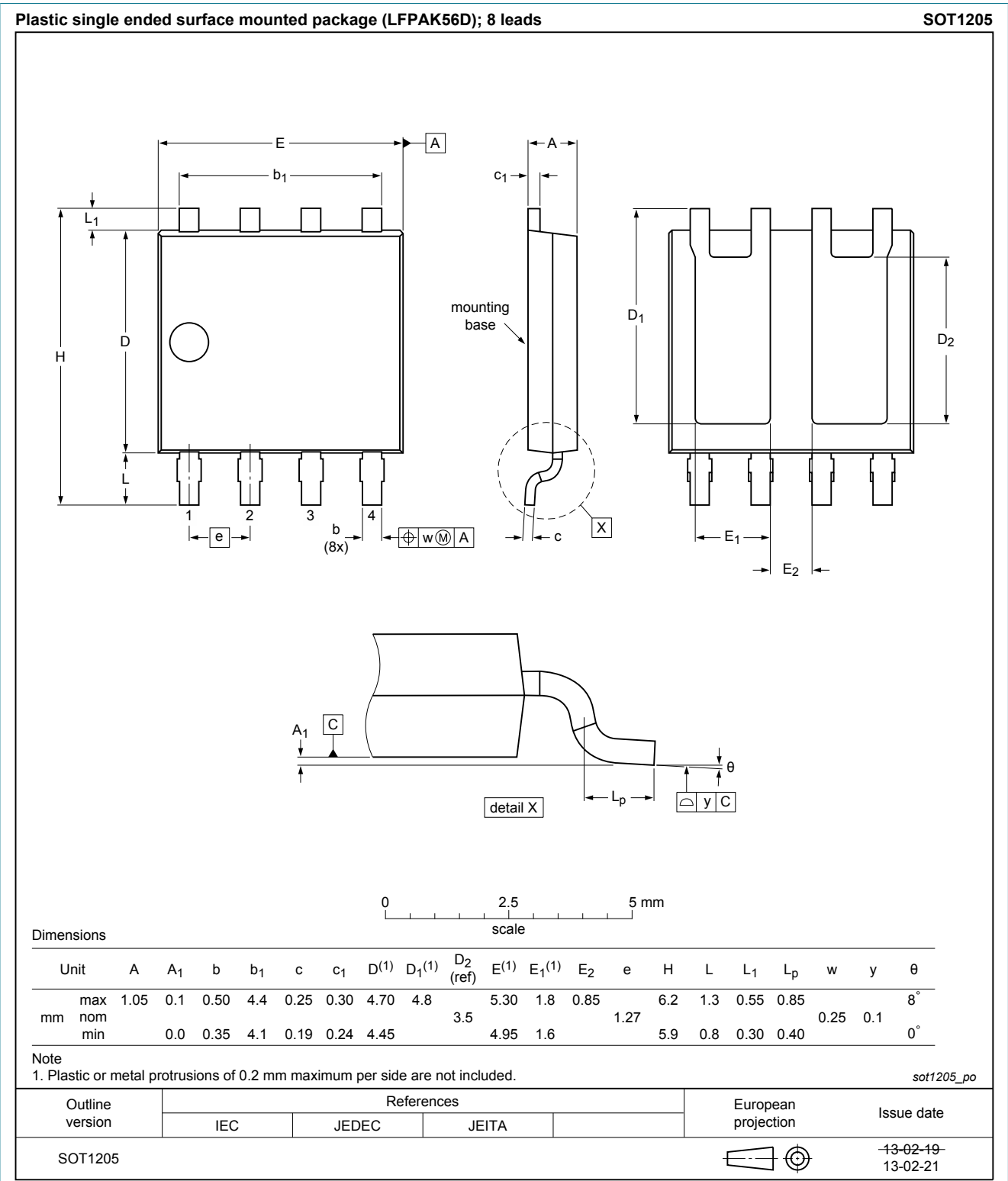


Fig. 17. Package outline LPAK56D (SOT1205)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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13. Contents

1 General description ..... 1

2 Features and benefits ..... 1

3 Applications ..... 1

4 Quick reference data ..... 1

5 Pinning information ..... 2

6 Ordering information ..... 2

7 Marking ..... 2

8 Limiting values ..... 2

9 Thermal characteristics ..... 4

10 Characteristics ..... 5

11 Package outline ..... 10

12 Legal information ..... 11

12.1 Data sheet status ..... 11

12.2 Definitions ..... 11

12.3 Disclaimers ..... 11

12.4 Trademarks ..... 12

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