



PMV75UP

20 V, P-channel Trench MOSFET

25 April 2014

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Low threshold voltage
- Very fast switching
- Enhanced power dissipation capability: $P_{\text{tot}} = 1000 \text{ mW}$

3. Applications

- LED driver
- Power management
- High-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

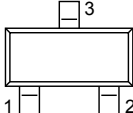
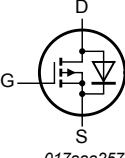
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_{\text{J}} = 25 \text{ }^{\circ}\text{C}$		-	-	-20	V
V_{GS}	gate-source voltage			-12	-	12	V
I_{D}	drain current	$V_{\text{GS}} = -4.5 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^{\circ}\text{C}$; $t \leq 5 \text{ s}$	[1]	-	-	-3.2	A
Static characteristics							
$R_{\text{DS(on)}}$	drain-source on-state resistance	$V_{\text{GS}} = -4.5 \text{ V}$; $I_{\text{D}} = -2.5 \text{ A}$; $T_{\text{J}} = 25 \text{ }^{\circ}\text{C}$		-	77	102	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-236AB (SOT23)	 017aaa257
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMV75UP	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code
PMV75UP	%CN

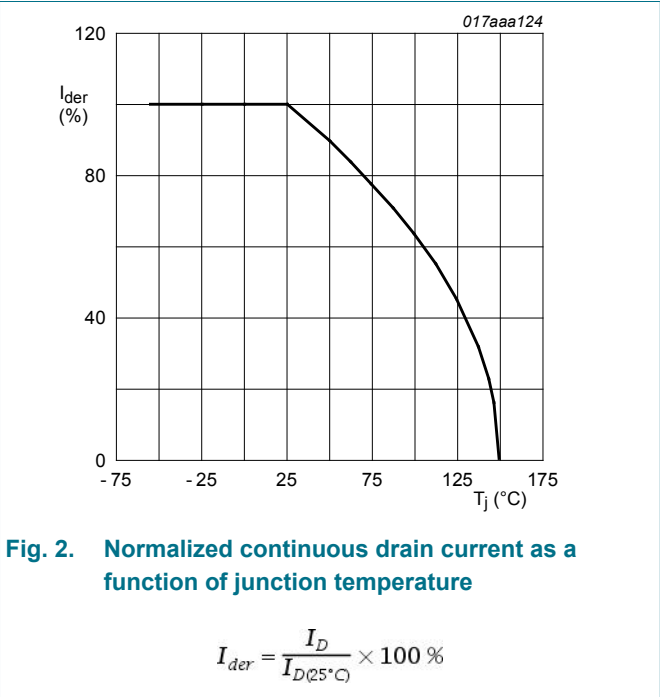
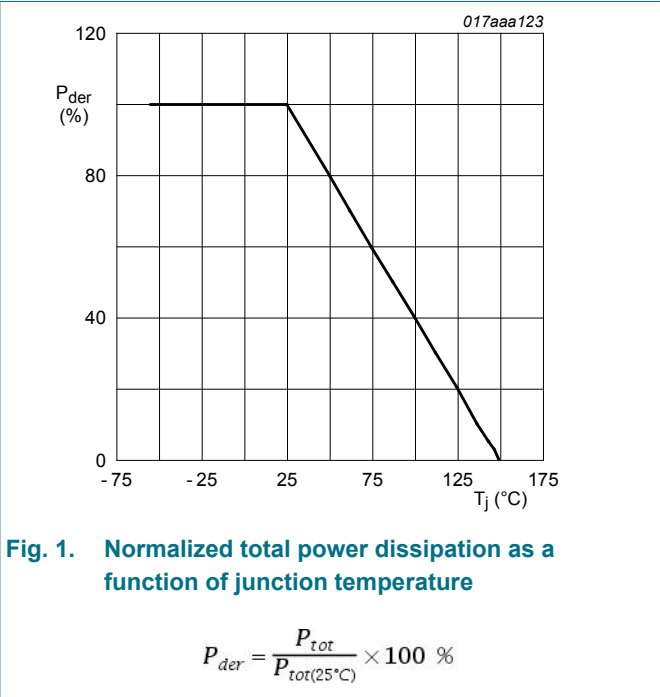
[1] % = placeholder for manufacturing site code

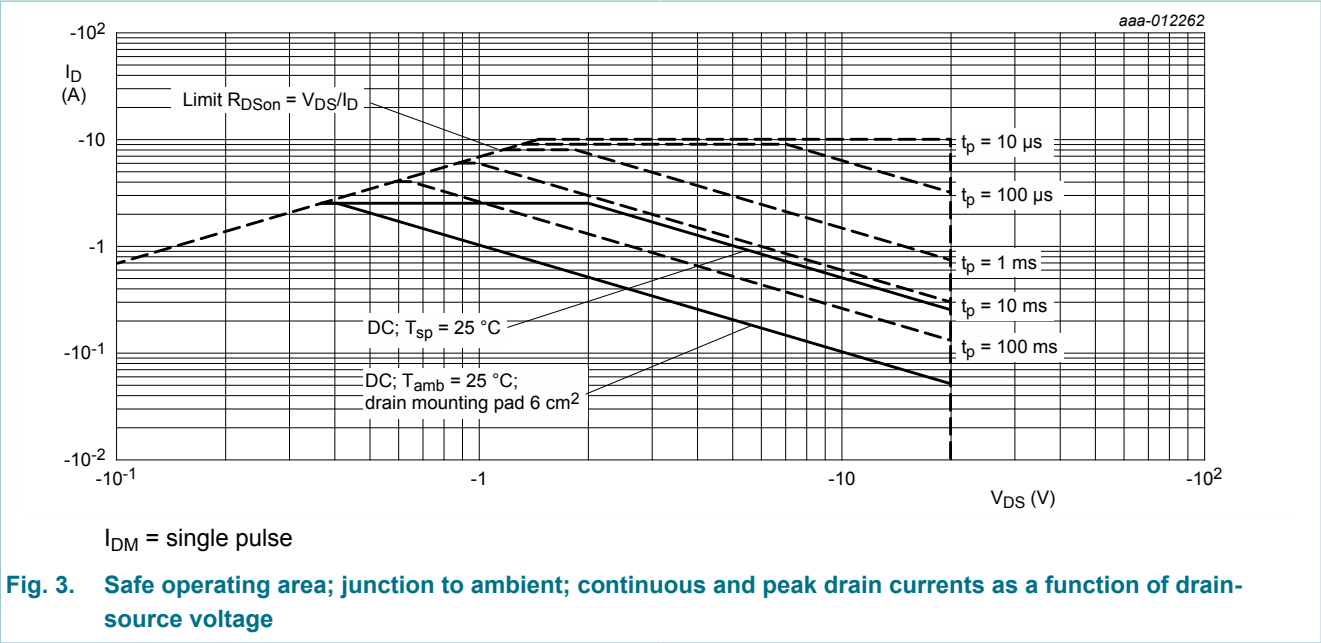
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-3.2	A
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-2.5	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-1.6	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-10	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	490	mW
			[1]	-	1000	mW
		T _{sp} = 25 °C		-	5000	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-0.9	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	217	255	K/W
			[2]	-	105	124	K/W
		in free air; $t \leq 5\ s$	[2]	-	73	86	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	20	25	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain $6\ cm^2$.

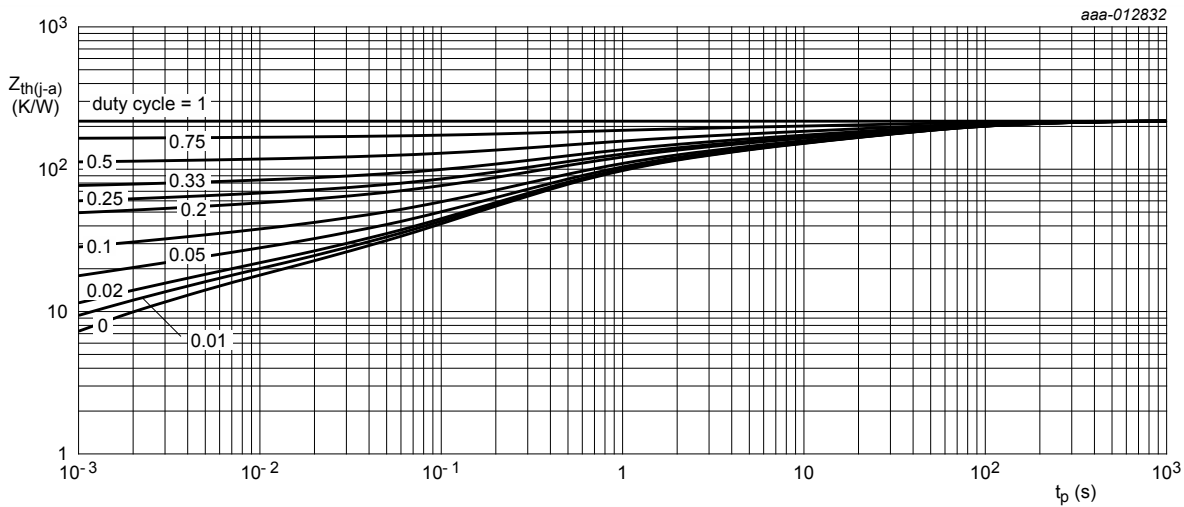


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

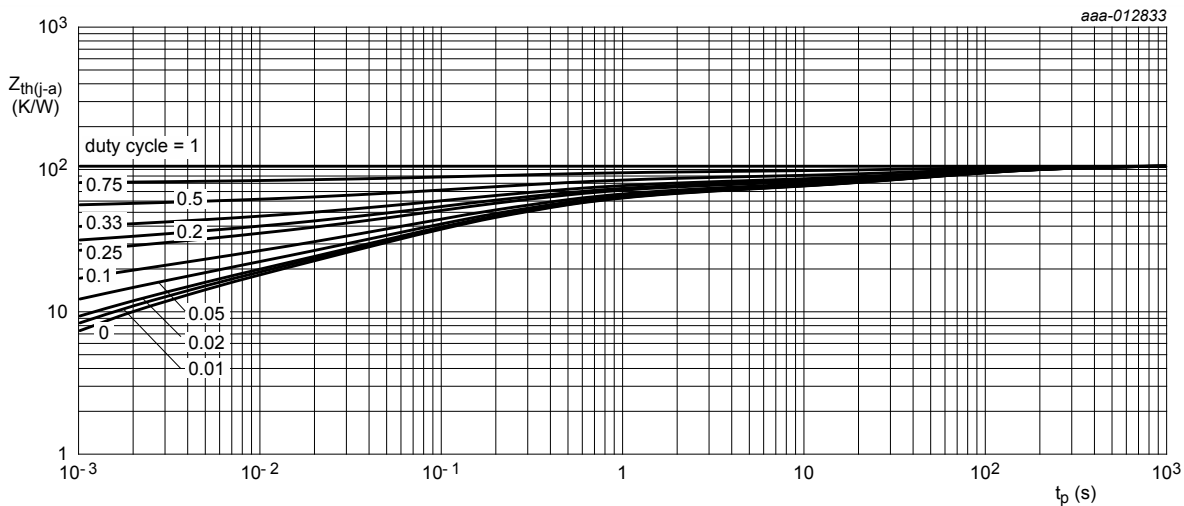


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		-0.47	-0.68	-0.9	V
I _{DSS}	drain leakage current	V _{DS} = -20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
I _{GSS}	gate leakage current	V _{GS} = 12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
		V _{GS} = -12 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -2.5 A; T _j = 25 °C		-	77	102	mΩ
		V _{GS} = -4.5 V; I _D = -2.4 A; T _j = 150 °C		-	110	146	mΩ
		V _{GS} = -2.5 V; I _D = -2.2 A; T _j = 25 °C		-	95	125	mΩ
		V _{GS} = -1.8 V; I _D = -1 A; T _j = 25 °C		-	120	156	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -2 A; T _j = 25 °C		-	15	-	S
R _G	internal gate resistance (AC)	f = 1 MHz		-	41	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -2.5 A; V _{GS} = -4.5 V; T _j = 25 °C		-	5	7.5	nC
Q _{GS}	gate-source charge			-	0.7	-	nC
Q _{GD}	gate-drain charge			-	0.9	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	550	-	pF
C _{oss}	output capacitance			-	63	-	pF
C _{rss}	reverse transfer capacitance			-	53	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -2.5 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	6	-	ns
t _r	rise time			-	14	-	ns
t _{d(off)}	turn-off delay time			-	120	-	ns
t _f	fall time			-	50	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -0.9 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.8	-1.2	V

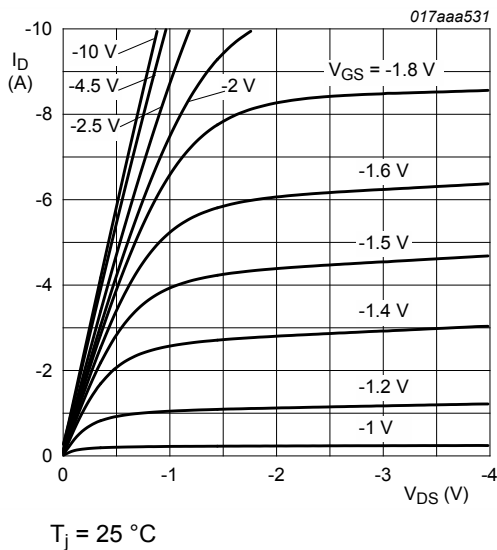


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

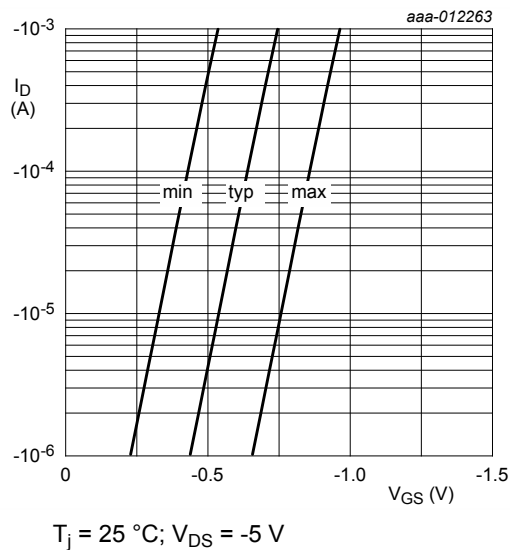


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

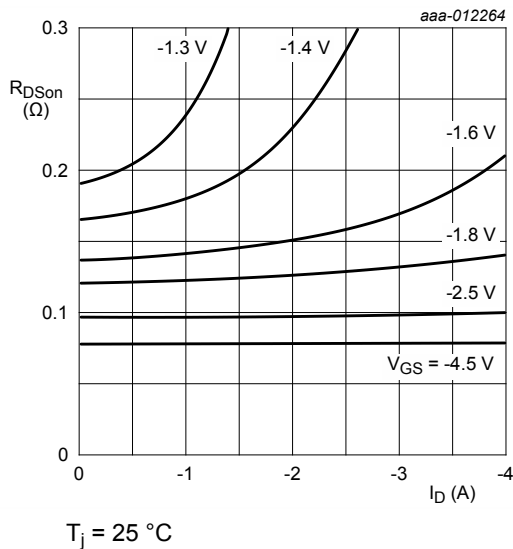


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

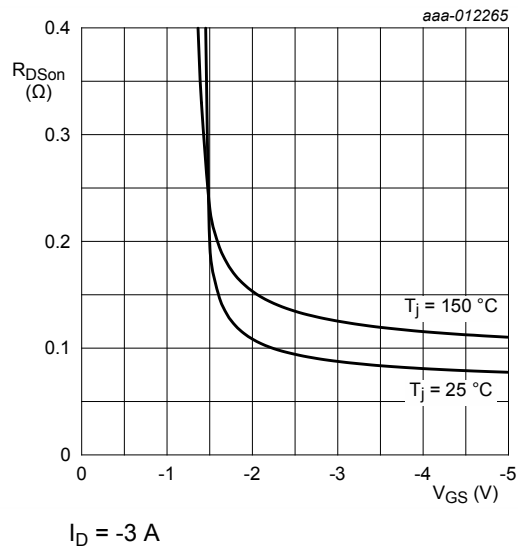


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

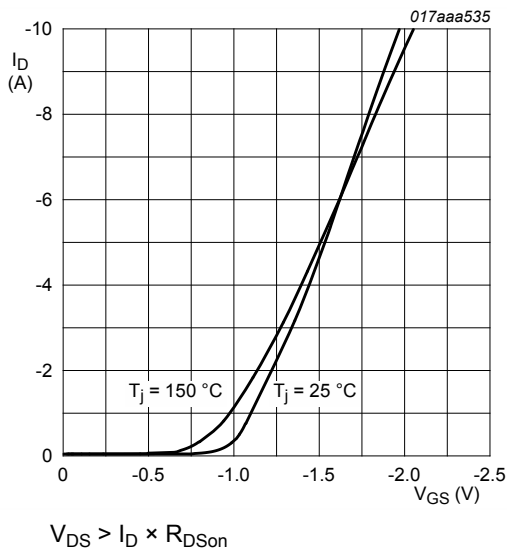


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

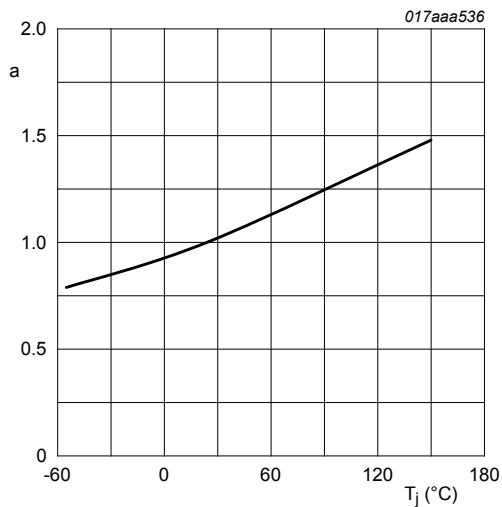


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ °C})}}$$

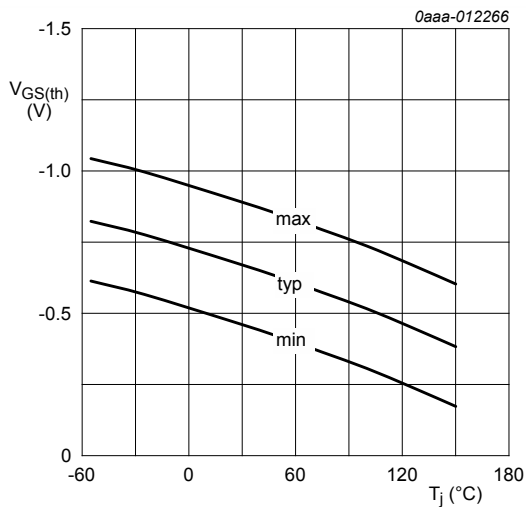


Fig. 12. Gate-source threshold voltage as a function of junction temperature

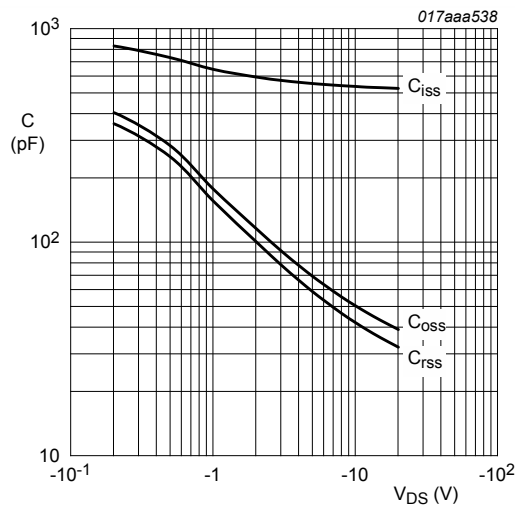


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

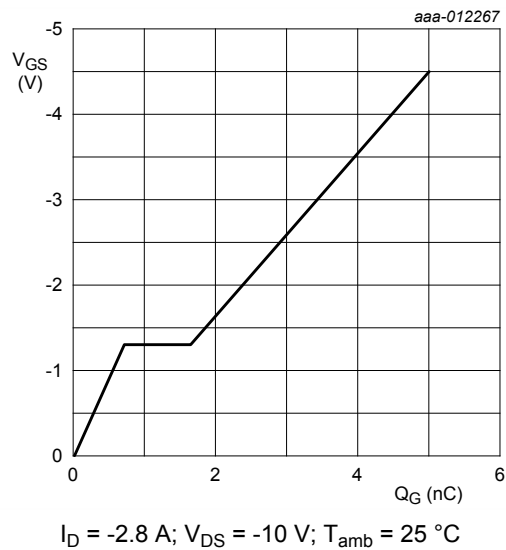


Fig. 14. Gate-source voltage as a function of gate charge; typical values

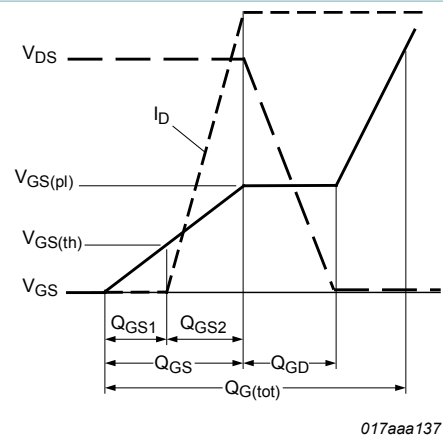
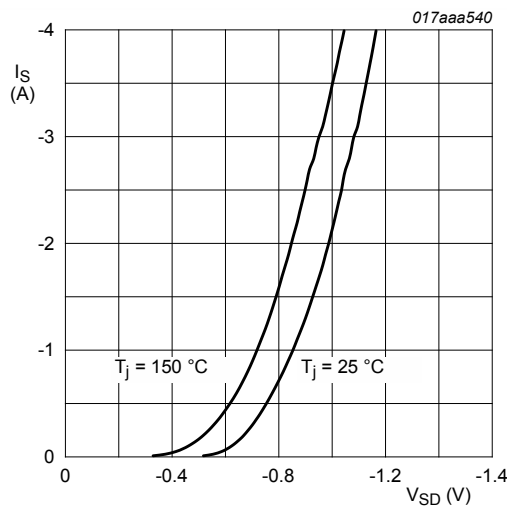


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

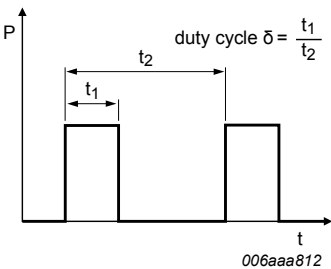


Fig. 17. Duty cycle definition

12. Package outline

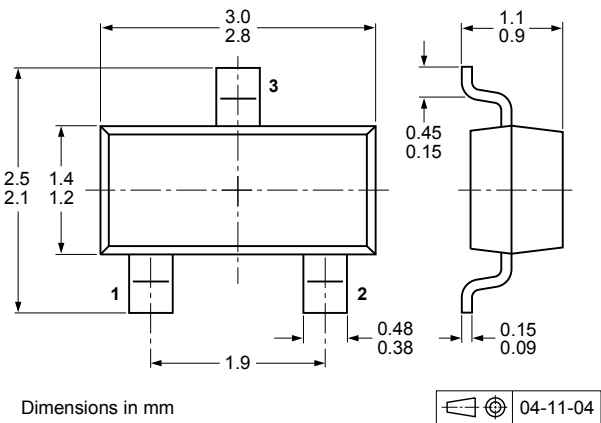


Fig. 18. Package outline TO-236AB (SOT23)

13. Soldering

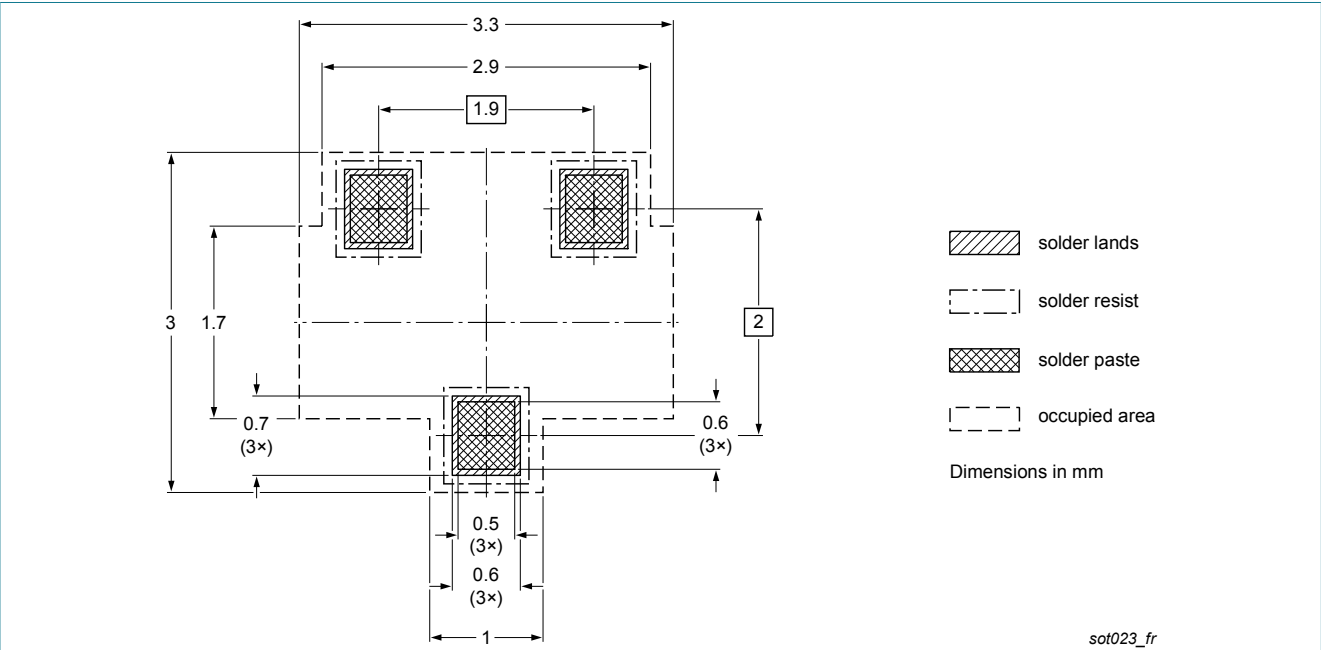


Fig. 19. Reflow soldering footprint for TO-236AB (SOT23)

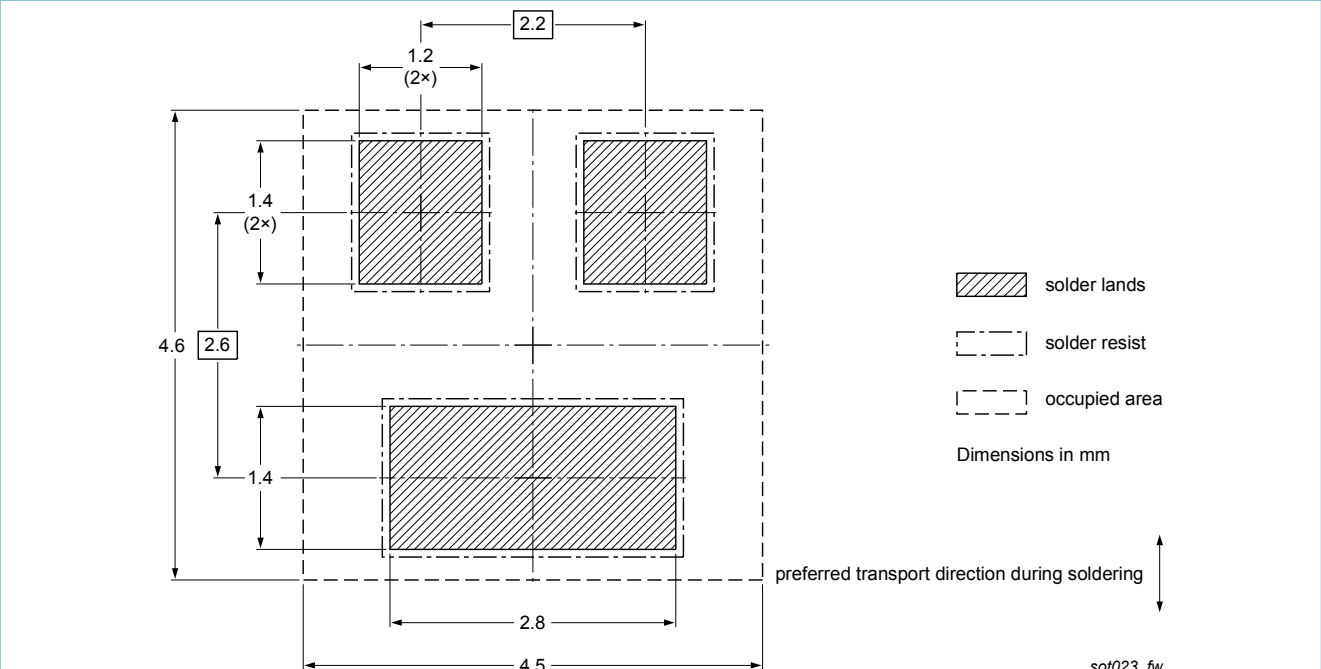


Fig. 20. Wave soldering footprint for TO-236AB (SOT23)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMV75UP v.1	20140425	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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