N-channel 40 V, 11.0 m $\Omega$  standard level MOSFET in LFPAK33 10 January 2025 Product data sheet

## 1. General description

Automotive qualified standard level N-channel MOSFET in an LFPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
  - · Low power losses, high power density
- · LFPAK copper clip package technology:
  - · High robustness and reliability
  - · Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

## 3. Applications

- 12 V automotive systems
- · Powertrain, chassis, body and infotainment applications
- · Medium/Low power motor drive
- · DC-DC systems
- LED lighting

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	40	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	-	35	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	50	W
Static characte	eristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11		6.5	9.3	11	mΩ
Dynamic chara	cteristics			•			
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; Fig. 13; Fig. 14		-	2	4	nC
Source-drain diode							
Q <sub>r</sub>	recovered charge	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}$		-	13	-	nC



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
S	softness factor	$I_S$ = 10 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C	-	0.59	-	

<sup>[1] 35</sup>A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		D
3	S	source		
4	G	gate		G_(□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□
mb	D	Mounting base; connected to drain	1 2 3 4 LFPAK33 (SOT1210)	mbb076 S

# 6. Ordering information

### **Table 3. Ordering information**

Type number	Package				
	Name	Description	Version		
BUK7M11-40H		Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210		

## 7. Marking

## Table 4. Marking codes

Type number	Marking code
BUK7M11-40H	71140н

# 8. Limiting values

### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
$V_{GS}$	gate-source voltage		[1]	-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	50	W
$I_D$	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[2]	-	35	А
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	34	А
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 3		-	193	А
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C

**Product data sheet** 

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drai	n diode					<u>'</u>
Is	source current	T <sub>mb</sub> = 25 °C		-	35	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$		-	193	Α
Avalanche r	ruggedness			,		'
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 35 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[3] [4]	-	16	mJ

- [1] Refer to application note AN90001 for further information.
- [2] 35A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.

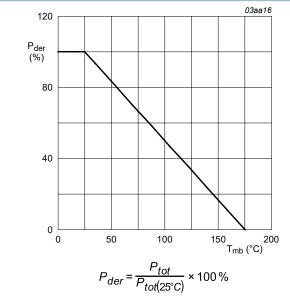
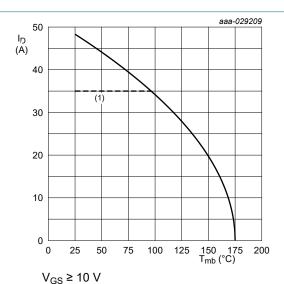


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



(1) 35A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

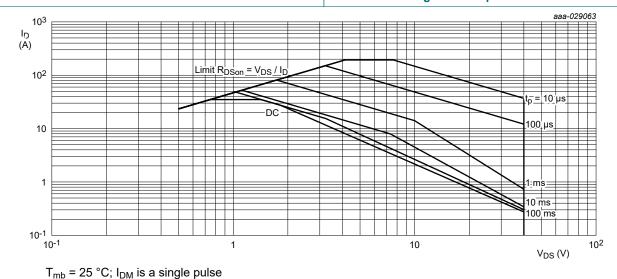
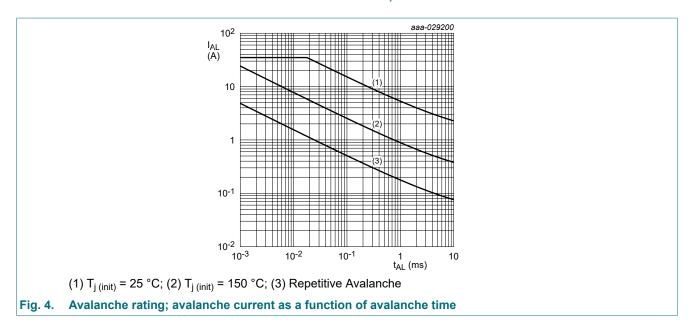


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

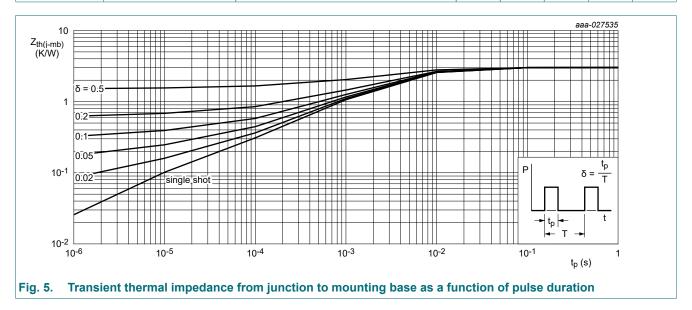
#### N-channel 40 V, 11.0 m $\Omega$ standard level MOSFET in LFPAK33



## 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
	thermal resistance from junction to mounting base	<u>Fig. 5</u>	-	2.79	3	K/W



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## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	40	43	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -40 °C	-	40.5	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	36	40	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 9;$ Fig. 10	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}; Fig. 10$	-	-	4.3	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 175 °C; Fig. 10	1	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.02	1	μA
		V <sub>DS</sub> = 16 V; V <sub>GS</sub> = 0 V; T <sub>i</sub> = 125 °C	-	0.32	10	μΑ
I <sub>GSS</sub>		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	23	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; Fig. 11	6.5	9.3	11	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 105 ^{\circ}\text{C};$ Fig. 12	8.9	13.4	16.5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 125 ^{\circ}\text{C};$ Fig. 12	9.8	14.5	17.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 °C;$ Fig. 12	11.9	17.6	21.3	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.3	0.9	2.3	Ω
Dynamic cl	naracteristics				'	
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V;	-	11.2	16	nC
Q <sub>GS</sub>	gate-source charge	Fig. 13; Fig. 14	-	3.4	5.1	nC
$Q_{GD}$	gate-drain charge		-	2	4	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	730	1022	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	288	403	pF
C <sub>rss</sub>	reverse transfer capacitance		-	35	77	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 3 \Omega; V_{GS} = 10 \text{ V};$	-	4.3	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	2.3	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	8.3	-	ns
t <sub>f</sub>	fall time		-	3.6	-	ns
Source-dra	in diode			'	'	
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <u>Fig. 16</u>	-	0.84	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	20	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 20 V	-	13	-	nC
S	softness factor	$I_S$ = 10 A; $dI_S/dt$ = -100 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C	-	0.59	-	
		I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -500 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>i</sub> = 25 °C	-	0.38	-	

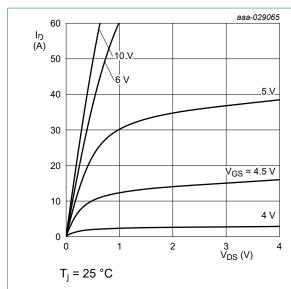


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

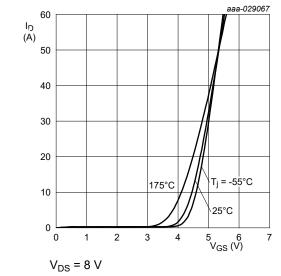


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

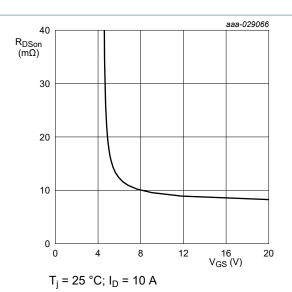


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

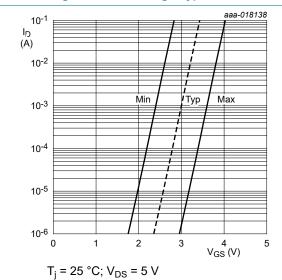


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

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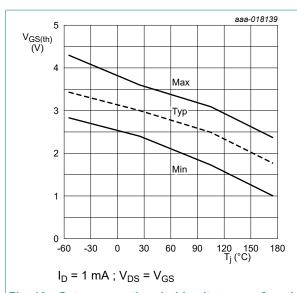


Fig. 10. Gate-source threshold voltage as a function of junction temperature

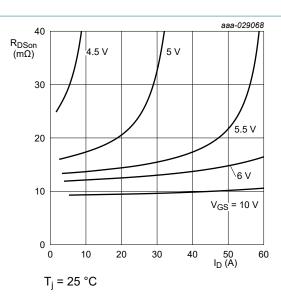


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

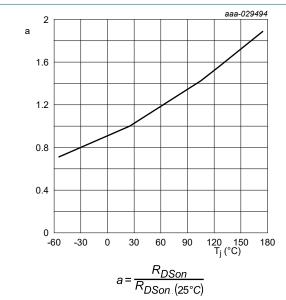


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

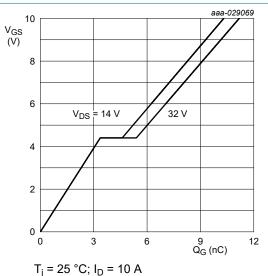


Fig. 13. Gate-source voltage as a function of gate charge; typical values

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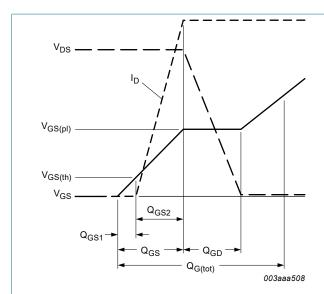
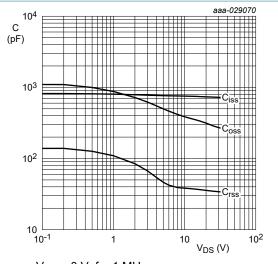


Fig. 14. Gate charge waveform definitions



 $V_{GS} = 0 V$ ; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

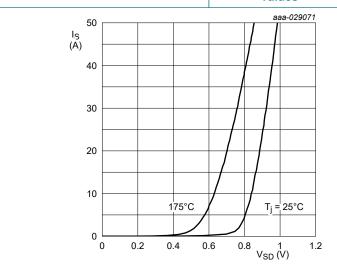
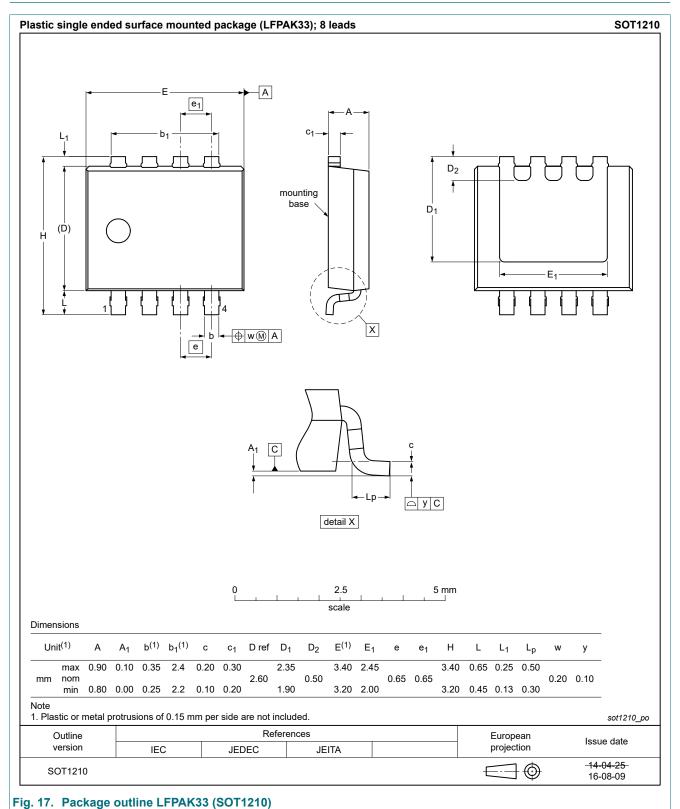


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

 $V_{GS} = 0 V$ 

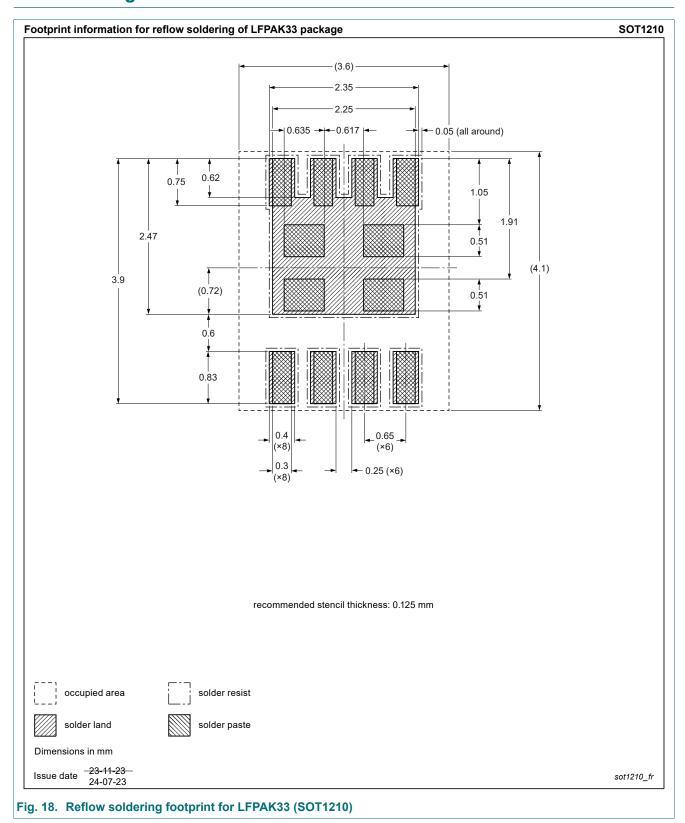
#### N-channel 40 V, 11.0 m $\Omega$ standard level MOSFET in LFPAK33

# 11. Package outline



### N-channel 40 V, 11.0 m $\Omega$ standard level MOSFET in LFPAK33

# 12. Soldering



**Product data sheet** 

## 13. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Product data sheet

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