74LV164-Q100

8-bit serial-in/parallel-out shift register

Rev. 4 — 31 January 2024 Product data sheet

1. General description

The 74LV164-Q100 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB) and either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into Q0, which is the logical AND-function of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset input (MR) overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide operating voltage: 1.0 V to 5.5 V
- Optimized for low-voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce): < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot): > 2 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Gated serial data inputs
- Asynchronous master reset
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV164D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV164PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LV164BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

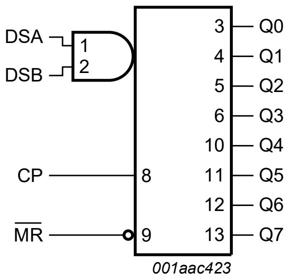


Fig. 1. Logic symbol

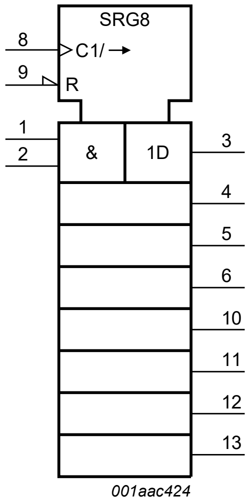


Fig. 2. IEC logic symbol

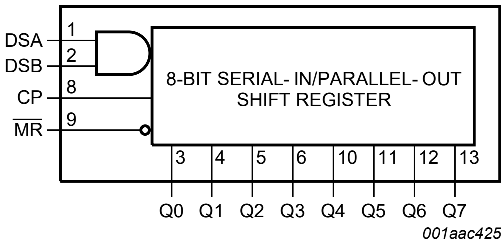
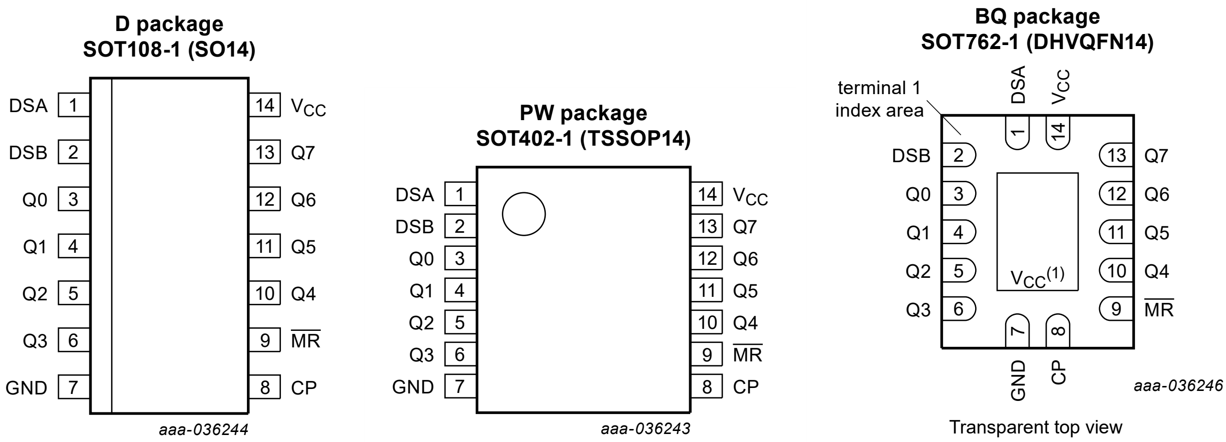


Fig. 3. Functional diagram

5. Pinning information

5.1. Pinning



(1) This is not a supply pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input SA
DSB	2	data input SB
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (edge triggered LOW-to-HIGH)
$\overline{MR}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q = lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH clock transition.

Operating mode	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V [1]	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V [1]	-	±50	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = -100 μA; V_{CC} = 1.2 V	-	1.2	-	-	-	V
		I_O = -100 μA; V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I_O = -100 μA; V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I_O = -100 μA; V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I_O = -100 μA; V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I_O = -6 mA; V_{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
		I_O = -12 mA; V_{CC} = 4.5 V	3.6	4.2	-	3.5	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		I_O = 100 μA; V_{CC} = 1.2 V	-	0	-	-	-	V
		I_O = 100 μA; V_{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I_O = 100 μA; V_{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I_O = 6 mA; V_{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
		I_O = 12 mA; V_{CC} = 4.5 V	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20.0	-	160	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ - 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Fig. 7.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	CP to Qn; see Fig. 4	[2]						
		V_{CC} = 1.2 V		-	75	-	-	-	ns
		V_{CC} = 2.0 V		-	26	39	-	49	ns
		V_{CC} = 2.7 V		-	19	29	-	36	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	12	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	14	23	-	29	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	-	12	19	-	24	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 5							
		V_{CC} = 1.2 V		-	75	-	-	-	ns
		V_{CC} = 2.0 V		-	26	39	-	49	ns
		V_{CC} = 2.7 V		-	19	29	-	36	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	12	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	14	23	-	29	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	-	12	19	-	24	ns
t_W	pulse width	CP; see Fig. 4							
		V_{CC} = 2.0 V		34	9	-	41	-	ns
		V_{CC} = 2.7 V		25	6	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	5	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	13	4	-	16	-	ns
		$\overline{MR}$; Fig. 5							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	6	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	13	5	-	16	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 5							
		V_{CC} = 1.2 V		-	30	-	-	-	ns
		V_{CC} = 2.0 V		19	10	-	24	-	ns
		V_{CC} = 2.7 V		14	8	-	18	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	11	6	-	14	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	8	5	-	10	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 6							
		V_{CC} = 1.2 V		-	15	-	-	-	ns
		V_{CC} = 2.0 V		22	5	-	26	-	ns
		V_{CC} = 2.7 V		16	4	-	19	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	13	3	-	15	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	9	2	-	10	-	ns

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_h	hold time	Dn to CP; see Fig. 6							
		V_{CC} = 1.2 V		-	-10	-	-	-	ns
		V_{CC} = 2.0 V		5	-3	-	5	-	ns
		V_{CC} = 2.7 V		5	-2	-	5	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	5	-2	-	5	-	ns
		V_{CC} = 4.5 V to 5.5 V	[3]	5	-1	-	5	-	ns
f_{max}	maximum frequency	see Fig. 4							
		V_{CC} = 2.0 V		14	40	-	12	-	MHz
		V_{CC} = 2.7 V		19	58	-	16	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF		-	78	-	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[3]	24	70	-	20	-	MHz
		V_{CC} = 4.5 V to 5.5 V	[3]	36	100	-	30	-	MHz
C_{PD}	power dissipation capacitance	V_{CC} = 3.3 V; C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	40	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz, f_o = output frequency in MHz

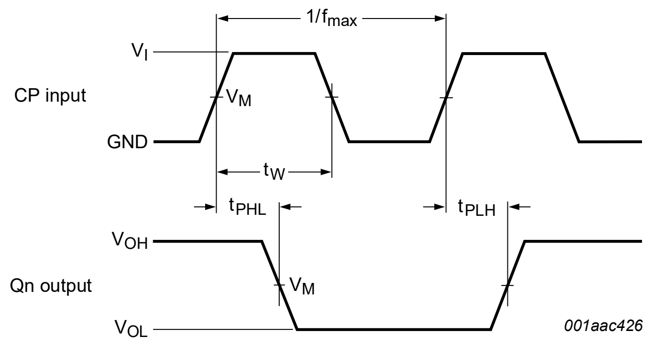
C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

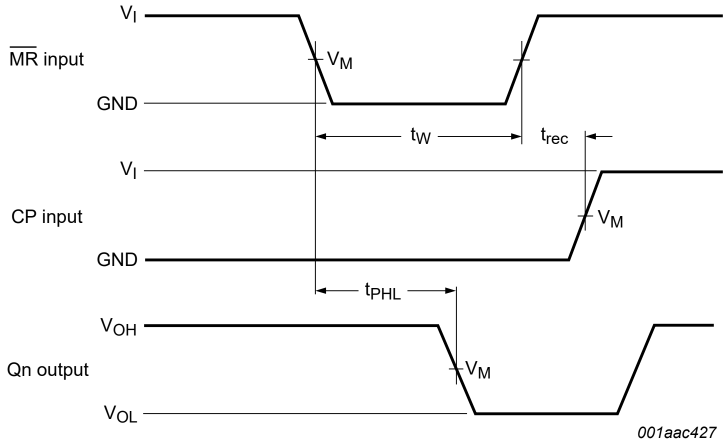
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

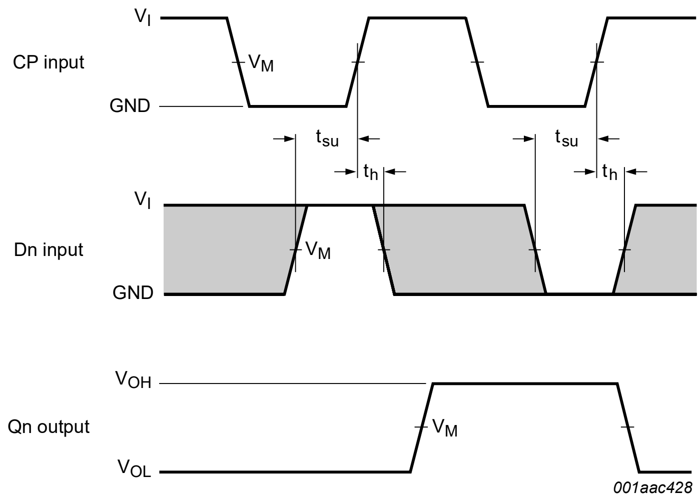
Fig. 4. Propagation delay clock (CP) to output (Qn), clock pulse width and maximum clock frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Pulse width master reset ($\overline{MR}$), propagation delay master reset ($\overline{MR}$) to output (Qn) and the master reset ($\overline{MR}$) to clock (CP) recovery time



Measurement points are given in Table 8.

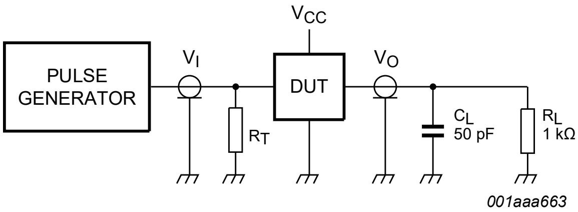
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6. Data set-up and hold times inputs (Dn) to clock (CP)

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	0.5 × V_{CC}	0.5 × V_{CC}
2.0 V	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5 × V_{CC}	0.5 × V_{CC}



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance;
C_L = Load capacitance including jig and probe capacitance;
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

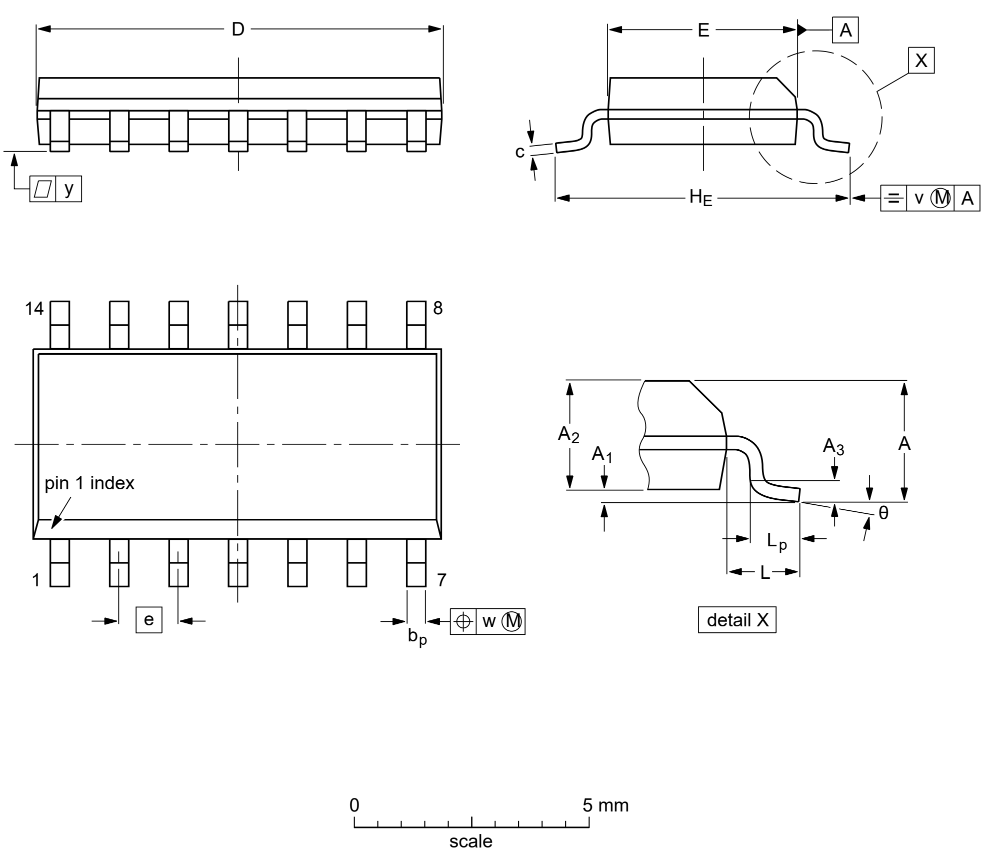
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		Test
V_{CC}	V_I	t_r , t_f	C_L	R_L	
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.0 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
2.7 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF, 15 pF	1 kΩ	t_{PHL}, t_{PLH}
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	t_{PHL}, t_{PLH}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

Note

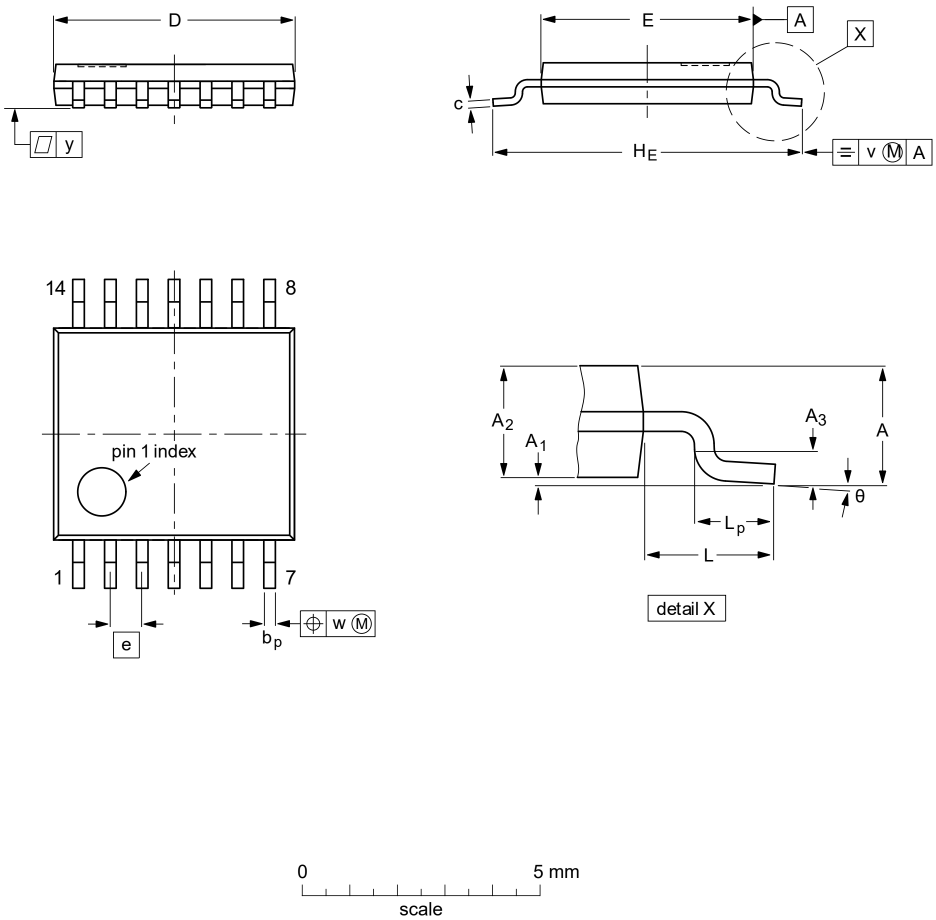
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

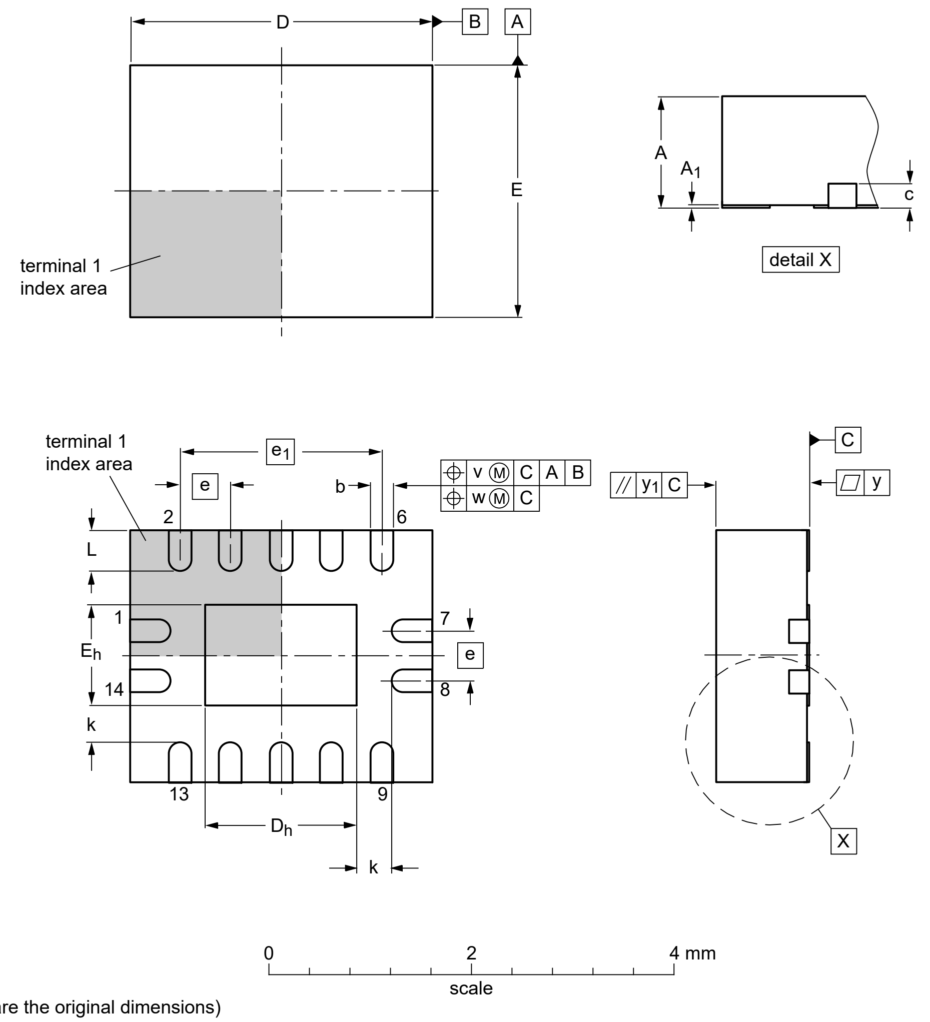
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV164_Q100 v.4	20240131	Product data sheet	-	74LV164_Q100 v.3
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74LV164_Q100 v.3	20200915	Product data sheet	-	74LV164_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation have been updated. • Package outline drawing of SOT762-1 (Fig. 10) updated.			
74LV164_Q100 v.2	20140918	Product data sheet	-	74LV164_Q100 v.1
Modifications:	• Section 2: ESD protection: MIL-STD-833 changed to MIL-STD883			
74LV164_Q100 v.1	20130626	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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