

74LVCU04A

Hex unbuffered inverter

Rev. 12 — 20 January 2025

Product data sheet

1. General description

The 74LVCU04A is a hex unbuffered inverter. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

2. Features and benefits

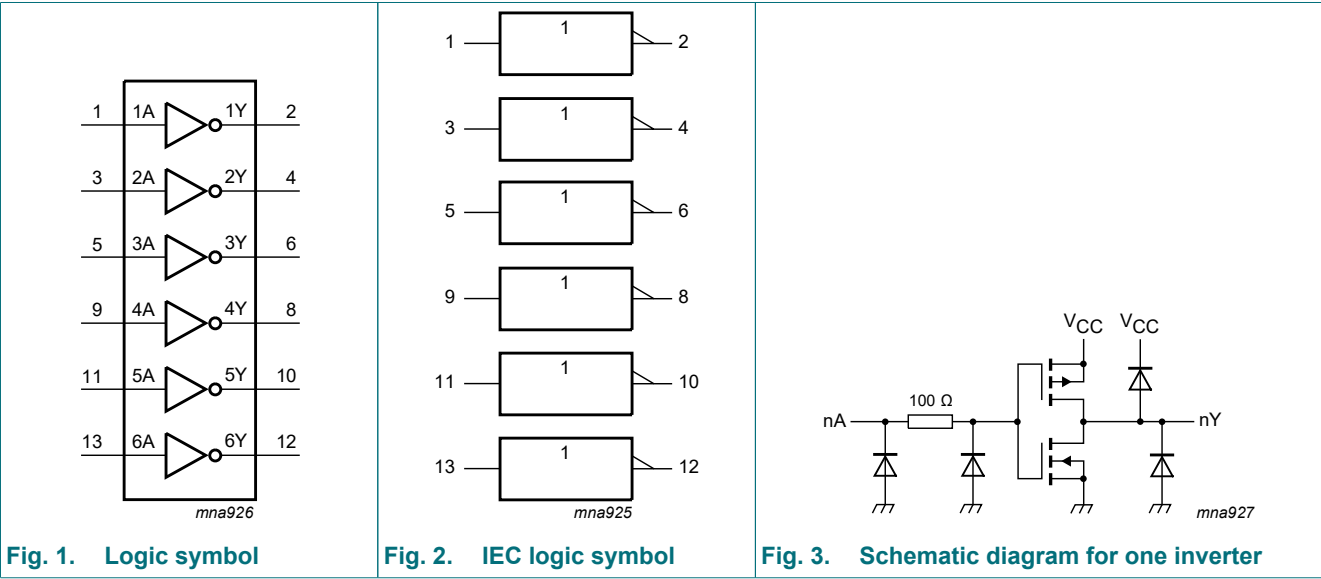
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVCU04AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVCU04APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVCU04ABQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram



5. Pinning information

5.1. Pinning

D package
SOT108-1 (SO14)

aaa-035254

PW package
SOT402-1 (TSSOP14)

aaa-035585

BQ package
SOT762-1 (DHVQFN14)

terminal 1 index area

Transparent top view

aaa-035256

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input nA	Output nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	[2]	-0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{OL(max)} = 0.5 V; I _O = -100 µA						
		V _{CC} = 1.2 V	1.08	-	-	1.12	-	V
		V _{CC} = 1.65 V to 1.95 V	1.3	-	-	1.5	-	V
		V _{CC} = 2.3 V to 2.7 V	1.8	-	-	2.0	-	V
		V _{CC} = 3.0 V	2.0	-	-	2.4	-	V
		V _{CC} = 3.6 V	2.4	-	-	2.8	-	V
V _{IL}	LOW-level input voltage	V _{OH(min)} = V _{CC} - 0.5 V; I _O = -100 µA						
		V _{CC} = 1.2 V	-	-	0.12	-	0.1	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.6	-	0.4	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.5	V
		V _{CC} = 3.0 V	-	-	1.0	-	0.6	V
		V _{CC} = 3.6 V	-	-	1.2	-	0.7	V
V _{OH}	HIGH-level output voltage	V _I = GND						
		V _{CC} = 3.0 V; I _O = -100 µA	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		V _{CC} = 1.65 V; I _O = -4 mA	1.2	-	-	1.05	-	V
		V _{CC} = 2.3 V; I _O = -8 mA	1.8	-	-	1.65	-	V
		V _{CC} = 2.7 V; I _O = -12 mA	2.2	-	-	2.05	-	V
		V _{CC} = 3.0 V; I _O = -18 mA	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{CC}						
		V _{CC} = 3.0 V; I _O = 100 µA	-	-	0.20	-	0.60	V
		V _{CC} = 1.65 V; I _O = 4 mA	-	-	0.45	-	0.65	V
		V _{CC} = 2.3 V; I _O = 8 mA	-	-	0.60	-	0.80	V
		V _{CC} = 2.7 V; I _O = 12 mA	-	-	0.40	-	0.60	V
		V _{CC} = 3.0 V; I _O = 24 mA	-	-	0.55	-	0.80	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.5	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

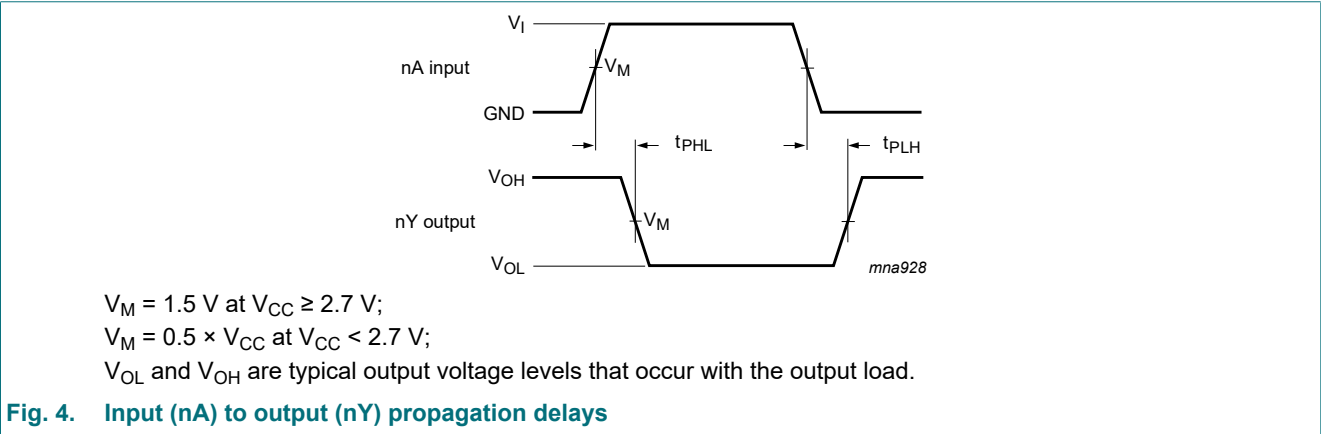
10. Dynamic characteristics

Table 7. Dynamic characteristics
 Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 4 [2]						
		V _{CC} = 1.2 V	-	6.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	0.3	3.7	7.8	0.3	9.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	4.4	0.5	5.2	ns
		V _{CC} = 2.7 V	0.5	2.0	4.5	0.5	6.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.0	4.0	0.5	5.0	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V [3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation capacitance	per inverter; V _I = GND to V _{CC} [4]						
		V _{CC} = 1.65 V to 1.95 V	-	2.3	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	5.5	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	8.4	-	-	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = number of inputs switching
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

10.1. Waveforms and test circuit



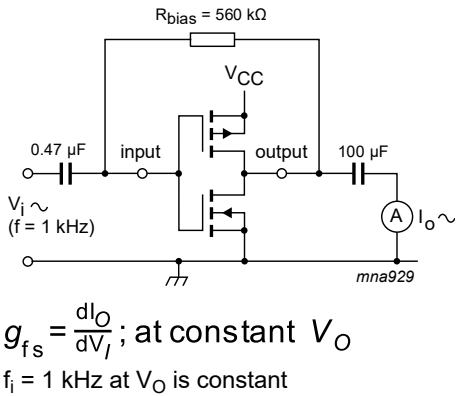


Fig. 5. Test setup for measuring forward transconductance

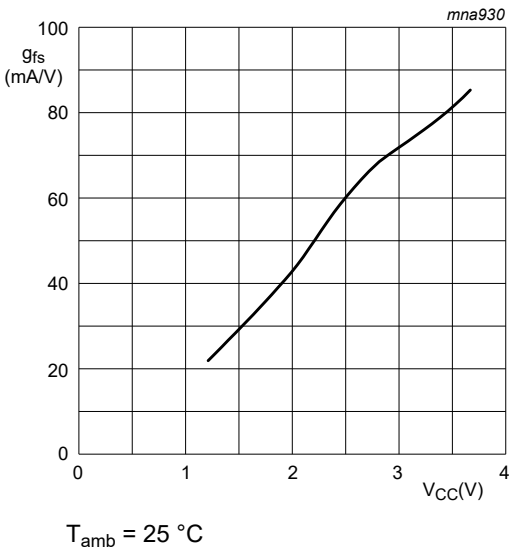
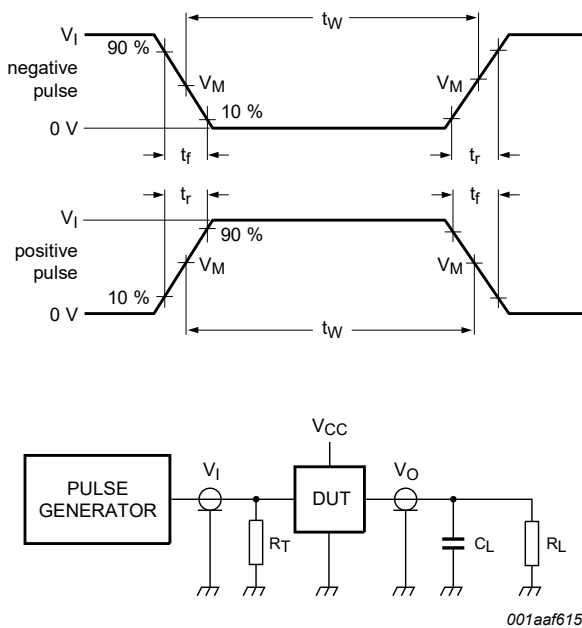


Fig. 6. Typical forward transconductance as a function of supply voltage



Test data is given in [Table 8](#). Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 7. Test circuit for measuring switching times

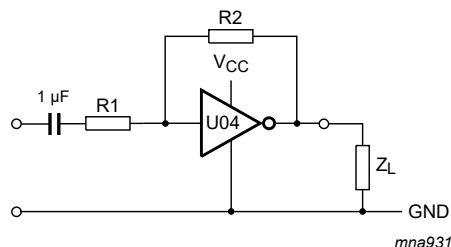
Table 8. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	500 Ω
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω

11. Application information

Some applications for the 74LVCU04A are:

- Linear amplifier: see [Fig. 8](#)
- Crystal oscillator designs; see [Fig. 9](#)
- Astable multivibrator; see [Fig. 10](#)



$$V_{o(p-p)} = V_{CC} - 1.5 \text{ V centered at } 0.5V_{CC}.$$

$$A_u = - \frac{G_{OL}}{1 + \frac{R1}{R2}(1 + G_{OL})}$$

G_{OL} = loop gain.

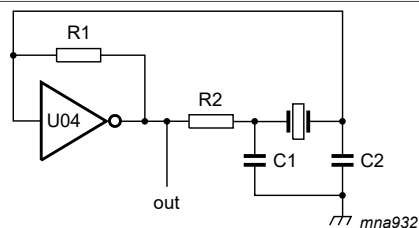
A_u = voltage amplification.

$R1 \geq 3 \text{ k}\Omega$, $R2 \leq 1 \text{ M}\Omega$

$Z_L > 10 \text{ k}\Omega$; $A_{OL} = 20$ (typ.)

Typical unity gain bandwidth product is 5 MHz.

Fig. 8. 74LVCU04A used as linear amplifier



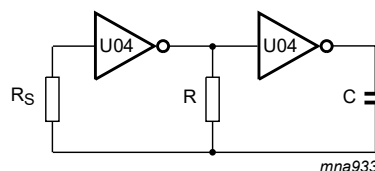
$C_1 = 47 \text{ pF}$ (typical)

$C_2 = 22 \text{ pF}$ (typical)

$R_1 = 1 \text{ to } 10 \text{ M}\Omega$ (typical)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at $V_{CC} = 3 \text{ V}$ and $f = 1 \text{ MHz}$)

Fig. 9. 74LVCU04A used as crystal oscillator



$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

$R_S \approx 2R$.

The average I_{CC} is approximately
 $3.5 + 0.05 f \text{ (MHz)} \times C \text{ (pF)}$ [mA] at $V_{CC} = 3.0 \text{ V}$.

Fig. 10. 74LVCU04A used as astable multivibrator

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig. 11. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

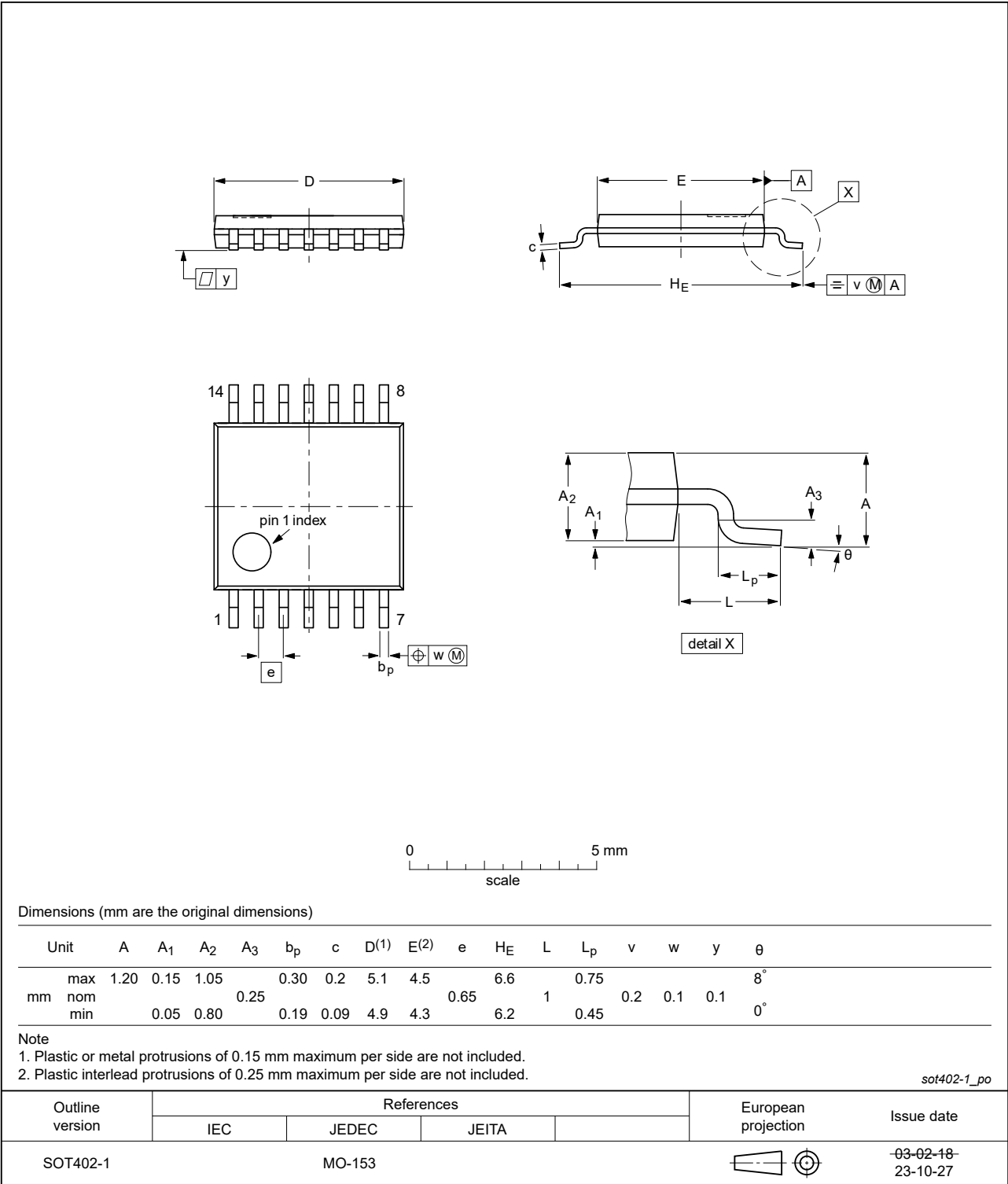


Fig. 12. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 13. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCU04A v.12	20250120	Product data sheet	-	74LVCU04A v.11
Modifications:	Table 6: $V_{OL(max)}$ at $T_{amb} = +125\text{ }^{\circ}\text{C}$ and $V_{CC} = 2.7\text{ V}$ changed to 0.6 V.			
74LVCU04A v.11	20240228	Product data sheet	-	74LVCU04A v.10
Modifications:	Fig. 11, Fig. 12: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVCU04A v.10	20230830	Product data sheet	-	74LVCU04A v.9
Modifications:	Section 1 updated. Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVCU04A v.9	20210331	Product data sheet	-	74LVCU04A v.8
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74LVCU04ADB (SOT337-1 / SSOP14) removed. Section 1 updated. Section 7: Derating values for P_{tot} total power dissipation updated.			
74LVCU04A v.8	20151218	Product data sheet	-	74LVCU04A v.7
Modifications:	Descriptive title updated. Added "unbuffered" (errata).			
74LVCU04A v.7	20111117	Product data sheet	-	74LVCU04A v.6
Modifications:	- Legal pages updated. Table 6, bodyrow ΔI_{CC}: condition V_{CC} changed.			
74LVCU04A v.6	20110809	Product data sheet	-	74LVCU04A v.5
74LVCU04A v.5	20040312	Product specification	-	74LVCU04A v.4
74LVCU04A v.4	20030901	Product specification	-	74LVCU04A v.3
74LVCU04A v.3	19980729	Product specification	-	74LVCU04A v.2
74LVCU04A v.2	19980729	Product specification	-	74LVCU04A v.1
74LVCU04A v.1	19980729	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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