Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020M-6 (SOT1220-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- · Low threshold voltage
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- · Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection > 2000 V HBM (class H2)

3. Applications

- · Charging switch for portable devices
- DC-to-DC converters
- · Power management in battery-driven portable devices
- · Hard disk and computing power management

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V _{DS}	drain-source voltage	T _j = 25 °C		-	-	-20	V	
V _{GS}	gate-source voltage			-10	-	10	V	
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-	-11	Α	
Static characte	Static characteristics							
R _{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -7.6 \text{ A}; T_j = 25 \text{ °C}$		-	17	21	mΩ	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain		D
2	D	drain	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
3	G	gate	7	
4	S	source	2 5	G (T)
5	D	drain	3 8 4	
6	D	drain	Transparent top view	
7	D	drain	DFN2020M-6 (SOT1220-2)	S 017aaa259
8	S	source		017aaa259

6. Ordering information

Table 3. Ordering information

Type number	Package						
	Name	Description	Version				
PMPB19R0UPE		plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2				

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB19R0UPE	ZR

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-10	10	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	-11	А
		V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-7.6	А
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-4.8	А
I _{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \le 10 \mu s$		-	-30	Α
P _{tot}	total power dissipation	T _{amb} = 25 °C; t ≤ 5 s	[1]	-	3.5	W
		T _{amb} = 25 °C	[1]	-	1.8	W
		T _{sp} = 25 °C		-	12.5	W
Tj	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain	n diode			<u> </u>		'
I _S	source current	T _{amb} = 25 °C	[1]	-	-1.7	А

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

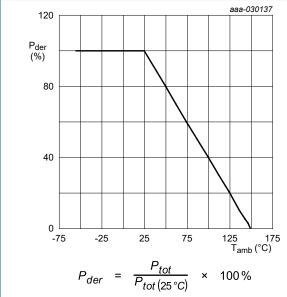


Fig. 1. Normalized total power dissipation as a function of ambient temperature

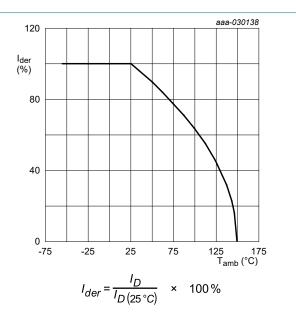


Fig. 2. Normalized continuous drain current as a function of ambient temperature

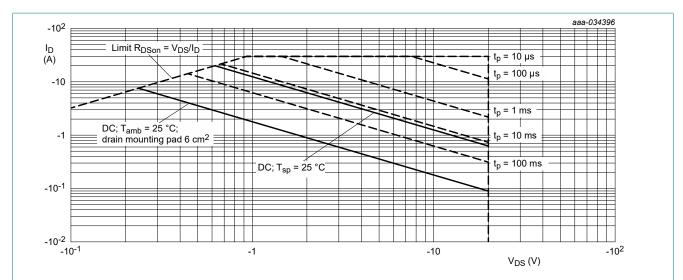


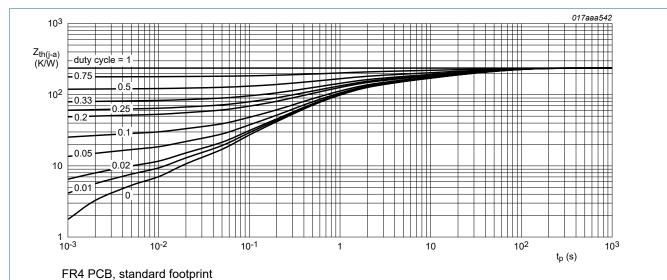
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

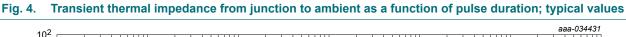
9. Thermal characteristics

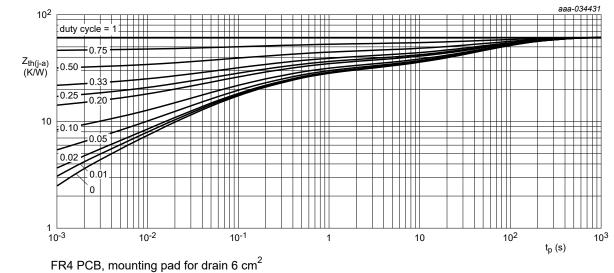
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)} thermal resistance from junction to ambient	thermal resistance from		[1]	-	235	270	K/W
	junction to ambient		[2]	-	61	70	K/W
	in free air; t ≤ 5 s	[2]	-	33	36	K/W	
R _{th(j-sp)}	thermal resistance from junction to solder point			-	7	10	K/W

- Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².







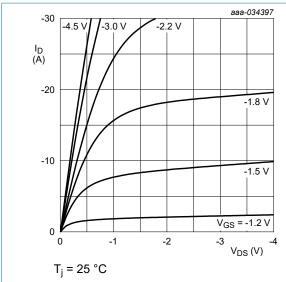
Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

Product data sheet

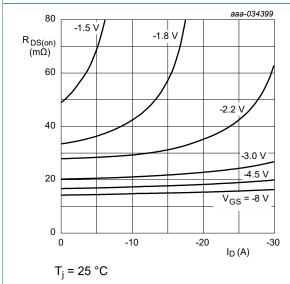
10. Characteristics

Table 7. Characteristics

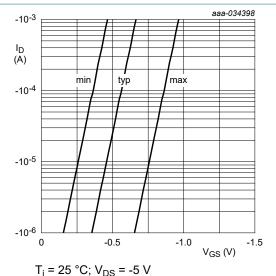
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source breakdown voltage	I_D = -250 μ A; V_{GS} = 0 V; T_j = 25 °C	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \ \mu A; \ V_{DS} = V_{GS}; \ T_j = 25 \ ^{\circ}C$	-0.4	-0.6	-0.9	V
I _{DSS}	drain leakage current	$V_{DS} = -20 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-1	μΑ
I _{GSS}	gate leakage current	V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-10	μA
		V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	10	μΑ
		$V_{GS} = -4.5 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	-2	μΑ
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C	-	-	2	μA
R _{DSon}	drain-source on-state	$V_{GS} = -4.5 \text{ V}; I_D = -7.6 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	17	21	mΩ
	resistance	V _{GS} = -4.5 V; I _D = -7.6 A; T _j = 150 °C	-	25	31	mΩ
		V_{GS} = -2.5 V; I_{D} = -6.3 A; T_{j} = 25 °C	-	24	30	mΩ
		V _{GS} = -1.8 V; I _D = -1 A; T _j = 25 °C	-	34	52	mΩ
		$V_{GS} = -1.5 \text{ V}; I_D = -0.1 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	50	110	mΩ
9 _{fs}	forward transconductance	$V_{DS} = -10 \text{ V}; I_D = -7.6 \text{ A}; T_j = 25 \text{ °C}$	-	17	-	S
R _G	gate resistance	f = 1 MHz	-	8	-	Ω
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	V_{DS} = -10 V; I_{D} = -7.4 A; V_{GS} = -4.5 V;	-	16	24	nC
Q _{GS}	gate-source charge	T _j = 25 °C	-	1.8	-	nC
Q_{GD}	gate-drain charge		-	5.1	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V;	-	1275	-	pF
C _{oss}	output capacitance	T _j = 25 °C	-	191	-	pF
C _{rss}	reverse transfer capacitance		-	171	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = -10 \text{ V}; I_D = -7.2 \text{ A}; V_{GS} = -4.5 \text{ V};$	-	4	-	ns
t _r	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	19	-	ns
t _{d(off)}	turn-off delay time	1	-	62	-	ns
t _f	fall time		-	36	-	ns
Source-dra	in diode		1	1		
V_{SD}	source-drain voltage	I _S = -1.7 A; V _{GS} = 0 V; T _i = 25 °C	-	-0.7	-1.2	V



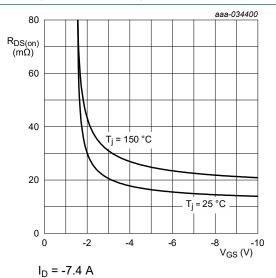
Output characteristics: drain current as a function of drain-source voltage; typical values



Drain-source on-state resistance as a function Fig. 8. of drain current; typical values



Sub-threshold drain current as a function of Fig. 7. gate-source voltage



Drain-source on-state resistance as a function Fig. 9. of gate-source voltage; typical values

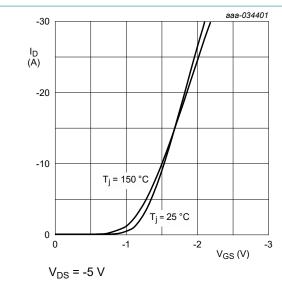


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

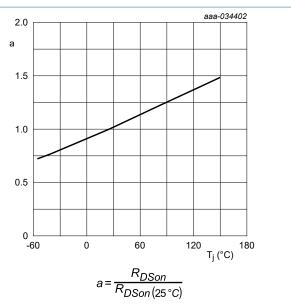


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

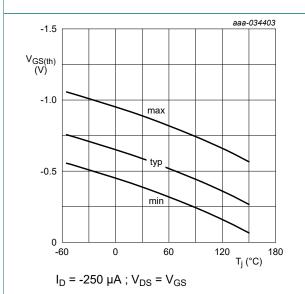
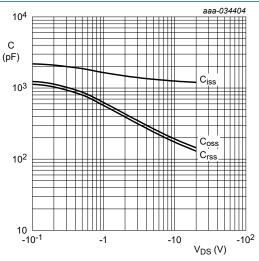


Fig. 12. Gate-source threshold voltage as a function of junction temperature



 $V_{GS} = 0 V$; f = 1 MHz

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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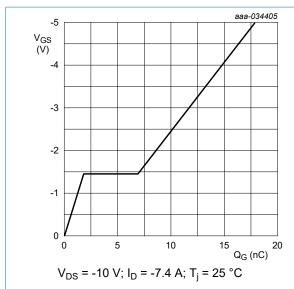


Fig. 14. Gate-source voltage as a function of gate charge; typical values

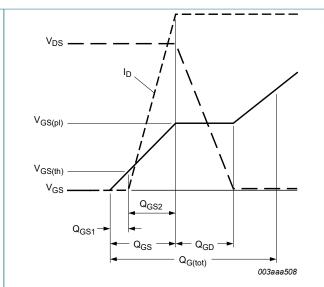


Fig. 15. Gate charge waveform definitions

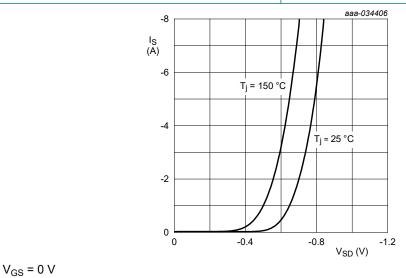
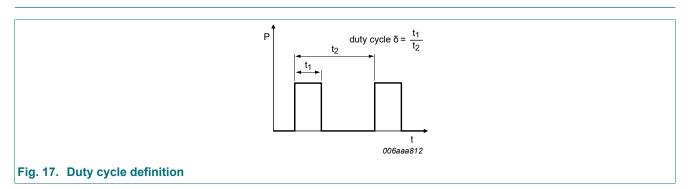


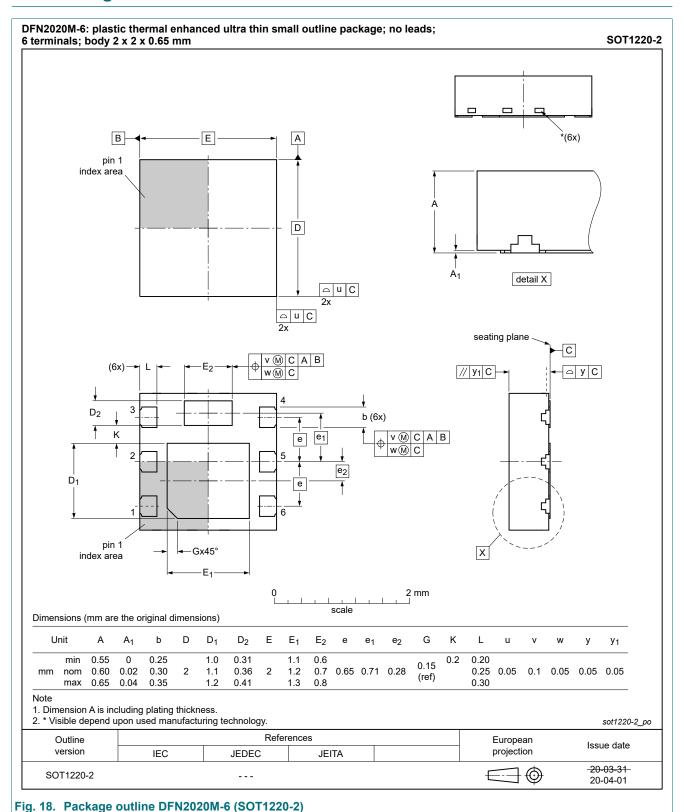
Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

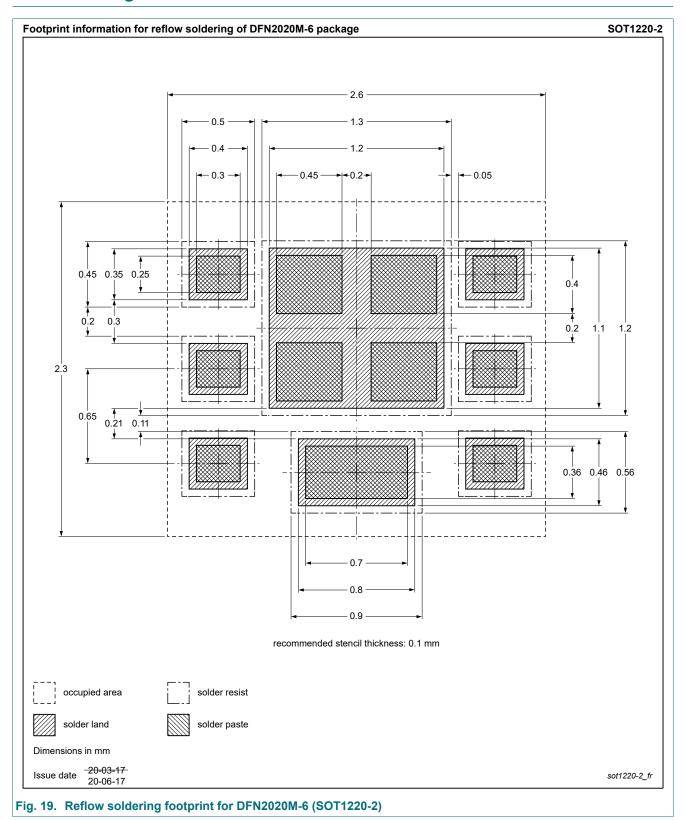


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12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB19R0UPE v.1	20220224	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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